A 1.28mW 100Mb/s Impulse UWB Receiver with Charge-Domain Correlator and Embedded Sliding Scheme for Data Synchronization

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Outline

• Introduction
  – Impulse Radio Ultra-Wideband (IR-UWB)

• Correlation-Based IR-UWB Receiver
  – Charge-Domain Sampling Correlator
  – Embedded Sliding Scheme for Data Synchronization

• Experimental Results

• Summary
Design Target

• Ultra Low Power RF Receiver
  – Low power (1mW)
  – High data rate (100Mbps)
  – Short distance (1m)

• Communication Method
  – Impulse UWB instead of OFDM-based UWB
  – DC-960MHz band instead of 3-10GHz band
  – BPSK modulation  ~~~~“1” ~~~~“0”
Conv. Impulse UWB Receiver (1): Thresholding-Based Architecture

- Any incoming pulse that crosses the threshold is detected and demodulated [2].

Pros: Simple Architecture $\Rightarrow$ Low Power
Cons: Sensitive to Noise $\Rightarrow$ Bad BER

Conv. Impulse UWB Receiver (2): Correlation-Based Architecture

- Correlation between the incoming signal and the template of the correlator [3].

- Pros: Robust to Noise ⇒ Good BER
- Cons: Analog Mixer & Sync ⇒ High Power

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- **Introduction**
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- **Correlation-Based IR-UWB Receiver**
  - Charge-Domain Sampling Correlator
  - Embedded Sliding Scheme for Data Synchronization

- **Experimental Results**

- **Summary**
Proposed Receiver Architecture

- $V_{out} > V_H, V_{cor} < V_L$: Converted to data bits.
- $V_L < V_{cor} < V_H$: Activating sliding scheme for sync.
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Principle of Correlation

Conventional
Continuous-Time
Voltage Domain [3]

$\int_{0}^{T} v_s(t)v_t(t-\tau)dt$

Discrete-Time
Voltage Domain

$\sum_{i=0}^{N-1} v_s[i]v_t[i-k]$

Discrete-Time
Charge Domain

$\sum_{i=0}^{N-1} v_s[i]C_t[i-k]$

Signal:
Voltage

Template:
Analog $\rightarrow$ High power

Charge-Domain Correlation

Incoming Signal:
(100Mb/s)

Template:

**Voltage**

- Capacitance
- CLK (2GHz)
- Time

Sampling Correlation:

\[ V_{\text{cor}} = \frac{V_{\text{DD}}}{2} + \sum_i C_i V_i / \sum_i C_i \]

- 2-GSa/s sampling of DC-960MHz band Gaussian pulse.
Charge-Domain Correlation

- Charge-Domain Sampling Correlator (CDSC)

Analog correlation is replaced with DC power-free charge-domain sampling correlator.

- Discrete template is determined by the capacitors.
Sampling Mode (1) of CDSC

- Sampling operation is implemented by turning on $\phi_1, \phi_2...\phi_7$ controlled switches sequentially.

- Sampling results are stored in the capacitors as $V_1, V_2...V_7$ respectively.
Sampling Mode (2) of CDSC

- Sampling operation is implemented by turning on $\phi_1$, $\phi_2$...$\phi_7$ controlled switches sequentially.

- Sampling results are stored in the capacitors as $V_1$, $V_2$...$V_7$ respectively.
Sampling Mode (3) of CDSC

- Sampling operation is implemented by turning on $\phi_1, \phi_2...\phi_7$ controlled switches sequentially.
- Sampling results are stored in the capacitors as $V_1, V_2...V_7$ respectively.
Sampling Mode (4) of CDSC

- Sampling operation is implemented by turning on $\phi_1, \phi_2...\phi_7$ controlled switches sequentially.

- Sampling results are stored in the capacitors as $V_1, V_2...V_7$ respectively.
Sampling Mode (5) of CDSC

- Sampling operation is implemented by turning on $\phi_1$, $\phi_2$…$\phi_7$ controlled switches sequentially.

- Sampling results are stored in the capacitors as $V_1$, $V_2$…$V_7$ respectively.
Sampling Mode (6) of CDSC

- Sampling operation is implemented by turning on $\phi_1, \phi_2...\phi_7$ controlled switches sequentially.

- Sampling results are stored in the capacitors as $V_1, V_2...V_7$ respectively.
Summing & Averaging Mode

- Stored voltages are weighted summed and averaged by turning on $\phi_r$ controlled switches.

- Subtraction operation is implemented by exchanging the two plate connections of the capacitors.
Summing & Averaging Mode

- Stored voltages are weighted summed and averaged by turning on $\phi_r$ controlled switches.

- Correlation results:

$$V_{\text{cor}} = \frac{V_{\text{DD}}}{2} + \left( \sum_{i=1}^{3} C_i V_i - \sum_{i=5}^{7} C_{8-i} V_i \right) / \sum_{i=1}^{3} 2C_i$$
Reset Mode of CDSC

- Correlator output is reset to $V_{DD}/2$ by clock $\phi_r$ after summing and averaging.

- After reset mode, correlator returns to sampling mode.
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Sliding Scheme for Sync

Phase Diagram of Discrete Template

Before Sync

Incoming Signal:

Template:

After Sync

10ns Cycle
20 Phase
(Step: 0.5ns)

θ = 0°

Phase Diagram of Discrete Template
Proposed Receiver Architecture

- Unlike tapped delay-line implementation [3], sliding scheme is achieved by utilizing the 2GHz clock for the sampling correlator.
Sliding Scheme

- \( V_{\text{cor}} < V_{\text{TH}} \Rightarrow \) Sliding scheme activated.

\[ V_L = \Delta V \]
\[ V_H = V_{\text{DD}} - \Delta V \]

Comparators

Pulse-Width Limiter

SR Latch

Clock Removal

Edge Combiner

20-Phase Sampling Clock Generator
Timing Chart (Out of Sync)

- $V_{\text{cor}} < V_{\text{TH}} \Rightarrow$ Sliding scheme activated.

- Clock removal signal: $RM = \phi_0 \& (UP \& DN)$

$RM = 0 \Rightarrow T_{\phi_0}$ is increased from 10ns to 10.5ns.
Timing Chart (In Sync)

- $V_{\text{cor}} > V_{\text{TH}} \Rightarrow$ Sliding scheme inactivated.

- $\text{RM} = 1 \Rightarrow T_{\phi_0}$ returns to 10ns and sync is achieved.
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Chip Micrograph and Layout

- 0.18 μm CMOS

Core area: 5561 μm²
Waveforms (Out of Sync)

- $V_{\text{cor}} < V_{\text{TH}} \Rightarrow$ Sliding scheme activated.

- Repeated phase-sliding $\Rightarrow T_{\phi3} = 10.5\text{ns}$.  

$V_{\text{in}}$ (100Mb/s)  
CLK (2GHz)  
$\phi_3$  
OUT

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>1</th>
</tr>
</thead>
</table>

$10.5\text{ns}$  
$19\text{ Pulses}$
Waveforms (In Sync)

- $V_{cor} > V_{TH} \Rightarrow$ Sliding scheme inactivated.

- Phase-sliding stopped $\Rightarrow T_{\phi_3} = 10\text{ns}$ (Sync achieved).
## Performance Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.18μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.8V</td>
</tr>
<tr>
<td>Data Rate</td>
<td>100Mbps</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>2GHz</td>
</tr>
<tr>
<td>Modulation</td>
<td>BPSK</td>
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### Power

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<table>
<thead>
<tr>
<th></th>
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</thead>
<tbody>
<tr>
<td>Correlator &amp; Synchronization</td>
<td>0.63mW</td>
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<tr>
<td>Clock Generator</td>
<td>0.53mW</td>
</tr>
<tr>
<td>Comparator</td>
<td>0.12mW</td>
</tr>
<tr>
<td>Total</td>
<td>1.28mW</td>
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<tr>
<td>Energy per bit</td>
<td>12.8pJ/bit</td>
</tr>
<tr>
<td>Core Area</td>
<td>5561μm²</td>
</tr>
</tbody>
</table>
Comparison with UWB RX’s

- Energy consumption: 12.8pJ/bit at 100Mbps
Summary

• DC-960MHz Band IR-UWB Receiver in 0.18\textmu m CMOS
  – Discrete-Time Charge-Domain Correlator
  – Sliding Scheme for Data Synchronization
• Compact receiver architecture
  – Achieving the lowest energy consumption of 12.8pJ/bit at 100Mbps in state-of-the-art correlation-based UWB receivers.
  – A potentially promising technology for low-cost and low-complexity wireless communications.