Switched Resonant Clocking (SRC) Scheme
Enabling Dynamic Frequency Scaling
and Low-Speed Test

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Abstract- A novel Switched Resonant Clocking (SRC) scheme is proposed to solve two basic problems of the conventional resonant clocking, that is, power increase and clock waveform instability at the lower clock frequency region. The power increase prohibits widely-used dynamic frequency scaling (DFS) and the waveform instability hinders low-speed function tests. A test chip in 0.18µm CMOS is manufactured and measured to show that the SRC suppresses power increase at low clock frequency and enables the low-speed tests, while reducing the clock power by 8% at 1.5-GHz clock with an area penalty of 4.8%.

I. INTRODUCTION

Decreasing the power of a clock distribution system in microprocessors and digital LSI's is a keen interest of designers, because the clocking power accounts for 10-40% of the total power. A resonant clock scheme is recently proposed [1-3] aiming at the clocking power reduction. By using the resonance of the large clock-node capacitance with an added inductor, the charging and discharging energy of the clock node can be recycled by means of an LC tank network. This results in the reduction of the clocking power. The effective clock frequency range of the resonant clock, however, is limited to the higher frequency region. For example, the microprocessor with the resonant clock in [3] successfully reduced the clocking power by 5-25% compared to the non-resonant clock at the target clock frequency of 4-5GHz. The resonant clocking in [3], however, showed much larger power than the non-resonant case in the lower frequency region below 3GHz. This is a problem when widely-used dynamic frequency scaling (DFS) [4] is employed. Moreover, the clock waveform is distorted and functional error arises at the frequency range below 1.6GHz due to the double count of the clock frequency. This prohibits low-speed testing of LSI's such as in wafer-level test. These two issues are obstacles for the resonant clocking to be widely used.

In this paper, a novel switched resonant clocking (SRC) scheme is proposed to solve both of the power increase and the waveform instability at the lower clock frequency region, while reducing the clock power at the target high frequency where maximum power consumption is observed.

II. PROBLEMS OF CONVENTIONAL RESONANT CLOCKING

Fig. 1 shows the conventional resonant clock distribution network [3]. The clock grid is driven by an H-tree. Inductors and decoupling capacitors (C_d) are added to the clock grid to resonate with the capacitance of the clock node [3].

In order to confirm the power increase at low clock frequency and the double switching, both the non-resonant clock circuit and the conventional resonant clock circuit were fabricated with 0.18µm CMOS. C_d and inductors were implemented with 330-pF chip capacitor and bonding wires, respectively.

Fig. 2 shows the measured clock power of the conventional resonant scheme. At 800MHz, the conventional resonant clock circuit achieved a maximum power reduction of 11% compared with the non-resonant clock circuit. At 150MHz, however, the power of the resonant clock circuit is 8.4 times larger than that of the non-resonant clock circuit.

Fig. 3 shows the equivalent circuits of the resonant clock.
Fig. 4 shows the measured waveforms of Clk in and Clk in the conventional resonant clock in Fig. 2 with clock frequency of 20MHz. Double switching is observed.

Fig. 3 shows equivalent circuits of the resonant clock circuit to explain the operation principle. At the resonant frequency of 800MHz, the capacitance of the clock loads ($C_{load}$) is resonated with the inductance ($L$), and the high impedance by the parallel resonance results in the lower power than the non-resonant clock as shown in Fig. 2. In contrast, at 150MHz, the low impedance by the series resonance of $C_d$ and $L$ results in the higher power than the non-resonant clock as shown in Fig. 2. The power increase at 150MHz is a serious problem of the resonant clock circuit if Dynamic Frequency Scaling is in use.

In order to solve the issues of the conventional resonant clocking, the Switched Resonant Clocking (SRC) scheme is proposed, whose schematic diagram is shown in Fig. 5. A switch is added in between the inductor and the decoupling capacitor ($C_d$). Usually adding a switch element in the resonant network is prohibited because it drastically reduces quality factor and damages the whole resonant characteristics. In this case, however, the major resonance is between the added inductor and the clock-grid capacitor, the resistance of the switch element does not affect the overall characteristics much.

In order to avoid the power increase and the double switching at low clock frequency, it is necessary to separate the inductor from the Clk node in Fig. 2(b) with a switch. Figs. 6(c) and (d) show two possible configurations of the switch (SW) location. Fig. 2(c) shows the proposed switched resonant clocking (SRC) and Fig. 2(d) shows a modified version of switched resonant clocking (mSRC). mSRC is shown to be a bad configuration because the main resonant tank includes the resistance of the added switch. Fig. 7 shows the simulated clock frequency dependence of the clock power for the non-resonant clocking, SRC and the mSRC where SW is turned on.

![Fig. 5 Proposed Switched Resonant Clocking (SRC).](image)

![Fig. 6 Equivalent circuit of various clock distribution circuits.](image)

![Fig. 7 Simulated clock frequency dependence of the clock power for the non-resonant clock, SRC and mSRC in Fig. 6.](image)
The power consumption of SRC is lower than that of the modified version at all frequency and lower than that of the non-resonant clock above 700MHz. In contrast, the power consumption of modified SRC is larger than that of the non-resonant clock at all frequency. The reason of the power difference between mSRC and SRC is as follows. Fig. 8 shows the equivalent circuits of SRC and mSRC. \( R_{tr} \) is the resistance of the transistor and \( C_d \) and \( C_{jd} \) are source and drain junction capacitance, respectively. As shown in Fig. 7, the power consumption of SRC is lower than that of mSRC, because \( C_{js} \) is directly added to \( C_{load} \) in mSRC (Fig. 8(b)), while \( C_{js} \) is connected to \( Clk \) node via \( L \) in SRC (Fig. 8(a)). Therefore, SRC instead of mSRC is adopted in this study.

It is also possible to insert SW in between \( C_d \) and the ground, but \( C_d \) is made with MOS capacitor so the parasitic capacitance may drastically increase.

The gate width \( W \) of the switch of SRC (Fig. 6(c)) is a critical design parameter in SRC. Here, it is shown that there is a trade-off in the choice of \( W \) between power reduction and waveform stability. The large \( W \) leads to large \( C_{js} / C_{jd} \) and small \( R_{tr} \), while the small \( W \) leads to small \( C_{js} / C_{jd} \) and large \( R_{tr} \). Fig. 9 shows the simulated clock frequency dependence of the clock power for the non-resonant clock and SRC with \( W \) of 10mm, 2mm and 0.5mm. By controlling SW depending on the clock frequency, the power increase problem of the resonant clock at low clock frequency is solved in SRC, because SRC where SW is turned on and SRC where SW is turned off have different power peaks. For example, in Fig. 9(a), the proposed SRC achieves the low power by turning off SW below 450MHz and turning on SW above 450MHz. The double switching problem of the resonant clock at low clock frequency is also solved in SRC.

In order to check the double switching characteristics, Fig. 10 shows the simulated waveform of \( Clk \) of SRC where SW is turned off at 450MHz clock with various \( W \) in Fig. 9. When \( W \) is 10mm, the severe double switching (Fig. 10(a)) and the large power increase at 450MHz compared with the non-resonant clock (Fig. 9(a)) are not acceptable, although the power reduction at 1.0GHz is large (Fig. 9(a)). In contrast, when \( W \) is 0.5mm, the small power reduction compared with the non-resonant clock (Fig. 9(c)) at high clock frequency is not attractive, although the no double switching (Fig. 10(c)) is observed.

Therefore, \( W \) of 2mm is adopted in this study in order to avoid the power increase (Fig. 9(b)) and the double switching (Fig. 10(b)) at low clock frequency, while reducing the clock power at high clock frequency.

IV. EXPERIMENTAL RESULTS

Figs. 11 (a) and (b) show the layout and the micrograph of a fabricated SRC test chip in 1.8V, 0.18\( \mu \)m CMOS respectively. Both \( L \) and \( C_d \) are integrated on chip using top interconnect layer and MOS capacitor. The die area is 0.8mm \( \times \) 0.93mm.

Table I shows a performance summary of SRC. In order to calculate the area penalty, the clock loads are converted to an
equivalent logic circuit. The calculated area penalty for the SRC is 4.8% assuming that the area of the flip-flops is 5% of the logic circuits.

Fig. 12(a) shows the measured clock frequency dependence of the clock power for the non-resonant clock and SRC where SW is turned on and off. By turning off SW below 850MHz and turning on SW above 850MHz, the proposed SRC can solve the power increase problem at low clock frequency and reduce the clock power at the target high clock frequency. Fig. 12(b) compares the measured clock frequency dependence of the clock power for the non-resonant clock, the conventional resonant clock in Fig. 2 and the SW-controlled SRC in Fig. 12(a). Compared with the non-resonant clock, the proposed SRC reduced the clock power by 8% at the target high clock frequency of 1.5GHz. Compared with the conventional resonant clock, the proposed SRC also reduced the clock power by 93% at the 20-MHz clock for the low-speed function tests. Fig. 13 shows the measured waveforms of Clkin and Clik for the non-resonant clock and SRC at 250MHz (low clock frequency) and 1.5GHz (target high clock frequency). The double switching was not observed.

V. CONCLUSIONS

Novel frequency scalable SRC circuits for high-speed microprocessors are proposed to solve the problems of both the power increase at low clock frequency in the DFS and the incompatibility to perform low-speed tests in the conventional resonant clock. The SRC test chips in 0.18µm CMOS reduces the clock power by 93% at 20-MHz clock and suppresses double switching at low clock frequency, while reducing the clock power by 8% at 1.5-GHz clock with an area penalty of 4.8%. The proposed SRC allows DFS and the low-speed tests, which expands the range of application of the resonant clock distributions.

Table I Performance Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>1.8V, 0.18µm CMOS</th>
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<tbody>
<tr>
<td>Area</td>
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<td></td>
</tr>
<tr>
<td>Clk buffers</td>
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</tr>
<tr>
<td>Clk loads</td>
<td>8930µm²</td>
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<tr>
<td>Equivalent</td>
<td>2741000µm² (a)</td>
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<tr>
<td>to logic area</td>
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</tr>
<tr>
<td>SRC</td>
<td></td>
</tr>
<tr>
<td>Inductor (1.6nH)</td>
<td>58750µm² (b)</td>
</tr>
<tr>
<td>Capacitor (Cp) (200pF)</td>
<td>64790µm² (c)</td>
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<tr>
<td>Switch</td>
<td>8733µm² (d)</td>
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<tr>
<td>Area Penalty</td>
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<td>(a)+(c)-(d) x 100</td>
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<tr>
<td>Maximum Power Reduction</td>
<td>8% at 1.8V, 1.5GHz</td>
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Fig. 12 Measured clock frequency dependence of the clock power. (a) Non-resonant clock and SRC where SW is turned on and off. (b) Non-resonant clock, conventional resonant clock and SW-controlled SRC.

Fig. 13 Measured waveforms of Clkin and Clik for the non-resonant clock and SRC at 250MHz and 1.5GHz.

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REFERENCES