Device-Circuit Interactions in Extremely Low Voltage CMOS Designs (Invited)

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Abstract

In this paper, energy and minimum operating voltage (VDDmin) are investigated for extremely-low-voltage CMOS logic designs. The dependences of energy and VDDmin on device parameters, such as threshold voltage, subthreshold swing parameter, and DIBL coefficient, are examined based on simulations and measurements.

Introduction

Extremely-low-voltage operation in VLSI’s is quite effective in reducing the power dissipation [1]. Fig. 1 shows simulated delay, power, and energy (power delay product) of a CMOS logic circuit. As the supply voltage (VDD) is reduced, the delay increases, whereas the power dissipation dramatically decreases. Therefore, extremely-low-voltage operation has been considered to be suitable for low-power applications in which circuit speed is not a primary concern or can be compensated by parallelization. For such applications, an energy per instructions is a key metric. As operation has been considered to be suitable for low-power applications in which circuit speed is not a primary concern or can be compensated by parallelization.

In this paper, what determines VDDmin is explained first, and then the dependences of VDDmin on energy on device parameters, such as threshold voltage, subthreshold swing parameter, and DIBL coefficient, are discussed.

Minimum Operating Voltage (VDDmin)

Fig. 2 shows a closed-form expression of VDDmin of logic gates where the number of gates is relatively large [3]. VDDmin can be expressed as a linear function of square-root of logarithm of the number of logic gates. This means that VDDmin rises as the number of logic gates increases. The slope of the function is proportional to the standard deviation of the within-die variation in the threshold voltage (VTH) difference between pMOS and nMOS transistors (σpn), and the intercept depends on the balance between intrinsic strengths of pMOS and nMOS transistors (β), device parameters, such as subthreshold swing parameter (n) and DIBL coefficient (η), and temperature (UT).

Fig. 3 illustrates VDDmin’s with various configurations of within-die VTH variation obtained by Monte Carlo SPICE simulations and the closed-form expression (Fig. 2). Simulated results indicate VDDmin is proportional to square-root of logarithm of the number of logic gates. Fig. 4 shows the dependence of VDDmin of inverter chain on σpn. As the number of gates increases, the rise in VDDmin due to within-die VTH variation is enlarged. This means mitigating VTH variation is effective in reducing VDDmin, especially for large-
scale circuits. For example, $V_{\text{DDmin}}$ of 100M inverters decreases by 87 mV if $\sigma_{pn}$ is reduced by 50%.

In addition, various gate chains were fabricated in a 65nm CMOS process, and $V_{\text{DDmin}}$'s of them were measured. The measurement results of the inverter and 2-input NAND chains are shown in Fig. 5. The closed-form expression (Fig. 2) also agrees with the measurement results.

Fig. 4 shows simulated $V_{\text{DDmin}}$'s of the inverter and NAND chains. $V_{\text{DDmin}}$'s of logic gates containing the larger number of stacked/paralleled transistors are much higher. This is because stacking and paralleling transistors contained in the NAND gate worsen the balance of the strength of pMOS and nMOS, which corresponds to the increase in parameter $|b|$ in the closed-form expression (Fig. 2). Although $V_{\text{DDmin}}$ can be reduced by adjusting the balance between the strength of pMOS and nMOS, it is usually impractical, since the gate sizes of either pMOS or nMOS transistors must be significantly enlarged for the adjustment, and hence it is not acceptable due to the area constraint [4]. Therefore, the logic gates with a lot of inputs should not be used in the design of extremely-low-voltage CMOS logic circuits.

In Fig. 6, it should be noted that the increase in the number of transistor stacks does not affect the slope which is proportional to $\sigma_{pn}$. It is well known that $\sigma_{pn}$ is proportional to $1/\sqrt{L \times W}$ [5]. For gate delays, transistor stack helps average gate delay variations induced by within-die $V_{\text{TH}}$. 
VI
\eta \propto \text{less than 0.3V.}

Fig. 9 illustrates the measured dependence of \( V_{DD_{\text{min}}} \) in a simplified energy model shown in Fig. 7. The decrease in \( V_{TH} \) can improve the circuit speed without any energy penalties.

Vopt is less than \( V_{TH} \), Vopt and Eopt hardly depend on \( V_{TH} \) [7].

On the other hand, \( V_{TH} \) itself does not determine \( V_{DD_{\text{min}}} \). Fig. 9 illustrates the measured dependence of \( V_{DD_{\text{min}}} \) in 100k-stage NAND2 chain on body bias of pMOS and nMOS [4]. When pMOS and nMOS are well-balanced, \( V_{DD_{\text{min}}} \) is lowest as shown in the optimal body bias line. In contrast, when pMOS and nMOS are unbalanced, \( V_{DD_{\text{min}}} \) increases. This is because \( V_{DD_{\text{min}}} \) does not depend on the absolute value of \( V_{TH} \) but is determined by the relative relation between pMOS and nMOS, which is represented by parameter \( |b| \) in the closed-form expression (Fig. 2).

Fig. 10 shows the dependence of the energy on subthreshold swing parameter \( n \); \( S=60\times n \text{mV/dec} \). \( V_{opt} \) and \( E_{opt} \) strongly depend on \( n \), and they are reduced as \( n \) decreases.

100k-stage NAND2 chain on body bias of pMOS and nMOS [4]. When pMOS and nMOS are well-balanced, \( V_{DD_{\text{min}}} \) is lowest as shown in the optimal body bias line. In contrast, when pMOS and nMOS are unbalanced, \( V_{DD_{\text{min}}} \) increases. This is because \( V_{DD_{\text{min}}} \) does not depend on the absolute value of \( V_{TH} \) but is determined by the relative relation between pMOS and nMOS, which is represented by parameter \( |b| \) in the closed-form expression (Fig. 2).

Fig. 10 shows the dependence of the energy on subthreshold swing parameter \( n \); \( S=60\times n \text{mV/dec} \). \( V_{opt} \) and \( E_{opt} \) are reduced as \( n \) decreases. Fig. 11 illustrates the dependence of \( V_{DD_{\text{min}}} \) of logic circuits on \( n \) obtained by the closed-form expression (Fig. 2). The decrease in \( n \) also reduces \( V_{DD_{\text{min}}} \).

Fig. 12 depicts the dependence of the energy on DIBL coefficient \( \eta \). While the energy does not depend on \( \eta \) for logic circuit, \( E_{opt} \) is reduced as \( \eta \) decreases for memory, since the influence of leakage energy increases as the activity factor \( \alpha \) is lowered.
Conclusion

In this paper, energy and $V_{DD_{min}}$ in extremely-low-voltage circuits were discussed. Insights obtained from the discussions are: (1) $V_{DD_{min}}$ is expressed as a function of the number of logic gates and its slope depends on within-die $V_{TH}$ variation. Thus, a mitigation of within-die $V_{TH}$ variation can significantly reduce $V_{DD_{min}}$. (2) The decrease in subthreshold swing parameter, that is, making the subthreshold slope steeper, is effective in reducing both the optimum energy ($E_{opt}$) and $V_{DD_{min}}$. (3) The decrease in DIBL coefficient ($\eta$), that is, mitigating the short-channel effect can reduce $E_{opt}$ of circuits with lower activity factors, such as memory.

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References