ASPIRE Workshop on Digital Transformation of Power Electronics for Data Centers

No registration required. Admission is free. Everyone is welcome.

Date: May 31, 2026, 1:00 PM to 5:00 PM
Venue: Kapiteinskamer I, Hilton Nagasaki
Address: 4-2 Onouemachi, Nagasaki, Japan
https://maps.app.goo.gl/o4ECp8J7RwgUksq19
https://www.hilton.com/en/hotels/ngsjphi-hilton-nagasaki/hotel-location/

Purpose of the Workshop:
This workshop aims to share recent advances in power electronics technologies for data centers and to strengthen international collaboration. It focuses on the development of digital gate platform technologies to improve energy efficiency and enable the digital transformation of power electronics. The workshop also provides a platform for researchers and students to exchange ideas, build global networks, and cultivate the next generation of leaders in this field.

Program (Edition of May 22, 2026)

Session 1: Oral Presentation (13:00 – 15:00)

Time	Presenter	Affiliation	Presentation Title
13:00 – 13:05	Makoto Takamiya	Univ. of Tokyo	Opening Remarks
13:05 – 13:30	Qiang Li	The University of Hong Kong	Advanced Power Converters with Integrated Magnetics for Data Centers
13:30 – 13:55	Jun Wang	University of Bristol	Advanced time-domain testing and modeling of power magnetics aided with AI
13:55 – 14:10	Makoto Takamiya	Univ. of Tokyo	Injecting Digital into Power Electronics via Gate Driver ICs
14:10 – 14:35	Yuhao Zhang	The University of Hong Kong	Application-Oriented Stability, Reliability, and Robustness of GaN Power Devices and ICs
14:35 – 15:00	Guo-Quan Lu	Virginia Tech	Advanced Power Electronics Packaging Materials

Coffee Break (15:00 – 15:15)

Session 2: Poster Session (15:15 – 17:00)

Presenter	Affiliation	Presentation Title
Che-An Cheng	Virginia Tech	CM Noise Modeling with Near-Field Couplings on GaN-Based PFC Converter
Yohei Sukita	Univ. of Tokyo	Method for Determining Switching Timing of Gate Drive Current of Active Gate Driver in SiC MOSFETs
Weijia Wang	Univ. of Tokyo	Stop-and-Go Active Gate Driver IC With Digitally Programmable Gate Current and 223-ps-Resolution Timing for SiC MOSFETs
Yichen Zhang	Univ. of Tokyo	4.5-W 5-V-Input DC-DC Converter With Six Isolated 15-V Outputs
Jiawei Huang	Univ. of Tokyo	Capacitive-Coupling Non-Contact Communication IC for Non-Contact Testing of HBM DRAM Chips
Juntian Chen	Univ. of Tokyo	Closed-Loop Real-Time Active Gate Driver IC for GaN in 22nm Process
Qingyang Tan	Tokyo Metropolitan Univ.	LLM-Guided Multi-Objective Co-Design of Circuit Parameters and Power Device Selection for Power Converters
Harutaka Suzuki	Tokyo Metropolitan Univ.	Optimal Primary Coil Placement in a Dual-Field Dynamic Wireless Power Transfer System
Kaiki Ueda	Tokyo Metropolitan Univ.	Design Method for a Low-Loss and Compact Inverter Used in a Magnetic Field Generator for Biological Applications
Satoshi Mikami	Tokyo Metropolitan Univ.	High-Accuracy Synchronization Method for Wireless Control of Power Modules with Built-in Gate Drive Circuits
Riku Takahashi	Tokyo Metropolitan Univ.	Fundamental Study on Transmission-Power Compensation in a Dynamic Wireless Power Transfer System with an Active Buffer
Yuto Saito	Tokyo Metropolitan Univ.	Inductor Design for Multilevel Converters Based on a Waveform-Emulation Iron-Loss Evaluation Method
Kotaro Oguchi	Tokyo Metropolitan Univ.	Rogowski Coil Array for High-Frequency Common-Mode Current Monitoring in MEA Propulsion Systems
Wataru Kodaka	Tokyo Metropolitan Univ.	Experimental Validation of an LLM-Based PI Gain Auto-tuning Method for a Half-bridge Inverter
Takachika Hatano	Tokyo Metropolitan Univ.	Design and Demonstration of a Rotation-Type Experimental System for Dynamic Wireless Power Transfer
Kazune Idei	Kyushu Univ.	Power Cycling Degradation Detection of Parallel SiC-MOSFETs Using Machine Learning on Switching Waveforms
Takehiro Ota	Kyushu Univ.	Transient Thermal Response Analysis in Power Cycling Degradation Detection Using the LHL Method
Haruki Nonaka	Kyushu Univ.	Shifts and Recovery of Device Characteristics in GaN-HEMTs
Shohei Zaizen	Kyushu Univ.	Impact of Emitter Parasitic Inductance on the Design of IGBT Power Modules Integrated with The Automatic Timing Control Digital Gate Driver

Sponsored by ASPIRE, Japan Science and Technology Agency (JST)

Contact Information Makoto Takamiya, University of Tokyo
Email: mtaka@iis.u-tokyo.ac.jp