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Research Interests

VLSI circuit design, specifically

(1) Low-voltage (0.5V)/low-power RF circuits for wireless sensor nodes
(2) Low-voltage (0.5V) power management circuits
(3) Power management circuits for energy harvesting
(4) Sub-0.5V low-voltage/low-power logic circuits
(5) Magnetically resonant wireless power transmission
(6) Large area and flexible electronics with organic transistors

Education

04/97 – 03/00 **Ph.D.** in Electronic Engineering, University of Tokyo, Japan
04/95 – 03/97 **M.S.** in Electronic Engineering, University of Tokyo, Japan
04/91 – 03/95 **B.S.** in Electronic Engineering, University of Tokyo, Japan

Academic Positions

04/05 – present **Associate Professor** in University of Tokyo, Japan
VLSI Design and Education Center
04/13 – 04/14 **Visiting Scholar** in University of California, Berkeley, USA
The Ubiquitous Swarm Lab, Prof. Jan Rabaey

Industry Positions

04/00 – 03/05 **Circuit designer** in NEC Corporation, Japan
Circuit design of high speed digital LSI's

Awards

[1] Best Paper Award, IEEE Wireless Power Transfer Conference (WPTC), 2013.
[2] Best Design Award in University LSI Design Contest, Asia-South Pacific Design Automation Conference (ASP-DAC), 2012.
[3] Paul Rappaport Award 2010 (Best paper in EDS publications), IEEE Electron Devices Society.
[4] IEEE SSCS Kansai Chapter Academic Research Award, IEEE Solid-State Circuits Society Kansai Chapter, 2011.
[5] Paul Rappaport Award 2009 (Best paper in EDS publications), IEEE Electron Devices Society.
[6] IEEE SSCS Kansai Chapter Academic Research Award, IEEE Solid-State Circuits Society Kansai Chapter, 2009.
[7] SSDM Young Researcher Award, International Conference on Solid State Devices and Materials, 1999.

Professional Activities

[1] Associate editor, IEICE Electronics Express (ELEX) (2013 -)

[2] Member, Technical Program Committee, IEEE International 3D Systems Integration Conference (3DIC) (2009 - 2013)

[3] Member, Technical Program Committee, IEEE Symposium on VLSI Circuits (2009 - 2014)

[4] Member, Technical Program Committee, Custom Applications and Low Power Techniques Sub-committee (2006), Custom Applications and Power Management Sub-committee (2007), Power Management Sub-committee (2008 - 2011), IEEE Custom Integrated Circuits Conference (CICC) (2006 - 2011)

[5] Member, Technical Program Committee, Advanced Silicon Circuits and Systems Sub-committee, International Conference on Solid State Devices and Materials (SSDM) (2003 - 2004)

Publications

(A) Book Chapters

[1] M. Takamiya, K. Ishida, T Sekitani, T. Someya, and T. Sakurai, "Organic Integrated Circuits for EMI Measurement," in the book entitled, "Stretchable Electronics", Editor: Takao Someya, Wilery-VCH, pp. 431-448, ISBN 978-3527329786, Feb. 2013.

[2] M. Takamiya, T. Sekitani, K. Ishida, T. Someya, and T. Sakurai, "Large Area Electronics with Organic Transistors," in the book entitled, "Applications of Organic and Printed Electronics", Editor: Eugenio Cantatore, Springer, pp. 101-113, ISBN 978-1461431596, Oct. 2012.

[3] M. Takamiya, K. Onizuka, K. Ishida, and T. Sakurai, "DC-DC Converter Technologies for On-Chip Distributed Power Supply Systems - 3D Stacking and Hybrid Operation," in the book entitled, "Emerging Technologies and Circuits", Editors: Amara Amara, Thomas Ea, and Marc Belleville, Springer, pp. 221-247, ISBN 978-9048193783, Sep. 2010.

[4] M. Takamiya, K. Onizuka, and T. Sakurai, "AC Coupled Wireless Power Delivery," in the book entitled, "Coupled Data Communication Techniques for High-Performance and Low-Power Computing", Editors: Ron Ho and Robert Drost, Springer, pp. 193-204, ISBN 978-1441965875, June 2010.

(B) Journals

[1] H. Fuketa, M. Nomura, M. Takamiya, and T. Sakurai, "Intermittent Resonant Clocking Enabling Power Reduction at Any Clock Frequency for Near/Sub-Threshold Logic Circuits," IEEE Journal of Solid-State Circuits, Vol.49, No.2, pp. 536-544, Feb. 2014.

[2] K. Takemura, K. Ishida, Y. Ishii, K. Maeda, M. Takamiya, T. Sakurai, and K. Baba, "Si Interposers with 15-um-thick Spiral Inductors and SrTiO3 Thin Film Capacitors for Novel 3D Stacked Buck Converters," Transactions of The Japan Institute of Electronics Packaging, Vol. 6, No. 1, pp. 78-86, 2013.

[3] H. Fuketa, R. Takahashi, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "Increase of Crosstalk Noise Due to Imbalanced Threshold Voltage Between nMOS and pMOS in Subthreshold Logic Circuits," IEEE Journal of Solid-State Circuits, Vol. 48, No. 8, pp. 1986-1994, Aug. 2013.

[4] H. Fuketa, K. Hirairi, T. Yasufuku, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "Minimizing Energy of Integer Unit by Higher Voltage Flip-Flop: VDDmin-Aware Dual Supply Voltage Technique," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 21, No. 6, pp. 1175-1179, June 2013.

[5] K. Ishida, T. -C. Huang, K. Honda, Y. Shinozuka, H. Fuketa, T. Yokota, U. Zschieschang, H. Klauk, G. Tortissier, T. Sekitani, H. Toshiyoshi, M. Takamiya, T. Someya, and T. Sakurai, "Insole Pedometer With Piezoelectric Energy Harvester and 2 V Organic Circuits," IEEE Journal of Solid-State Circuits, Vol.48, No.1, pp. 255-264, Jan. 2013.

[6] K. Mori, H. Lim, S. Iguchi, K. Ishida, M. Takamiya, and T. Sakurai, “Positioning-Free Resonant Wireless Power Transmission Sheet With Staggered Repeater Coil Array (SRCA),” IEEE Antennas and Wireless Propagation Letters, Vol. 11, pp. 1710-1713, Dec. 2012. (Invited)

[7] R. Takahashi, H. Takata, T. Yasufuku, H. Fuketa, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "Large Within-Die Gate Delay Variations in Sub-Threshold Logic Circuits at Low Temperature," IEEE Transactions on Circuits and Systems-II, Express Briefs, Vol.59, No.12, pp. 918-921, Dec. 2012.

[8] T. Yokota, T. Sekitani, T. Tokuhara, N. Take, U. Zschieschang, H. Klauk, K. Takimiya, T. -C. Huang, M. Takamiya, T. Sakurai, and T. Someya, "Sheet-Type Flexible Organic Active Matrix Amplifier System Using Pseudo-CMOS Circuits With Floating-Gate Structure," IEEE Transactions on Electron Devices, Vol. 59, No. 12, pp. 3434 - 3441, Dec. 2012.

[9] P. -H. Chen, X. Zhang, K. Ishida, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "An 80 mV Startup Dual-Mode Boost Converter by Charge-Pumped Pulse Generator and Threshold Voltage Tuned Oscillator With Hot Carrier Injection," IEEE Journal of Solid-State Circuits, Vol. 47, No. 11, pp. 2554-2562, Nov. 2012.

[10] X. Zhang, K. Ishida, H. Fuketa, M. Takamiya, and T. Sakurai, "On-Chip Measurement System for Within-Die Delay Variation of Individual Standard Cells in 65-nm CMOS," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 20, No. 10, pp. 1876-1880, Oct. 2012.

[11] N. Masunaga, K. Ishida, T. Sakurai, and M. Takamiya, "EMI Camera LSI (EMcam) with On-Chip Loop Antenna Matrix to Measure EMI Noise Spectrum and Distribution," IEICE Transaction on Electronics, E95-C, No.6, pp. 1059-1066, June 2012.

[12] L. Liu, T. Sakurai, and M. Takamiya, "A 315MHz Power-Gated Ultra Low Power Transceiver in 40nm CMOS for Wireless Sensor Network," IEICE Transaction on Electronics, E95-C, No.6, pp. 1035-1041, June 2012.

[13] X. Zhang, Y. Pu, K. Ishida, Y. Ryu, Y. Okuma, P. -H. Chen, K. Watanabe, T. Sakurai, and M. Takamiya, "A 1-V-Input Switched-Capacitor Voltage Converter with Voltage-Reference-Free Pulse-Density Modulation," IEEE Transactions on Circuits and Systems-II: Express Briefs, Vol.59, No.6, pp. 361-365, Jun. 2012.

[14] P. -H. Chen, K. Ishida, K. Ikeuchi, X. Zhang, K. Honda, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "Startup Techniques for 95 mV Step-Up Converter by Capacitor Pass-On Scheme and Vth-Tuned Oscillator With Fixed Charge Programming," IEEE Journal of Solid-State Circuits, Vol.47, No.5, pp. 1252-1260, May. 2012.

[15] K. Ishida, T. -C. Huang, K. Honda, T. Sekitani, H. Nakajima, H. Maeda, M. Takamiya, T. Someya, and T. Sakurai, "A 100-V AC Energy Meter Integrating 20-V Organic CMOS Digital and Analog Circuits With a Floating Gate for Process Variation Compensation and a 100-V Organic pMOS Rectifier," IEEE Journal of Solid-State Circuits, Vol.47, No.1, pp. 301-309, Jan. 2012.

[16] M. Daito, Y. Nakata, S. Sasaki, H. Gomyo, H. Kusamitsu, Y. Komoto, K. Iizuka, K. Ikeuchi, G. -S. Kim, M. Takamiya, and T. Sakurai, "Capacitively Coupled Non-Contact Probing Circuits for Membrane-Based Wafer-Level Simultaneous Testing," IEEE Journal of Solid-State Circuits, Vol.46, No.10, pp. 2386-2395, Oct. 2011.

[17] T. Yasufuku, Y. Nakamura, Z. Piao, M. Takamiya, and T. Sakurai, "Power Supply Voltage Dependence of Within-Die Delay Variation of Regular Manual Layout and Irregular Place-and-Route Layout," IEICE Transaction on Electronics, E94-C, No.6, pp. 1072-1075, June 2011.

[18] K. Ikeuchi, H. Kusamitsu, M. Daito, G. -S. Kim, M. Takamiya, and T. Sakurai, "1 Gb/s, 50um X 50um Pads on Board Wireless Connector Based on Track-and-Charge Scheme Allowing Contacted Signaling," IEICE Transaction on Electronics, E94-C, No.6, pp. 992-998, June 2011.

[19] L. Liu, T. Sakurai, and M. Takamiya, "0.6V Voltage Shifter and Clocked Comparator for Sampling Correlation-Based Impulse Radio UWB Receiver," IEICE Transaction on Electronics, E94-C, No.6, pp. 985-991, June 2011.

[20] X. Zhang, Y. Pu, K. Ishida, Y. Ryu, Y. Okuma, P. -H. Chen, T. Sakurai, and M. Takamiya, "A Variable Output Voltage Switched- Capacitor DC-DC Converter with Pulse Density and Width Modulation (PDWM) for 57% Ripple Reduction at Low Output Voltage," IEICE Transaction on Electronics, E94-C, No.6, pp. 953-959, June 2011.

[21] Y. Okuma, K. Ishida, Y. Ryu, X. Zhang, P. -H. Chen, K. Watanabe, M. Takamiya, and T. Sakurai, "0.5-V Input Digital Low-Dropout Regulator (LDO) with 98.7% Current Efficiency in 65nm CMOS," IEICE Transaction on Electronics, E94-C, No.6, pp. 938-944, June 2011.

[22] K. Ishida, T. Yasufuku, S. Miyamoto, H. Nakai, M. Takamiya, T. Sakurai, and K. Takeuchi, "1.8 V Low-Transient-Energy Adaptive Program-Voltage Generator Based on Boost Converter for 3D-Integrated NAND Flash SSD," IEEE Journal of Solid-State Circuits, Vol.46, No.6, pp. 1478-1487, June 2011.

[23] L. Liu, T. Sakurai, and M. Takamiya, "A Charge-Domain Auto- and Cross-Correlation Based Data Synchronization Scheme With Power-and Area-Efficient PLL for Impulse Radio UWB Receiver," IEEE Journal of Solid-State Circuits, Vol.46, No.6, pp. 1349-1359, June 2011.

[24] Y. Pu, X. Zhang, K. Ikeuchi, A. Muramatsu, A. Kawasumi, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "Post-Silicon Clock Deskew Employing Hot-Carrier Injection Trimming With On-Chip Skew Monitoring and Auto-Stressing Scheme for Sub/Near Threshold Digital Circuits," IEEE Transactions on Circuits and Systems-II, Vol. 58, No. 5, pp. 294-298, May 2011.

[25] T. Yokota, T. Nakagawa, T. Sekitani, Y. Noguchi, K. Fukuda, U. Zschieschang, H. Klauk, K. Takeuchi, M. Takamiya, T. Sakurai, and T. Someya, "Control of Threshold Voltage in Low-Voltage Organic Complementary Inverter Circuits with Floating Gate Structures," Applied. Physics. Letters, 98, 193302, May 2011.

[26] P. -H. Chen, K. Ishida, X. Zhang, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "0.18-V Input Charge Pump with Forward Body Bias to Startup Boost Converter for Energy Harvesting Applications," IEICE Transaction on Electronics, E94-C, No.4, pp.598-604, Apr. 2011.

[27] K. Johguchi, T. Hatanaka, K. Ishida, T. Yasufuku, M. Takamiya, T. Sakurai, and K. Takeuchi, "Through-Silicon Via Design for a 3-D Solid-State Drive System With Boost Converter in a Package," IEEE Transaction on Components, Packaging and Manufacturing Technology, Vol.1, No.2, pp. 269-277, Feb. 2011.

[28] K. Ishida, N. Masunaga, R. Takahashi, T. Sekitani, S. Shino, U. Zschieschang, H. Klauk, M. Takamiya, T. Someya, and T. Sakurai, "User Customizable Logic Paper (UCLP) with Sea-of Transmission-Gates (SOTG) of 2-V Organic CMOS and Ink-Jet Printed Interconnects," IEEE Journal of Solid-State Circuits, Vol.46, No.1, pp. 285-292, Jan. 2011.

[29] L. Liu, Z. Zhou, T. Sakurai, and M. Takamiya, "A 1.76mW, 100Mbps Impulse Radio UWB Receiver with Multiple Sampling Correlators Eliminating Need for Phase Synchronization in 65-nm CMOS," IEICE Transaction on Electronics, E93-C, No.6, pp. 796-802, June 2010.

[30] Y. Kato, T. Sekitani, Y. Noguchi, T. Yokota, M. Takamiya, T. Sakurai and T, Someya, "Large-Area Flexible Ultrasonic Imaging System With an Organic Transistor Active Matrix," IEEE Transactions on Electron Devices, Vol. 57, No. 5, pp. 995 - 1002, May 2010.

[31] T. Yasufuku, T. Niiyama, Z. Piao, K. Ishida, M. Murakata, M. Takamiya, and T. Sakurai, "Difficulty of Power Supply Voltage Scaling in Large Scale Subthreshold Logic Circuits,"IEICE Transaction on Electronics, E93-C, No.3, pp.332-339, March 2010.

[32] T. Yasufuku, K. Ishida, S. Miyamoto, H. Nakai, M. Takamiya, and T. Sakurai, "Inductor and TSV Design of 20-V Boost Converter for Low Power 3D Solid State Drive with NAND Flash Memories ,"IEICE Transaction on Electronics, E93-C, No.3, pp.317-323, March 2010.

[33] K. Ishida, N. Masunaga, Z. Zhou, T. Yasufuku, T. Sekitani, U. Zschieschang, H. Klauk, M. Takamiya, T. Someya, and T. Sakurai, "Stretchable EMI Measurement Sheet With 8 X 8 Coil Array, 2 V Organic CMOS Decoder, and 0.18 um Silicon CMOS LSIs for Electric and Magnetic Field Detection," IEEE Journal of Solid-State Circuits, Vol. 45, No. 1, pp. 249-259, Jan. 2010.

[34] T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai, and T. Someya, "Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays," Science, Vol. 326, pp. 1516 - 1519, Dec. 2009.

[35] L. Liu, M. Takamiya, T. Sekitani, Y. Noguchi, S. Nakano, K. Zaitsu, T. Kuroda, T. Someya, and T. Sakurai, "A 107-pJ/bit 100-kb/s 0.18-um Capacitive-Coupling Transceiver With Data Edge Signaling and DC Power-Free Pulse Detector for Printable Communication Sheet," IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 56, No. 11, pp. 2511 - 2518, Nov. 2009.

[36] G.-S. Kim, M. Takamiya, and T. Sakurai, "A 25-mV-Sensitivity 2-Gb/s Optimum-Logic-Threshold Capacitive-Coupling Receiver for Wireless Wafer Probing Systems,"IEEE Transactions on Circuits and Systems―II: Express Briefs, Vol. 56, No. 9, pp. 709 - 713, Sep. 2009.

[37] L. Liu, Y. Miyamoto, Z. Zhou, K. Sakaida, J. Ryu, K. Ishida, M. Takamiya, and T. Sakurai, "A 100Mbps, 4.1pJ/bit Threshold Detection-Based Impulse Radio UWB Transceiver in 90nm CMOS ," IEICE Transaction on Electronics, E92-C, No.6, pp.769-776, June 2009.

[38] T. Sekitani, K. Zaitsu, Y. Noguchi, K. Ishibe, M. Takamiya, T. Sakurai, and T. Someya, "Printed Nonvolatile Memory for a Sheet-Type Communication System ," IEEE Transactions on Electron Devices, Vol. 56, No. 5, pp. 1027 - 1035, May 2009.

[39] Y. Nakamura, M. Takamiya, and T. Sakurai, "An On-Chip Noise Canceller with High Voltage Supply Lines for Nanosecond-Range Power Supply Noise," IEICE Transaction on Electronics, E92-C, No.4, pp.468-472, April 2009.

[40] M. Takamiya and T. Sakurai, "Low Power VLSI Circuit Design with Fine-Grain Voltage Engineering," IPSJ Transactions on System LSI Design Methodology, Vol. 2, pp. 18 - 29, Feb. 2009. (Invited)

[41] D. Levacq, M. Takamiya, and T. Sakurai, "Backgate Bias Accelerator for sub-100 ns Sleep-to-Active Modes Transition Time," IEEE Journal of Solid-State Circuits, Vol. 43, No. 11, pp. 2390 - 2395, Nov. 2008.

[42] K. Onizuka, K. Inagaki, H. Kawaguchi, M. Takamiya, and T. Sakurai, "Stacked-Chip Implementation of On-Chip Buck Converter for Distributed Power Supply System in SiPs," IEEE Journal of Solid-State Circuits, Vol. 42, No. 11, pp. 2404 - 2410, Nov. 2007.

[43] K. Ishida, A. Tamtrakarn, H. Ishikuro, M. Takamiya, and T. Sakurai, "An Outside-Rail Opamp Design Relaxing Low-Voltage Constraint on Future Scaled Transistors," IEICE Transaction on Electronics, E90-C, No.4, pp.786-792, April 2007.

[44] Y. Kato, T. Sekitani, M. Takamiya, M. Doi, K. Asaka, T. Sakurai, and T. Someya, "Sheet-Type Braille Displays by Integrating Organic Field-Effect Transistors and Polymeric Actuators ", IEEE Transactions on Electron Devices, Vol. 54, No. 2, pp. 202 - 209, Feb. 2007.

[45] M. Takamiya, T. Sekitani, Y. Kato, H. Kawaguchi, T. Someya, and T. Sakurai, "An Organic FET SRAM with Back Gate to Increase Static Noise Margin and its Application to Braille Sheet Display," , IEEE Journal of Solid-State Circuits, Vol. 42, No. 1, pp. 93 - 100, Jan. 2007.

[46] K. Onizuka, H. Kawaguchi, M. Takamiya, and T. Sakurai, "VDD-Hopping Accelerators for On-Chip Power Supply Circuit to Achieve Nanosecond-Order Transient Time," IEEE Journal of Solid-State Circuits, Vol. 41, No. 11, pp. 2382 - 2389, Nov. 2006.

[47] S. Iba, T. Sekitani, Y. Kato, T. Someya, H. Kawaguchi, M. Takamiya, T. Sakurai, and, S. Ta-kagi, "Control of Threshold Voltage of Organic Field-Effect Transistors with Double Gate Structure," Applied Physics Letters, 87, 023509, July 2005.

[48] M. Takamiya and M. Mizuno, "A 6.7-fF/um2 Bias-Independent Gate Capacitor (BIGCAP) with Digital CMOS Process and its Application to the Loop Filter of a Differential PLL", IEEE Journal of Solid-State Circuits, Vol. 40, No. 3, pp. 719 - 725, Mar. 2005.

[49] M. Takamiya and T. Hiramoto, "High Drive-Current Electrically Induced Body Dynamic Threshold SOI MOSFET (EIB-DTMOS) with Large Body Effect and Low Threshold Voltage", IEEE Transactions on Electron Devices, Vol. 48, No. 8, pp. 1633 - 1640, Aug. 2001.

[50] T. Hiramoto, M. Takamiya, H. Koura, T. Inukai, H. Gomyo, H. Kawaguchi, and T. Sakurai, "Optimum Device Parameters and Scalability of Variable Threshold Voltage Complementary MOS (VTCMOS)", Japanese Journal of Applied Physics, Vol. 40, Part 1, No. 4B, pp. 2854 - 2858, April, 2001.

[51] Y. Yasuda, M. Takamiya, and T. Hiramoto, "Threshold Voltage Fluctuations Induced by Statistical "Position" and "Number" Impurity Fluctuations in Bulk MOSFETs", Superlattices and Microstructures, Vol. 28, No. 5/6, pp. 357 - 361, November/December, 2000.

[52] Y. Yasuda, M. Takamiya, and T. Hiramoto, "Separation of Effects of Statistical Impurity Number Fluctuations and Position Distribution on Vth Fluctuations in Scaled MOSFETs", IEEE Transactions on Electron Devices, Vol. 47, No. 10, pp. 1838 - 1842, October, 2000.

[53] H. Koura, M. Takamiya, and T. Hiramoto, “Optimum Conditions of Body Effect Factor and Substrate Bias in Variable Threshold Voltage MOSFETs” Japanese Journal of Applied Physics, Vol. 39, No. 4B, pp. 2312 - 2317, April, 2000.

[54] T. Hiramoto and M. Takamiya, “Low Power and Low Voltage MOSFETs with Variable Threshold Voltage Controlled by Back-Bias”, IEICE Transaction on Electronics, E83-C, pp.161-169, Feb. 2000. (Invited Paper)

[55] T. N. Duyet, H. Ishikuro, Y. Shi, T. Saraya, M. Takamiya, and T. Hiramoto, "Measurement of Energetic and Lateral Distribution of Interface State Density in Fully-Depleted Silicon on Insulator Metal-Semiconductor Field-Effect Transistors", Japanese Journal of Applied Physics, Vol. 38, No. 4B, pp. 2496 - 2500, April, 1999.

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[57] T. Mukaiyama, K. Saito, H. Ishikuro, M. Takamiya, T. Saraya, and T. Hiramoto, "Fabrication of Gate-All Around MOSFET by Silicon Anisotropic Etching Technique", Solid State Electronics, Vol. 42, No. 7-8, pp. 1623 - 1626, July - August, 1998.

[58] T. N. Duyet, H. Ishikuro, M. Takamiya, T. Saraya, and T. Hiramoto, "Suppression of Geometric Component of Charge Pumping Current in Thin Film SOI MOSFET", Japanese Journal of Applied Physics, Part 2, Vol. 37, No. 7B, pp. L855 - L858, July, 1998.

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(C) Conference Papers

[1] M. Takamiya, "Extremely Low-Power Circuit Design for Wearable Systems," IEEE International Solid-State Circuits Conference (ISSCC), Evening Session, "Wearable Wellness Devices: Fashion, Health, and Informatics", San Francisco, USA, Feb. 2014. (Invited)

[2] H. Fuketa, K. Yoshioka, T. Yokota, W. Yukita, M. Koizumi, M. Sekino, T. Sekitani, M. Takamiya, T. Someya, and T. Sakurai, "Organic-Transistor-Based 2kV ESD-Tolerant Flexible Wet Sensor Sheet for Biomedical Applications with Wireless Power and Data Transmission Using 13.56MHz Magnetic Resonance," IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, USA, pp. 490-491, Feb. 2014.

[3] T. Someya, T. Sekitani, M. Kaltenbrunner, T. Yokota, H. Fuketa, M. Takamiya, and T. Sakurai, "Ultraflexible Organic Devices for Biomedical Applications," IEEE International Electron Devices Meeting (IEDM), Washington DC, USA, pp. 8.5.1-8.5.4, Dec. 2013. (Invited)

[4] X. Zhang, Y. Okuma, P. -H. Chen, K. Ishida, Y. Ryu, K. Watanabe, T. Sakurai, and M. Takamiya, "A 0.6-V Input 94% Peak Efficiency CCM/DCM Digital Buck Converter in 40-nm CMOS with Dual-Mode-Body-Biased Zero-Crossing Detector," IEEE Asian Solid-State Circuits Conference (A-SSCC), Singapore, pp. 45-48, Nov. 2013.

[5] H. Fuketa, R. Takahashi, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "Variation-aware Subthreshold Logic Circuit Design," IEEE International Conference on ASIC (ASICON), Shenzhen, China, pp. 95-98, Oct. 2013. (Invited)

[6] A. Borna, M. Takamiya, and J. Rabaey, "The Path Toward Energy-Efficient Inference Engine Architectures on Scaled and Beyond-CMOS Fabrics," Third Berkeley Symposium on Energy Efficient Electronic Systems, Berkeley, USA, Oct. 2013.

[7] M. Takamiya, "Energy Efficient 0.5V Logic, RF, and Power Management Circuits," IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Monterey, USA, Oct. 2012. (Invited)

[8] K. Mori, Y. Okuma, X. Zhang, H. Fuketa, T. Sakurai, and M. Takamiya, "Analog-Assisted Digital Low Dropout Regulator (AAD-LDO) with 59% Faster Transient Response and 28% Ripple Reduction,"

International Conference on Solid State Devices and Materials (SSDM), Fukuoka, Japan, pp. 888-889, Sep. 2013.

[9] S. Yoshimoto, S. Miyano, M. Takamiya, H. Shinohara, H. Kawaguchi, and M. Yoshimoto, "A 40-nm 8T SRAM with Selective Source Line Control of Read Bitlines and Address Preset Structure," IEEE Custom Integrated Circuits Conference (CICC), San Jose, USA, pp. 1-4, Sep. 2013.

[10] H. Fuketa, K. Ishida, T. Sekitani, M. Takamiya, T. Someya, and T. Sakurai, "Large-Area and Flexible Sensors with Organic Transistors," IEEE International Workshop on Advances in Sensors and Interfaces (IWASI), Bari, Italy, pp. 87-90, June 2013. (Invited)

[11] S. Iguchi, A. Saito, Y. Zheng, K. Watanabe, T. Sakurai, and M. Takamiya, "93% Power Reduction by Automatic Self Power Gating (ASPG) and Multistage Inverter for Negative Resistance (MINR) in 0.7V, 9.2μW, 39MHz Crystal Oscillator," IEEE Symposium on VLSI Circuits, Kyoto, pp. C142-C143, June 2013.

[12] M. Nomura, A. Muramatsu, H. Takeno, S. Hattori, D. Ogawa, M. Nasu, K. Hirairi, S. Kumashiro, S. Moriwaki, Y. Yamamoto, S. Miyano, Y. Hiraku, I. Hayashi, K. Yoshioka, A. Shikata, H. Ishikuro, M. Ahn, Y. Okuma, X. Zhang, Y. Ryu, K. Ishida, M. Takamiya, T. Kuroda, H. Shinohara, and T. Sakurai, "0.5V Image Processor with 563 GOPS/W SIMD and 32bit CPU Using High Voltage Clock Distribution (HVCD) and Adaptive Frequency Scaling (AFS) with 40nm CMOS," IEEE Symposium on VLSI Circuits, Kyoto, pp. C36-C37, June 2013.

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