# Deep Sub-0.1μm Fully Depleted SOI MOSFET's with Ultra-Thin Silicon Film and Thick Buried Oxide for Low-Power Applications

*Student paper*

Makoto Takamiya[1], Yuri Yasuda[1], and Toshiro Hiramoto[1,2]
[1] Institute of Industrial Science, University of Tokyo, Tokyo, Japan
[2] VLSI Design and Education Center, University of Tokyo, Japan
E-mail: taka@nano.iis.u-tokyo.ac.jp

## Abstract

We propose device structures of ultra thin FD SOI MOSFETs for very low power applications. In order to design such devices, a novel scaling methodology for FD SOI MOSFETs has been developed and a scaling scenario to the deep sub-0.1 μm regime is shown. The short channel effect is suppressed by ultra thin SOI film and the steep subthreshold slope is achieved by thick buried oxide. It is also shown by means of 2D-device simulation that FD SOI MOSFETs will be miniaturized further than bulk MOSFETs without degrading the steep subthreshold slope and increasing *Vth* fluctuations, even if the gate oxide thickness is not scaled.

## 1. Introduction

Fully depleted (FD) SOI MOSFETs are attractive for very low power applications due to low parasitic capacitances and a steep subthreshold slope. These merits come from the existence of a buried oxide. The scaling of FD SOI MOSFETs is also promising because the channel depletion width can be limited by the SOI thickness. Several scaled SOI MOSFETs have been proposed or fabricated, and their performances have been confirmed [1-4]. However, they are not suitable for low power applications because the subthreshold slope has been greatly degraded and parasitic capacitances have increased due to thin buried oxide. In this paper, we propose device structures of ultra thin FD SOI MOSFETs for very low power applications. Special attention has been paid to the degradation of the subthreshold slope.

## 2. Ultra Thin FD SOI MOSFETs

Fig. 1 shows the proposed device structure of a 0.05 μm channel length FD SOI MOSFET. Short channel effect is suppressed by the ultra thin SOI. The non-doped channel reduces *Vth* fluctuations. To realize the steep subthreshold slope and low parasitic capacitances, buried oxide thickness remains thick. Key processes of FD SOI MOSFETs are the reduction of S/D resistance and the gate material for *Vth* adjustment. The S/D resistance is reduced by the selective Si epitaxial growth and the subsequent silicide [4,5], and mid-gap material [6-8] is utilized for the gate electrodes as shown in Fig. 1. The proposed device structure is based on the scaling scenario we have developed for low power FD SOI MOSFETs. The detailed scaling methodology and the comparison with conventional bulk MOSFETs are described in the following sections.

## 3. Scaling Methodology for FD SOI MOSFETs

Fig. 2 shows a schematic view of FD SOI MOSFETs. We considered four device parameters; gate oxide thickness ($t_{fox}$), SOI thickness ($t_{SOI}$), buried oxide thickness ($t_{box}$), and channel doping concentration ($N_A$). As shown in Fig.3, subthreshold swing ($S$) is roughly determined by the ratio of $t_{fox}$ to $t_{box}$. To realize $S$ lower than 65 mV/dec, $t_{box}$ should be more than ten times as thick as $t_{fox}$. To understand the degradation of $S$ by the short channel effect (SCE), we have derived the potential at the back interface by solving a 2D Poisson's equation analytically. Here, we have introduced the natural length ($\lambda$) [9-11] and modified for the ultra thin FD SOI MOSFETs.

$$\lambda \equiv \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left(1+\frac{\varepsilon_{ox}}{2\varepsilon_{Si}}\frac{t_{SOI}}{t_{fox}}\right)\cdot t_{SOI}\cdot t_{fox}} \qquad (1)$$

Fig. 4 (a) shows the simulation [12] results of $S$ degradation by SCE for four generations below 0.1 μm

listed in Table 1. When $L_{eff}$ is normalized by $\lambda$, the degradation of $S$ shows a universal curve as shown in Fig. 4 (b). It is found that $S$ is always 80mV/dec when $L_{eff} = 6\lambda$. This means that $t_{fox}$ and $t_{SOI}$ only have an influence on SCE of FD SOI MOSFETs and that SCE can be suppressed even if $t_{box}$ is thick.

Fig. 5 (a) summarizes the scaling scenario of FD SOI MOSFETs to the deep sub-0.1 μm regime developed by the above mentioned analytical results. A criterion of SCE is set to $S$ = 80mV/dec (i.e. $L_{eff} = 6\lambda$). Each curve corresponds to $S$ = 80 mV/dec. In the lower left region of each curve, SCE can be suppressed in each generation. Scaling of $t_{fox}$ and $V_{dd}$ is assumed as shown in Figs. 5 (b) and (c). At $L_{eff}$ shorter than 0.15 μm, $t_{fox}$ is assumed to remain 30 Å by the direct tunneling limit. This result shows that the FD SOI MOSFETs can be scaled by thinning $t_{SOI}$ even if the $t_{fox}$ is constant. The constant $t_{fox}$ scaling doesn't enhance the speed greatly, but it can reduce power consumption drastically compared with the conventional scaling.

## 4. Comparison with Bulk MOSFET's

### *A. Short Channel Effect*

When gate oxide thickness ($t_{fox}$) does not scale as shown in Fig. 5 (b), SCE of bulk MOSFETs can be suppressed only by the reduction of the channel depletion width and S/D junction depth ($X_j$). Fig.6 shows $S$ vs. $N_A$ for long channel bulk MOSFETs. Although SCE can be suppressed, increasing $N_A$ (i.e. decreasing the channel depletion width) degrades $S$ of long channel bulk MOSFETs when $t_{fox}$ is constant. Fig. 7 compares the degradation of $S$ in bulk MOSFETs (constant $N_A$) with FD SOI MOSFETs. The device parameters are shown in Tables 1 and 2. In the 0.1 μm generation, bulk MOSFETs show better SCE than FD SOI MOSFETs [1,7]. In the 0.03 μm generation, however, bulk MOSFETs show worse SCE than FD SOI MOSFETs. This is because the channel depletion width is not scaled in bulk MOSFETs with constant $N_A$. In FD SOI MOSFETs, the channel depletion width is scaled with $t_{SOI}$ and the degradation of $S$ is suppressed even if $N_A$ is non-doped.

### *B. Vth Fluctuations*

In FD SOI MOSFETs, *Vth* is controlled by $N_A$ within a range of fully depletion. However, to adjust *Vth* to a proper value in case of the $N^+$ poly Si gate, higher $N_A$ is required with the scaling and causes the problem of *Vth* fluctuations. Fig.8 shows calculated *Vth* fluctuations of FD SOI MOSFETs as a function of $L_{eff}$. The statistical variation of channel dopant number [13] and the process variation of $t_{SOI}$ are considered. *Vth* is set to the value in the inset. *Vth* fluctuations increase with scaling down the device sizes. On the other hand, FD SOI MOSFETs with non-doped $N_A$ would reduce *Vth* fluctuations drastically, because *Vth* is determined only by the work function difference. Therefore, FD SOI MOSFETs should be miniaturized with non-doped $N_A$ rather than high $N_A$, and *Vth* should be adjusted by midgap material for gate electrode.

## 5. Conclusions

We have proposed device structures of ultra thin FD SOI MOSFETs for very low power applications. In order to design such devices, a novel scaling methodology for FD SOI MOSFETs is developed and a scaling scenario to the deep sub-0.1 μm regime is shown. Scaling of the gate oxide thickness and the SOI thickness is essential. The ultra thin SOI film suppresses the short channel effect and the thick buried oxide achieves the steep subthreshold slope. Using the proposed methodology, we have shown that, unlike bulk MOSFETs, FD SOI MOSFETs will be miniaturized further by thinning the SOI thickness without degrading the steep subthreshold slope and increasing *Vth* fluctuations, even if the gate oxide thickness is not scaled.

## References


[1] Y.Omura et al: IEDM Tech. Dig., pp.675-678, 1991
[2] L.T.Su et al: IEEE Electron Device Lett., vol.15, no.9, pp.366-369, 1994
[3] T.Shimatani et al: Ext. Abs. SSDM, pp.494-496, 1996
[4] M.Cao et al: IEEE Electron Device Lett., vol.18, no.6, pp.251-253, 1997
[5] Y.Nakahara et al: Symp. on VLSI Tech. Dig., pp.174-175, 1996
[6] J.M.Hwang et al: IEDM Tech. Dig.,pp.345-348,1992
[7] N.Kistler et al: IEDM Tech. Dig.,pp.727-730,1993
[8] H.Shimada et al: IEDM Tech. Dig.,pp.881-884,1995
[9] R.H.Yan et al: IEEE Trans. Electron Devices, vol.39, no.7, pp.1704-1710, 1992
[10] K.Suzuki et al: IEEE Trans. Electron Devices, vol.40, no.12, pp.2326-2329, 1993
[11] G.F.Niu et al: IEEE Trans. Electron Devices, vol.43, no.11, pp.2034-2037, 1996
[12] "TMA MEDICI Ver 2.3 User's Manual", Technology Modeling Associates, Inc., 1997
[13] T.Mizuno : Jpn. J. Appl. Phys. Vol.35, pp.842-848, 1996

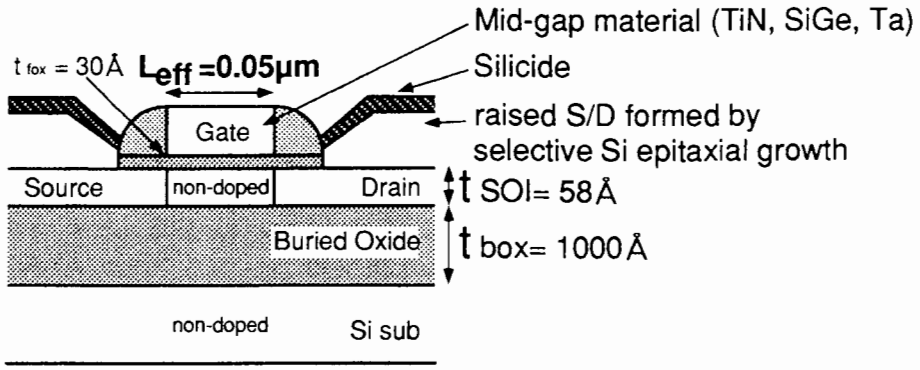



**Fig.1** The proposed device structure of a 0.05μm FD SOI MOSFET. Short channel effect is suppressed by the ultra thin SOI. The steep subthreshold slope and low parasitic capacitances are realized by the thick buried oxide. The non-doped SOI reduces Vth fluctuations.

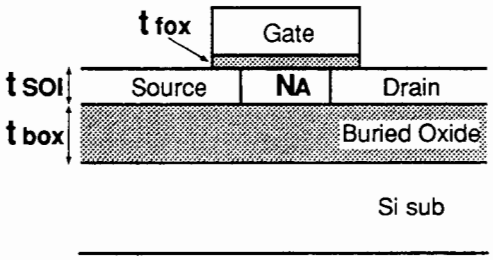



**Fig.2** Schematic of FD SOI MOSFETs.

**Table.1** Device parameters of FD SOI MOSFETs below 0.1μm. They are based on Fig.5 (a).

| | type A | type B | type C | type D |
|---|---|---|---|---|
| $t_{fox}$ | 30Å | ← | ← | ← |
| $t_{SOI}$ | 162Å | 98Å | 58Å | 24Å |
| $t_{box}$ | 1000Å | ← | ← | ← |
| $N_A$ | $1\times10^{15}$ cm$^{-3}$ | ← | ← | ← |
| $N_{sub}$ | $1\times10^{15}$ cm$^{-3}$ | ← | ← | ← |
| $V_{ds}$ | 1V | 0.84V | 0.71V | 0.55V |
| | 0.1μm Generation | 0.07μm Generation | 0.05μm Generation | 0.03μm Generation |

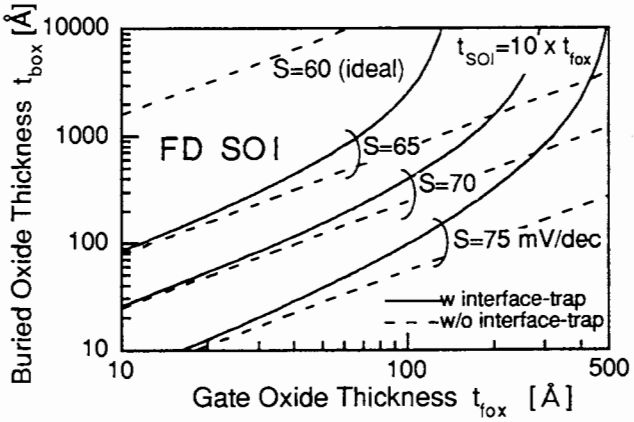
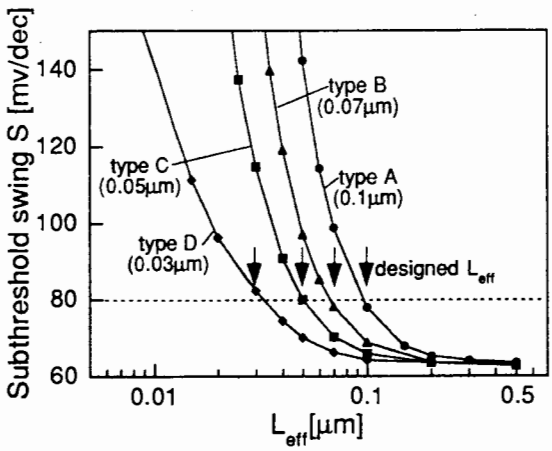
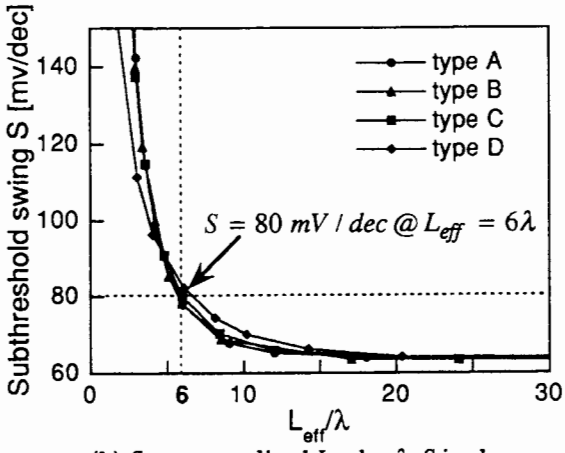



**Fig.3** The dependence of $S$ on $t_{fox}$ and $t_{box}$. To realize $S$ lower than 65 mV/dec, $t_{box}$ should be more than ten times as thick as $t_{fox}$.

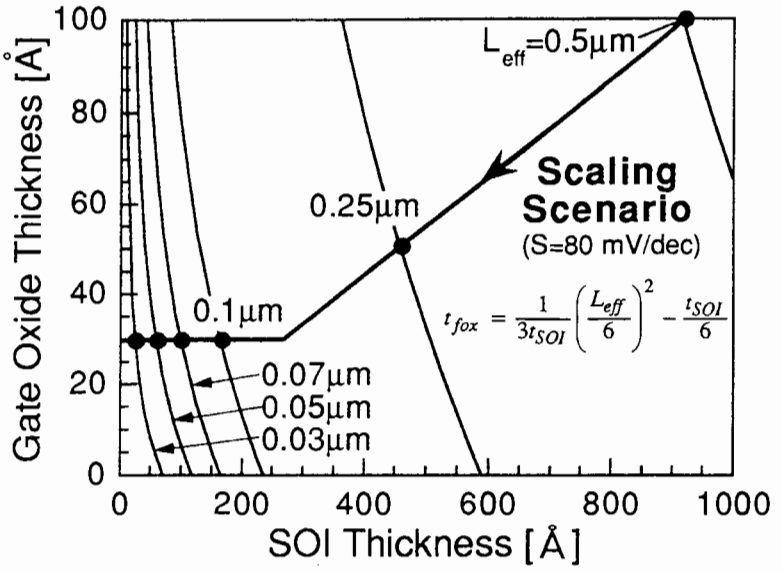



(a) $S$ vs. $L_{eff}$ of FD SOI MOSFETs shown in Table 1.

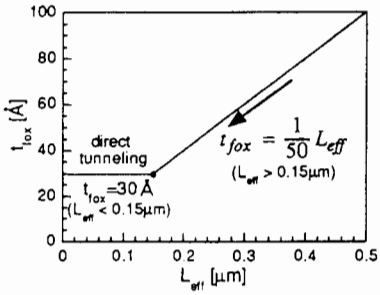



(b) $S$ vs. normalized $L_{eff}$ by λ. $S$ is always 80mV/dec when $L_{eff}$ = 6λ.

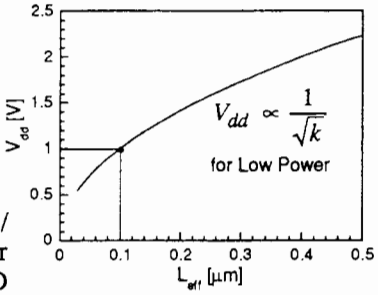
**Fig.4** Degradation of $S$ by the short channel effect.




(a) Scaling scenario of $t_{fox}$ and $t_{SOI}$. A criterion of SCE is set to $S$ = 80mV/dec (i.e. $L_{eff} = 6\lambda$). Each curve corresponds to $S$ = 80 mV/dec. In the lower left region of each curve, SCE can be suppressed in each generation. FD SOI MOSFETs can be scaled by thinning $t_{SOI}$ even if the $t_{fox}$ is constant.




(b) Scaling scenario of $t_{fox}$.




(c) Scaling scenario of $V_{dd}$.

**Fig.5** Scaling scenario of FD SOI MOSFETs to the deep sub-0.1μm regime.

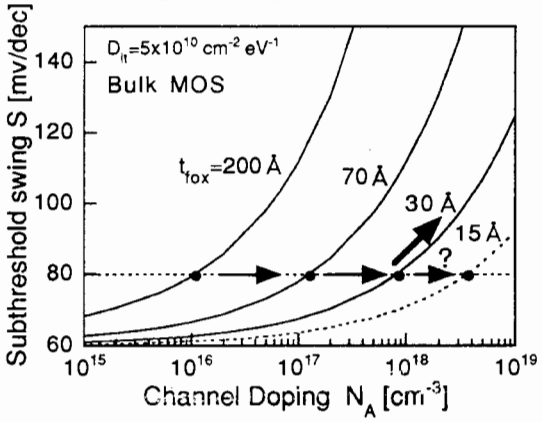



**Fig.6** $S$ vs. $N_A$ for long channel bulk MOSFETs. Increasing $N_A$ (i.e. decreasing the channel depletion width) degrades $S$ of long channel bulk MOSFETs when $t_{fox}$ is constant.

**Table.2** Device parameters of bulk MOSFETs below 0.1μm. $X_j$ equals to $t_{SOI}$ in Table.1.

| | type A' | type D' |
|---|---|---|
| $t_{fox}$ | 30Å | ← |
| $X_j$ | 162Å | 24Å |
| $N_A$ | 1×10$^{18}$ cm$^{-3}$ | ← |
| $V_{ds}$ | 1V | 0.55V |
| | 0.1μm Generation | 0.03μm Generation |

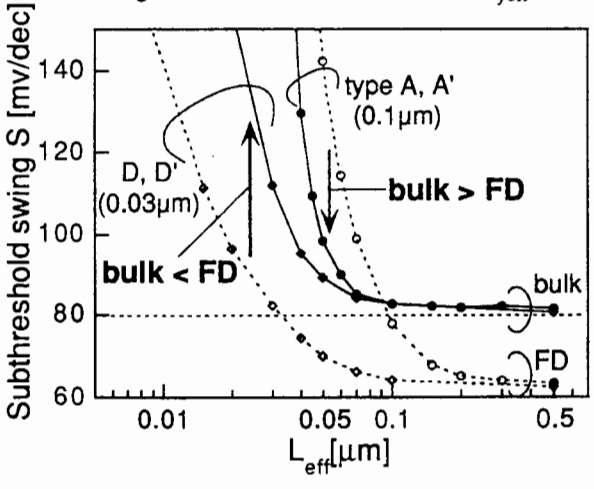



**Fig.7** $S$ vs. $L_{eff}$ of FD SOI and bulk MOSFETs shown in Table.1 and 2. In the 0.03 μm generation, bulk MOSFETs show worse SCE than FD SOI MOSFETs.

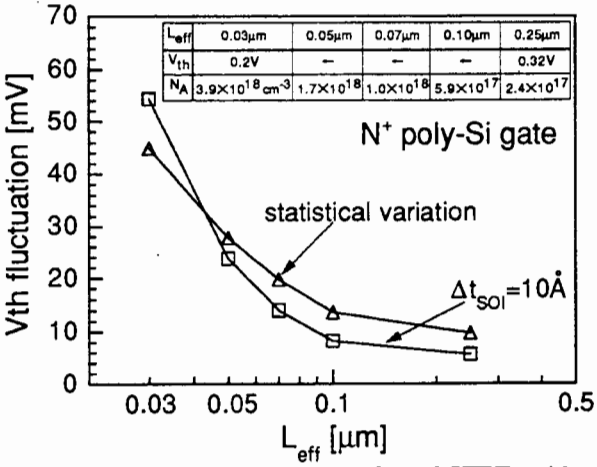



**Fig.8** *Vth* fluctuations of FD SOI MOSFETs with N$^+$ poly gate. The fluctiations are greatly reduced in the FD SOI MOSFETs with non-doped SOI and the mid-gap gate material.