Extended Abstracts of the 1998 International Conference on Solid State Devices and Materials, Hiroshima, 1998, pp. 322-323

Measurement of Energetic and Lateral Distribution of Interface State Density in FD SOI MOSFETs

Tran Ngoc Duyet*, Hiroki Ishikuro*, Yi Shi*, Takuya Saraya*, Makoto Takamiya* and Toshiro Hiramoto*,**

*Institute of Industrial Science, University of Tokyo, Minato-ku, Tokyo 106-8558, Japan

Phone/Fax: +81-3-5411-0695, E-mail: duyet@nano.iis.u-tokyo.ac.jp

**VLSI Design and Education Center, University of Tokyo, 113-8656, Japan

1. Introduction

The charge pumping (CP) [1-2] current in FD SOI MOSFETs, where the resistivity of the body region is generally high, tends to have a very large geometry-dependent component [3] resulting in the overestimation of interface state density (Dit). When the rise and fall times are relatively long, i.e. the measurement frequency is low, this undesirable component is negligible but the sensitivity is severely reduced. Therefore, the new method to suppress this effect and enhance the sensitivity is strongly required as the devices are scaled down. We have already developed a new measurement technique using the reverse pulse (RP) bias to suppress the geometric component in FD SOI MOSFET [4]. In this work, we extend this method and apply to the accurate measurement of energetic and lateral distribution of Dit in FD SOI MOSFET by the RP charge pumping method.

2. Device

The devices used in this study are fully-depleted SOI NMOSFETs as shown in Fig. 1. The thicknesses of the gate oxide, Si, and buried oxide films are 5 nm, 100 nm, and 98 nm, and the effective gate length and width are 2 μm and 20 μm, respectively. For source/drain and the main part of gate poly regions, phosphorus ions were implanted, while for the body contact, boron ions were used. It should be noted that boron ions were also implanted to the gate poly region near the body contact.

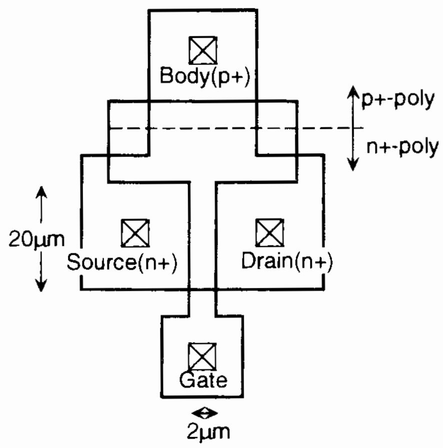

Fig. 1: Top view of the fabricated devices.

3. Geometric Component and Reverse Pulse Method

Fig. 2 shows the typical CP current (Icp) characteristics obtained in the variable amplitude mode with different rise and fall times (tr,tf). The observed two stepwise increases of Icp are the results of the two different n+ and p+ poly gate regions [4]. When tr and tf are 1 μs, no geometric component is observed and the Icp at the first step corresponds accurately to Dit. When tr decreases to 0.1 μs, the first step increases dramatically due to the additional geometric component resulting from the inefficiency of hole collection by the body contact. As shown in the figure, by applying the RP bias (Vp) to the body contact [4] only during the rise time, the geometric component by holes is completely suppressed even if tr is 0.1 μs. The geometric component by electrons, which is not observed in this sample, can be also suppressed by the RP bias to the source and drain only during the fall time. It is also found [4] that this method also avoid the reduction of the effective channel length which is observed in the dc body bias method [3].

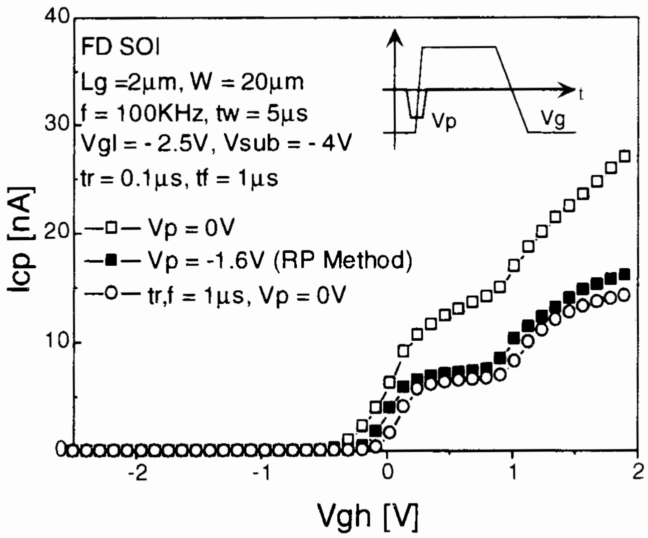

Fig. 2: CP current characteristics in the variable amplitude mode. The geometric component is completely suppressed when Vp = -1.6V. The inset shows the waveform of the gate voltage and the body bias.

4. Energetic distribution of interface state density

The energetic distribution of Dit is obtained from the dependence of Icp on tr and tf [2]. Fig. 3 shows the tr and tf dependence of Icp. When tf is 1 μs and tr is varied, Icp increases rapidly at tr = 0.1 μs due to the geometric component, indicating that the accurate energetic distribution can not be obtained. In the RP method, however, the geometric component is negligible and no increase in Icp is observed even at tr = 0.1 μs.

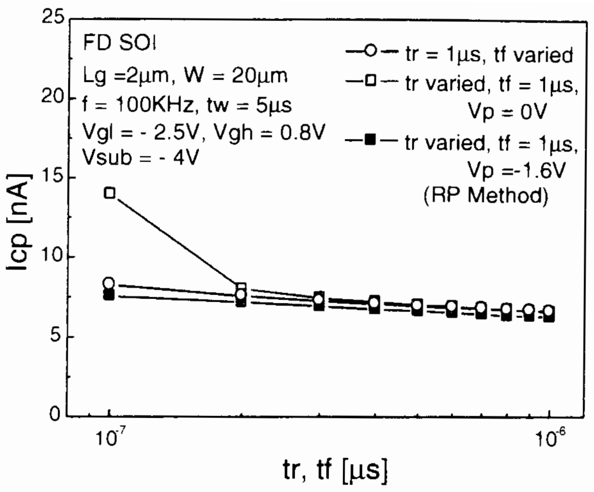

Fig. 3: Rise and fall time dependence of Icp. Accurate rise time dependence of Icp is obtained when applying to the body the reverse pulse bias Vp=-1.6V.

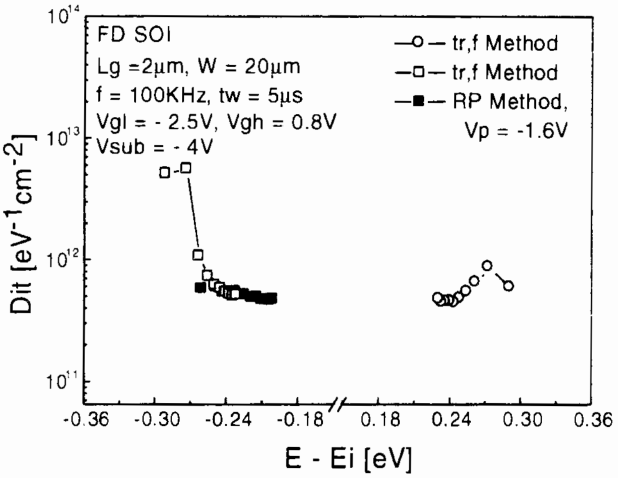

Fig. 4: Interface state density energetic distribution with and without the body reverse pulse bias.

Fig. 4 shows the energetic distribution of Dit obtained with and without the RP body bias. When the RP method is not used, the extracted Dit increases rapidly near the valence band edge (tr≦0.4μs). However, by applying to the RP bias Vp = -1.6V, an accurate Dit can be evaluated. It should be noted that due to the reverse bias at the rise time, the measurable energy range is shifted to the midst of the energy gap in the RP method as shown in the figure.

5. Lateral distribution of interface state density

The lateral Dit distribution is obtained by the expansion of the depletion regions near the source and drain by changing the DC reverse bias [5]. In the small DC bias and small tr, however, the geometric component leads to the overestimation of Dit. To avoid this effect, a new RP waveform is used, where the top level of the RP body bias is kept constant during the rise time and the base level of the RP bias is changed, as shown in the insert of Fig. 5. This waveform expands the depletion regions while suppressing geometric component. Therefore, the lateral Dit distribution can be accurately determined.

Fig. 5 shows the lateral profiles of Dit obtained by the DC reverse bias and the present RP bias methods. When tr and tf are 0.1μs in the DC method, the extracted Dit is dramatically overestimated due to the geometric component. In the RP method, however, the geometric component is not involved even when tr and tf are 0.1 μs. This method is sensitive with high frequency and can be applied to the scaled FD SOI MOSFETs.

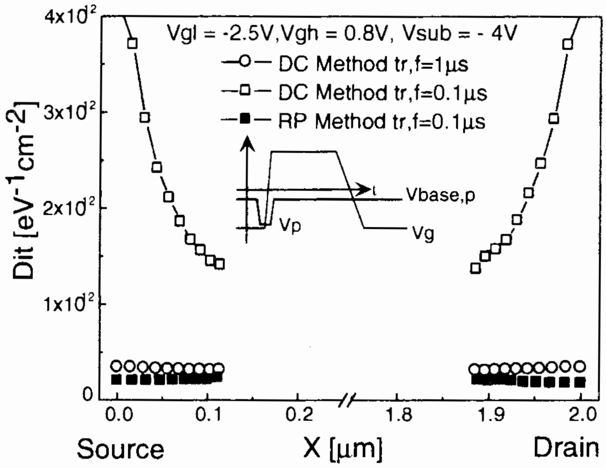

Fig. 5: Lateral distribution of interface state density using the DC and reverse pulse methods. An accurate estimation of Dit by the reverse pulse method is obtained even at a very short tr,f (0.1μs). The inset shows the waveform of the gate voltage and the body bias.

6. Conclusions

A new method for determining energetic and lateral distributions of the interface state densities is proposed. The main advantage is that it allows us to accurately measure the interface state properties in FD SOI MOSFETs where the geometric component often appears as a serious problem. The proposed method can be expected to be more powerful in scaled FD SOI devices, in which a high frequency CP pulse, consequently small rise and fall time must be used to reduce the signal/noise ratio.

References

[1] J.S. Brugler and P.G.A. Jespers: IEEE Trans. Electron Devices, **16** (1969) 297.

[2] G. Groeseneken, H.E. Maes, N. Beltran and R.F. De Keersmaecker: IEEE Trans. Electron Devices, **31** (1984) 42.

[3] Y. Li and T.P. Ma: Int. Symp. on VLSI Tech., Syst. and Appl., p.144, (1995).

[4] T.N. Duyet, H. Ishikuro, M. Takamiya, M. Saraya and T. Hiramoto: Jpn. J. Appl. Phys. (to be submitted).

[5] P. Heremans, J. Witters, G. Groeseneken and H.E. Maes: IEEE Trans. Electron Devices, **36** (1989) 1318.