High Performance Electrically Induced Body Dynamic Threshold SOI MOSFET (EIB-DTMOS) with Large Body Effect and Low Threshold Voltage

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Abstract

A novel Electrically Induced Body DTMOS (EIB-DTMOS) is proposed where the body is electrically induced by substrate bias and its high performance is demonstrated by experiments and simulations. EIB-DTMOS achieves the large body effect and low V_{th} at the same time. Among several DTMOS's, the accumulation mode EIB-DTMOS shows the highest current drive at fixed off-current due to the large V_{th} shift and the suppressed short channel effect.

Introduction

The top priority in low power device design is a high current drive at very low supply voltage (V_{dd} < 0.5 V). The dynamic threshold SOI MOSFET (DTMOS) has an ideal subthreshold slope and a high current drive [1]. To enhance the current drive of DTMOS, a large body effect is essential, because DTMOS operating at V_{dd} effectively operates at V_{dd} $+\Delta V_{th}$, where ΔV_{th} is the V_{th} shift due to the body effect obtained by connecting gate to body [2]. However, it is very hard to attain a large body effect factor ($\gamma \equiv \Delta V_{th} / \Delta V_{bs}$) at low V_{th}, because γ is primarily determined by the ratio of gate oxide thickness to channel depletion layer width (W_d) which is reduced by high channel doping concentration. The previously reported DTMOS's [1,3-5] have small γ due to low V_{th} and do not take full advantage of high current drive inherent to DTMOS. In this study, we propose a novel Electrically Induced Body DTMOS (EIB-DTMOS) which achieves large γ and low V_{th} at the same time. Thin SOI layer thickness provides very large γ, while V_{th} is determined by impurity concentration in the SOI layer. Experimental and simulation results demonstrate the superiority of EIB-DTMOS to conventional DTMOS and normal SOI MOSFETs. γ is as high as 0.8 - 1 and V_{th} can be set to around 0.1 V.

Device Structure

Fig. 1 shows schematic cross-sections of the proposed EIB-DTMOS in an inversion mode and an accumulation mode. The body region is electrically induced (accumulated in the inversion mode and inverted in the accumulation mode) by a static substrate bias at the back-interface in the SOI layer. The gate is tied to this electrically induced body via a body contact terminal. The back gates below buried oxide are fabricated by ion implantation through buried oxide [6,7]. In EIB-DTMOS, the channel depletion layer width (W_d) equals to the SOI thickness. Therefore, by thinning the SOI thickness, EIB-DTMOS can reduce W_d and realize larger γ and thus, higher current drive than the conventional DTMOS. Reduced W_d also leads to suppressed short channel effect.

Experimental

The inversion mode EIB-MOSFET is compared with conventional fully depleted (FD) and partially depleted (PD) SOI MOSFETs by experiment. The devices measured are fully depleted SOI nMOSFETs fabricated on a SIMOX wafer [8]. Thicknesses of the gate oxide, SOI, and buried oxide are 10 nm, 40 nm, and 100 nm, respectively. The SOI layer is p-type with concentration in the order of 10^{16} cm^{-3}. A MOSFET is measured in three different modes (FD, PD, and EIB-DTMOS) by changing the bias conditions shown in Table I. Fig. 2 shows subthreshold characteristics in the three modes. EIB-DTMOS has the ideal subthreshold slope, and γ is as high as 0.8 resulting from thin SOI thickness which corresponds to W_d. Fig. 3 shows V_{th} rolloff and subthreshold slope degradation by the short channel effect (SCE). EIB-DTMOS suppresses SCE very well, because drain depletion layer width is reduced by the forward body bias in DTMOS. In Fig. 4, on/off characteristics are compared. EIB-DTMOS shows high current drive and low off-current due to high γ and steep subthreshold slope. These experimental results show EIB-DTMOS is superior to conventional FD and PD SOI MOSFETs.

Comparison with other DTMOS

In order to demonstrate advantages of EIB-DTMOS, four types of DTMOS shown in Fig. 5 are compared by device simulation [9]. Type-A is a conventional DTMOS [1, 3-5] and type-C is a counter doped DTMOS [2,10]. Type-B and D are the inversion mode and accumulation mode EIB-DTMOS, respectively. Channel profiles of type-C and D can be realized by Sb ion implantation [11].

A. Inversion mode EIB-DTMOS

Fig. 6 shows the dependence of V_{th} on γ for type-A and B. γ of type-B has two times as large as that of type-A at fixed V_{th} [12], because W_d of type-B is half of that of type-A, which is shown analytically. The experimental result (V_{th} =0.45 V, γ= 0.8) in the previous section is also plotted, which fits the simulation very well. However, V_{th} of the experimental result is too high for supply voltage below 0.5 V. The decrease in V_{th} leads to the decrease in γ as shown in the Fig. 6. In the inversion mode EIB-DTMOS, therefore, the large γ and low V_{th} are not attained at the same time.

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B. Accumulation mode EIB-DTMOS

To realize both large γ and low V_{th}, the accumulation mode device (type-D) is required. In type-D, the body region is formed by electrically inverted carriers and W_d is limited by thin SOI thickness. The carrier concentration of the body (holes for nMOS) could be very high and a very steep carrier profile is achieved. On the other hand, the conventional counterpart of type-D is a counter doped DTMOS (type-C), where not only the counter doped region but the body region is formed by the doping. Therefore, the body concentration is limited and it is very difficult to obtain a steep carrier profile. γ of type-C and D are also plotted in Fig.6. Type-D has much higher γ due to the thin SOI layer and steeper carrier profile.

C. Body resistance

Body RC delay is a serious problem in DTMOS with wide gate width (W_g), because body potential doesn't follow the gate voltage and differs in the gate width direction in AC operation [3,5,13]. EIB-DTMOS also has the serious body RC delay. Body capacitance of EIB-DTMOS (type-B, D) is much lower than that of the conventional DTMOS (type-A, C), because p-n junction area is very small. However, EIB-DTMOS has higher body resistance (10~100 kΩ/□) than the conventional DTMOS (5~50 kΩ/□) and bulk DTMOS (1~10 kΩ/□) [5], because the body is electrically induced only at SOI/buried oxide interface. Fig. 7 shows the channel donor concentration (N_{D4}) dependence of front V_{th}, back V_{th}, γ, and body sheet resistance in the accumulation mode EIB-DTMOS (type-D). By increasing N_{D4}, front V_{th} is lowered and γ is increased due to thinning of the effective SOI thickness, which results in higher current drive. However, high N_{D4} also leads to increased body resistance, because back V_{th} is also lowered and the back-interface is not sufficiently inverted at a given negative substrate bias. To decrease the body resistance, higher substrate bias is needed but causes a reliability problem in buried oxide (E_{box} > 5 MV/cm) as shown in Fig. 7 (b). A low/high/low channel profile alleviates the problem. A DTMOS divided into n narrow MOSFETs with respective body contacts is also effective, because body resistance is proportional to n^{-2}. The effect of body resistance on the AC performance will be discussed later.

D. Performance

Fig. 8 shows V_{th} rolloff and S degradation of type-A, B, C, and D with V_{th} of 0.12 V at L_g = 0.5 μm. SCE of type-D is the smallest. Fig. 9 shows on/off characteristics of the four types. Although the on-current for the four type is almost the same at fixed L_g, type-D shows three decades less off-current than type-A at L_g = 0.07 μm due to suppressed SCE. Fig. 10 shows on/off characteristics of type-A, C, and D with the same off-current at L_g =0.07 μm. Type-D shows one and a half times as high on-current as type-A due to large γ in spite of much less DIBL in type-D as shown in the inset of Fig. 10. These results indicate that type-D has better performance than any other DTMOS at any conditions.

Fig. 11 shows forward bias p-n junction current of type-A, B, C, and D. Type-D shows the smallest leakage current due to very small junction area and high hole concentration. When the SOI thickness is thinned below 10 nm in EIB-DTMOS to scale down L_g, leakage current will increase due to direct tunneling between electrons at the front interface and holes at the back interface [14].

Finally, we compare AC characteristics of type-C, and D by mixed-mode simulations. Fig. 12 shows the dependence of the inverter delay on wire capacitance. Type-D is faster than type-C, because type-D has higher current drive and lower junction capacitance. In Fig. 12, the effect of the body resistance is negligible because W_g is narrow. When W_g is wider, the body RC delay becomes comparable to the gate delay and the body potential does not follow the gate voltage, resulting in slower propagation delay. When W_g is much wider and body RC delay is much longer, the body potential will strongly depend on history of the input and output voltages and vary between 0 V and V_{dd}. In such a case, history dependent propagation delay and large power consumption due to low V_{th} would be expected.

Conclusions

We have proposed the high performance EIB-DTMOS with large body effect and low V_{th}. Electrically induced body with high carrier concentration at back interface and thin SOI layer reduces the channel depletion layer width and maximizes the body effect. Among several DTMOS's, the accumulation mode EIB-DTMOS shows the highest current drive at fixed off-current due to the large V_{th} shift and the suppressed short channel effect.

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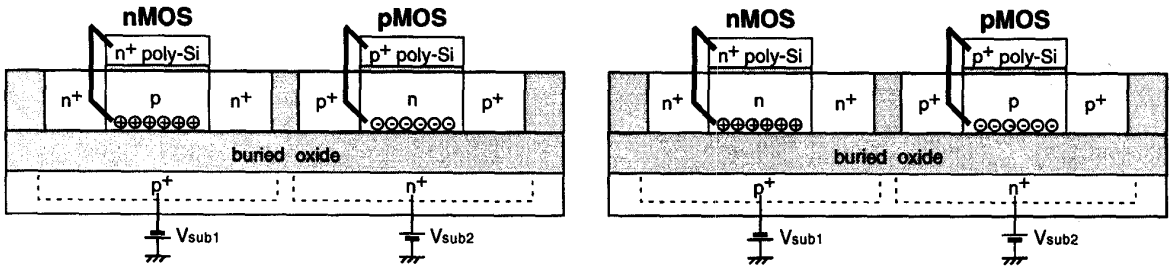


(a)Inversion mode EIB-DTMOS (b)Accumulation mode EIB-DTMOS

Fig. 1 Schematic cross-sections of the proposed EIB-DTMOS. The gate electrode is connected to the body. (a) The inversion mode EIB-DTMOS, where the body region is electrically induced (accumulated) by substrate bias. (b) The accumulation mode EIB-DTMOS, where the body region is electrically induced (inverted) by substrate bias. The accumulation mode EIB-DTMOS achieves both large γ and low V_{th}.

Table I Three operation modes of a SOI nMOSFET measured. When V_{bs}=0V and V_{sub}=0V, the device operates as a fully-depleted (FD) mode. When V_{bs}=0V and V_{sub}= -20V, holes are induced at the back-interface and it operates as a partially-depleted (PD) mode. When gate is tied to body (V_{bs}=V_{gs}) and V_{sub}= -20V, gate is connected to the electrically induced holes at the back-interface and it operates as the inversion mode EIB-DTMOS.

operation mode	V_{bs}	V_{sub}
FD SOI MOSFET	0V	0V
PD SOI MOSFET	0V	-20V
EIB-DTMOS	$=V_{gs}$	-20V

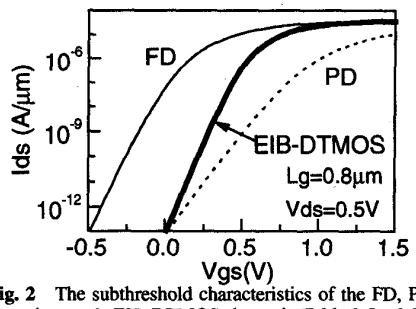
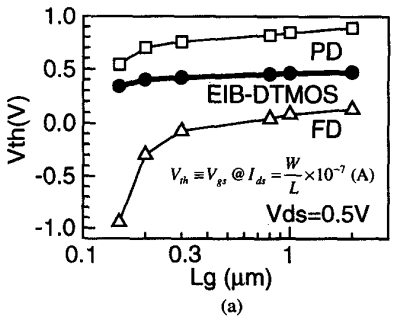


Fig. 2 The subthreshold characteristics of the FD, PD, and inversion mode EIB-DTMOS shown in Table I. L_g=0.8μm.



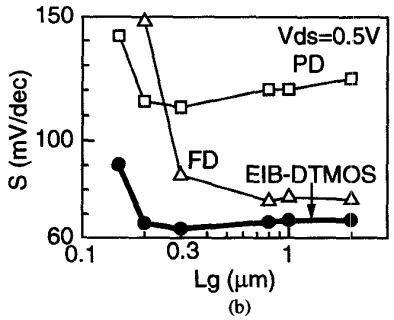


Fig. 3 (a) The dependence of V_{th} on L_g. (b) The dependence of subthreshold slope on L_g. EIB-DTMOS has the ideal subthreshold slope and suppresses the short channel effect well. The definition of V_{th} is shown in the inset.

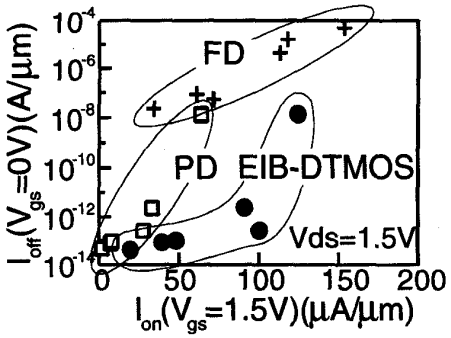
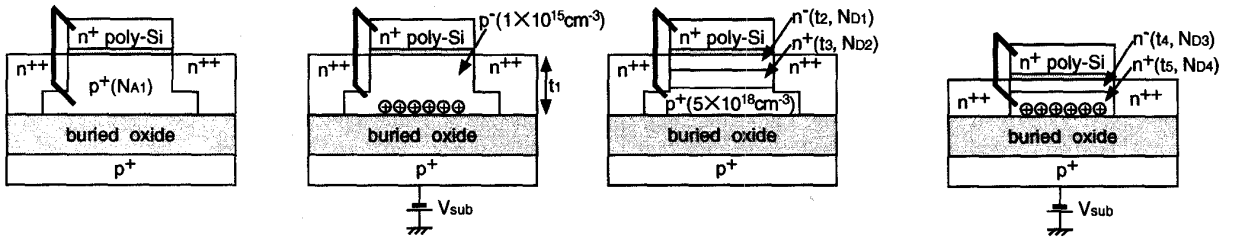


Fig. 4 The on/off characteristics of the FD, PD, and EIB-DTMOS. L_g is varied. EIB-DTMOS shows the high current drive and low off-current, while FD shows large off-current and PD shows the poor current drive.



(a) Type-A (Conventional DTMOS) (b) Type-B (Inversion mode EIB-DTMOS) (c) Type-C (Counter Doped DTMOS) (d) Type-D (Accumulation mode EIB-DTMOS)

Fig. 5 Four types of DTMOS compared in this study. Type-A is a conventional DTMOS [1, 3-5] and type C is a counter doped DTMOS [2,10]. Type-B and D are the proposed EIB-DTMOS in the inversion mode and accumulation mode, respectively. Type-D with large γ and low V_{th} achieves the highest current drive. Gate oxide thickness is 3nm, buried oxide thickness is 20nm, and supply voltage is 0.5V in all cases. The junction depth of extension is 15nm, and the SOI thickness for type-D is also 15nm. Surface concentration of type-C and D is low to avoid the impurity scattering. The substrate voltage (V_{sub}) is -12V for type-B and D. t_2=t_4=5nm, t_5=10nm, N_{D1}=N_{D3}=1x10^{17}cm^{-3}, N_{D2}=5x10^{18}cm^{-3}, N_{D4}=1x10^{19}cm^{-3}. N_{A1}, t_1, and t_3 are varied.

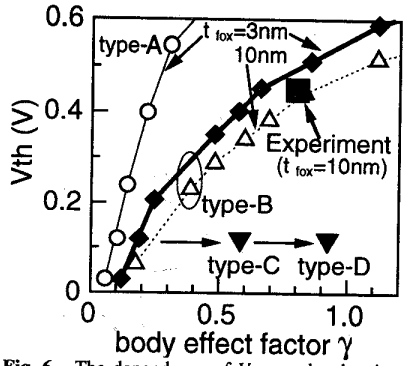
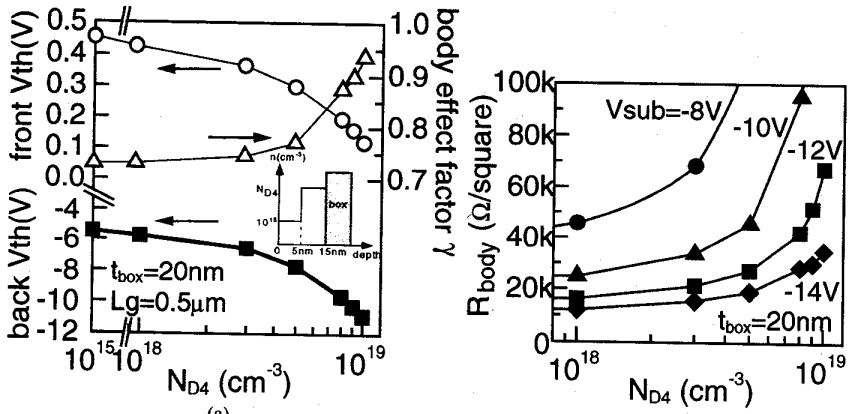
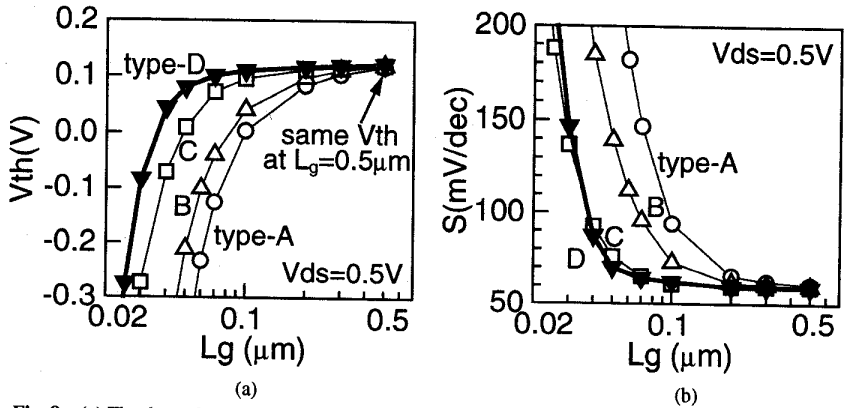


Fig. 6 The dependence of V_{th} on γ by the simulations for type-A and B. Experimental data is also plotted. They fit very well. γ of type-B has two times as large as that of type-A at fixed V_{th}. To vary V_{th} and γ, N_{A1} is changed for type-A and t_1 is changed for type-B. γ of type-C and D in Figs. 8-9 are also plotted.



(a) (b)

Fig. 7 (a) N_{D4} dependence of front V_{th}, back V_{th}, and γ in type-D. (b) N_{D4} dependence of body sheet resistance in type-D. As N_{D4} increases, low front V_{th} and large γ are obtained. However, body resistance increases due to low back V_{th}. To decrease the body resistance, high V_{sub} is required.



(a) (b)

Fig. 8 (a) The dependence of V_{th} on L_g, and (b) the dependence of subthreshold slope on L_g for type-A, B, C, and D, which have V_{th} of 0.12V at L_g=0.5μm. Type-D suppresses SCE very well. Device parameters are N_{A1}=3.1x10^{16}cm^{-3}, t_1=89nm, and t_3=8.7nm.

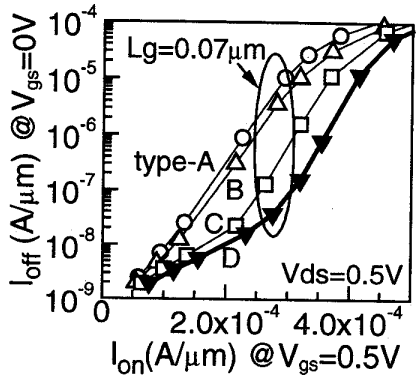


Fig. 9 The on/off characteristics of type-A, B, C, and D. L_g is varied. V_{th} is set to 0.12V at L_g=0.5μm. At L_g =0.07μm, type-D shows three decades less off-current than type-A due to the suppressed SCE, while the on-current is almost the same. Device parameters are the same as Fig. 8.

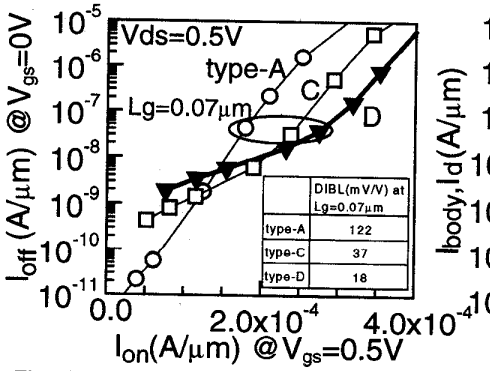


Fig. 10 The on/off characteristics of type-A, C, and D with the same off-current at L_g=0.07μm. L_g is varied. Type-D shows one and a half times as high on-current as type-A due to the large γ in spite of much less DIBL in type-D shown in the inset. N_{A1}=2x10^{17}cm^{-3}, and t_3=8nm.

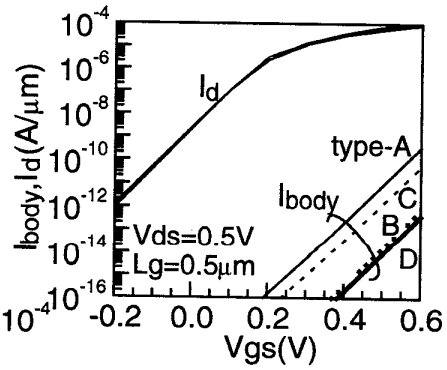


Fig. 11 The body current characteristics of type-A, B, C, and D. Drain current is also shown for comparison. Type-D has the smallest leakage current due to very small junction area and high hole concentration.

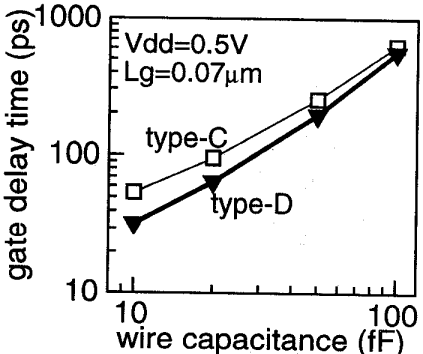


Fig. 12 The dependence of the inverter delay of type-C, and D with the same off-current on wire capacitance. Type-D is faster than type-C, because type-D has higher current drive and lower junction capacitance. L_n/W_n=0.07μm/0.5μm for nMOS, and L_p/W_p=0.07μm/1μm for pMOS. Device parameters are the same as Fig. 10.