Jpn. J. Appl. Phys. Vol. 37 (1998) pp. L 855–L 858
Part 2, No. 7B, 15 July 1998

Suppression of Geometric Component of Charge Pumping Current in Thin Film Silicon on Insulator Metal-Oxide-Semiconductor Field-Effect Transistors

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(Received April 14, 1998; accepted for publication May 27, 1998)

A new reverse pulse method is proposed for precise measurement of charge pumping current in silicon on insulator metal-oxide-semiconductor field-effect transistors (SOI MOSFETs), where the reverse pulse voltage is applied to the body only at the gate voltage rise time. The majority carries of the high resistive body region can be completely removed by applying the reverse pulse to the body. Therefore, the undesirable, geometry-dependent component which causes imprecise measurement of the interface trap density on SOI MOSFETs is suppressed. This method also suppresses the reduction of effective channel length which takes place when using a DC reverse bias. It is demonstrated that the accurate measurements of the interface density on SOI MOSFETs are possible.

KEYWORDS: SOI MOSFET, charge pumping, geometric component, effective channel length, DC reverse bias, pulse reverse bias

1. Introduction

Charge pumping (CP)[1,2] is a very sensitive method for the characterization of low concentrations of interface states ($10^9\,\mathrm{cm^{-2}\,eV^{-1}}$) in short-channel metal-oxide-semiconductor (MOS) devices. The principle of the conventional CP method[3,4] is to repeatedly switch the gate from accumulation to inversion and vice versa, while keeping the source, drain and body contacts grounded or slightly reverse biased. During accumulation, some of the majority carriers provided by the body are trapped on the interface states. During the rising edge of the gate pulse, the mobile majority carriers are collected rapidly from the accumulation layer by the body, and then the trapped majority carriers recombine with the minority carriers provided by the source and drain. Similarly, during the falling edge of the gate pulse, when the gate surface is pulsed from inversion to accumulation, the trapped minority carriers recombine with majority carriers. These recombination processes give rise to a dc charge-pumping current (I_{cp}) in the body (of the same magnitude as an opposite-sign current flowing through the source and drain contacts), which is a frequency-amplified measurement of the density of interface states. A major problem of the CP measurement on MOSFETs is the so-called "geometric component" of the CP current,[1,4] which occurs if all mobile carriers of one type, majority carriers during the rise and minority ones during the fall of the gate pulse, are not removed rapidly enough before the arrival of the other type of carrier. The carriers that are left behind will recombine with carriers of the other type and therefore an additional component of CP current that does not involve the interface states arises. This undesirable parasitic component of I_{cp} is responsible for an unacceptable overestimation of interface state density.

In SOI MOSFETs, particularly in thin film SOI devices, where the resistivity of the body region is comparatively high, this parasitic recombination tends to occur more often, disrupting information from the interface . The geometric component can be suppressed using the reverse bias method.[5] However, using this method, the effective channel length is also undesirably reduced, therefore the imprecise results of the CP current and consequently, an underestimation of the interface state density might be mistakenly obtained. In this paper, we present a new method to suppress both the parasitic geometric effects and the reduction of the effective channel length.

2. Experimental

The devices used in this study are fully-depleted SOI NMOSFETS fabricated on SIMOX wafers with n^+ polysilicon gate. Figure 1 shows the top view of the fabricated devices. The Si film thickness is 100 nm and the average doping concentration of the body is $\bar{N} = 10^{17}\,\mathrm{cm^{-3}}$. The thicknesses of the gate oxide and buried oxide are 5 nm and 98 nm, respectively. For source, drain and the main part of gate polysilicon regions phosphorus was implanted at 25 keV at a dose of 10^{15} $\mathrm{cm^{-2}}$, while for the body contact, boron ions were implanted at 110 keV with a dose of 10^{15} $\mathrm{cm^{-2}}$. It should be noted that boron ions were also implanted to the gate poly region near the body contact. Therefore, the gate poly has both n^+ and p^+ regions. The effective gate width is $W = 20\,\mu$m whereas the gate length is $L_{\mathrm{g}} = 5\,\mu$m.

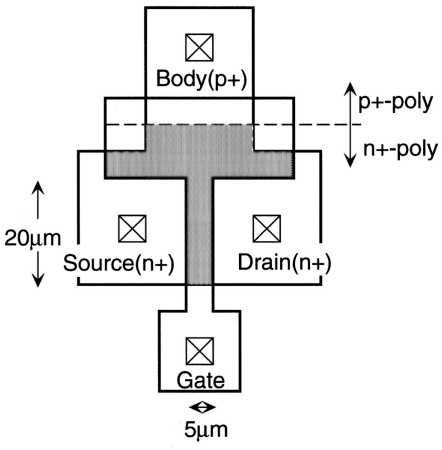

Fig. 1. Top view of the fabricated SOI devices.

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The experimental setup for the new charge pumping measurements on SOI MOSFETs is shown in Fig. 2. The gate of a MOS transistor is connected to a pulse generator, and a DC reverse bias or pulse reverse bias is applied to the body while the current flowing through the source and drain contacts is measured.

3. Results and Discussion

Figure 3 shows the results obtained from the variable amplitude CP method, in which the base level of the pulse, V_{GL}, is fixed while the CP current is measured as a function of the amplitude (i. e. V_{GH}-V_{GL}) by varying V_{GH}. A strong dependence on the rise/fall time (t_r, t_f) can be clearly observed. The measured CP current at the long rise and fall time $t_r = 1\mu$s, $t_f = 1\mu$s is considered as reference data where the minimum distribution of the geometric component is adjusted.

Two stepwise increases in the CP current are observed. Tseng *et al.* also reported the similar results and attributed the second stepwise increase to interface states at the edges.[6)]

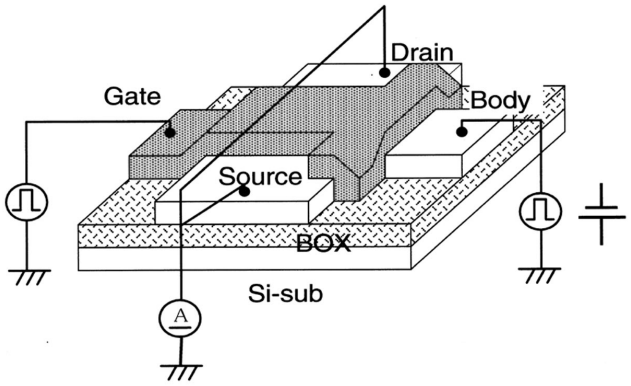

Fig. 2. Experimental setup for charge pumping measurement on SOI MOSFETs.

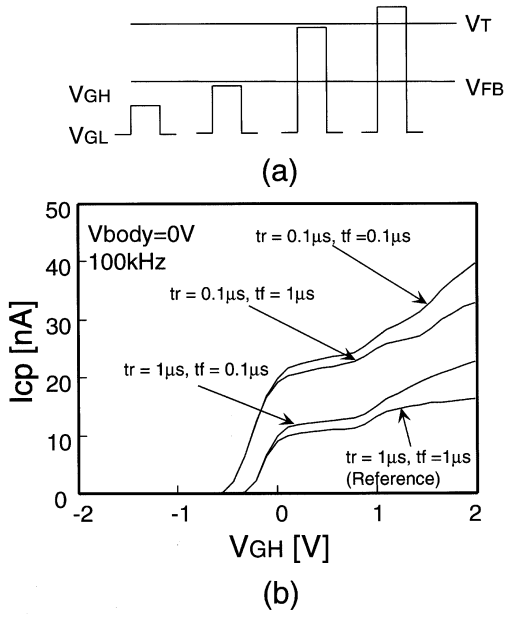

Fig. 3. (a) Illustration of applied voltage in the variable amplitude CP method. (b) Charge pumping current as a function of the top level of the gate pulse. Rise and fall times are changed. Reference data do not have any geometric component.

In our data, however, the ratio of the magnitudes of the CP currents and the difference of the gate voltages V_{GH} at which these currents start to increase are around 1:3 and 1 V, respectively, being nearly equal to the ratio of the areas and the difference of the work functions of the n^+ and p+ polysilicon gate regions. It is concluded, therefore, that the second stepwise increase is due to the influence of the p^+ polysilicon and not to edge effects. The influence of this p+ polysilicon region does not affect the results discussed in this paper. The CP current at the rise and fall times $t_r = 1\mu$s, $t_f = 0.1\mu$s is not significantly different from that in the reference data. A small difference of these CP currents can be understood as the change of energy windows which can be scanned by the gate pulses at different fall times. The channel length ($L_g = 5\,\mu$m) is short enough to allow the mobile electrons to flow back to the source and drain contacts before the accumulation layer is formed. The measured CP current here is attributed to the interface state recombination, and does not involve bulk recombination. From these results, it can be simply concluded that in SOI NMOS devices where $L_g = 5\,\mu$m, the mobile electrons do not play an important role in inducing the geometric current at least at a fall time $t_f = 0.1\,\mu$s.

However, one can easily see from this figure, as the rise time decreases to $t_r = 0.1\,\mu$s, the CP current increases dramatically. The origin of this overshoot current was originally explained in ref. 5. During rise time, the gate surface goes from accumulation to inversion. Electrons come from the source and drain while holes in the channel are forced to leave and are collected by the body contact. In SOI devices, however, since body contact is only on one side of the device resulting in the relatively high resistivity of the body region, some of the holes do not have enough time to travel through the entire channel width (20 μm in this case) before the electrons rush in, and these holes may recombine with the incoming electrons before they are collected. This parasitic recombination is added to the interface-state-based CP current, therefore, the overvalued CP current is experimentally observed for the short rise time. The major cause of this undesirable added component is believed to be the result of the inefficiency of the body contact to collect carriers. An illustration of the mobile carriers in the channel during rise and fall time t_r, t_f is shown in Fig. 4.

To control this extremely unfavorable component, the DC reverse method[5)] has been proposed where a DC reverse bias is applied to the body as shown in Fig. 5. Compared to the reference data at the long rise and fall time ($t_r = 1\,\mu$s, $t_f = 1\,\mu$s) where the CP current is assumed to not have a geometric component, the recombined I_{cp} at $t_r = 0.1\,\mu$s, $t_f = 1\,\mu$s and $V_{body} = 0$ V is comparatively high due to the added geometric component. The geometric component significantly decreases with an increase in the DC reverse bias. The result with the body contact voltage, $V_{body} = -0.5$ V, shows practically no geometric component in I_{cp} at a rise time as short as 0.1 μs. However, as the applied body bias continues to slightly increase, the CP current steeply decreases due to the effect of shortening of the effective channel length resulting from an expansion of the depletion regions surrounding the source and drain. The difference between the curves at $V_{body} = -0.5$ V and -0.6 V shows that it is extremely difficult to determine a suitable reverse voltage in the DC body method in order to suppress the geometric component with-

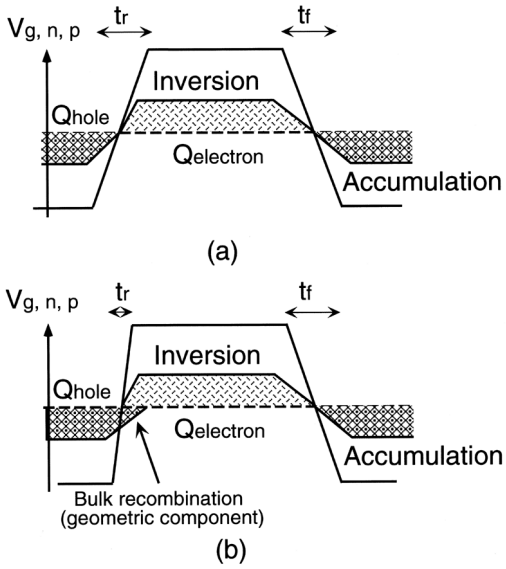

Fig. 4. Illustration of mobile carriers in the channel during rise and fall times (t_r, t_f) of the gate pulse. The vertical axis shows gate voltage, electron and hole concentrations. (a) Electrons and holes have enough time to flow back to source, drain and body contacts, respectively (rise and fall times $t_r = 1\,\mu$s, $t_f = 0.1$ and $1\,\mu$s). (b) Holes are not removed rapidly enough before the arrivals of electrons (rise time $t_r = 0.1\,\mu$s). The remaining holes recombine with the incoming electrons, resulting in parasitic recombination current.

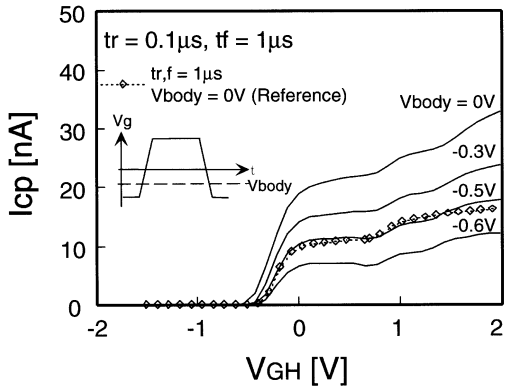

Fig. 5. DC body bias dependence of the charge pumping current.

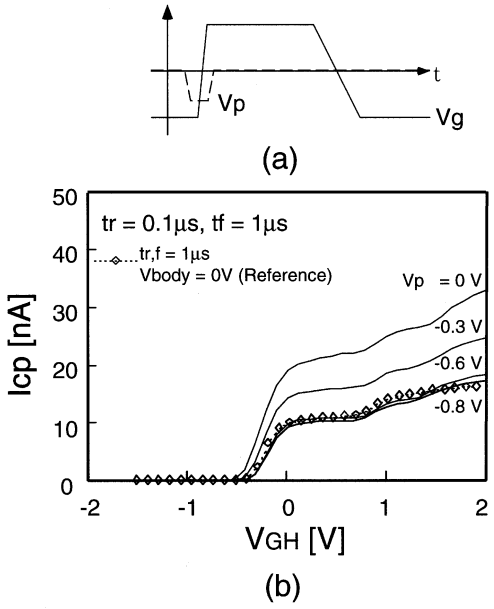

Fig. 6. The reverse pulse method: (a) The waveforms of the pulses applied to the gate and body contacts. (b) Body pulse top level dependence of the charge pumping current.

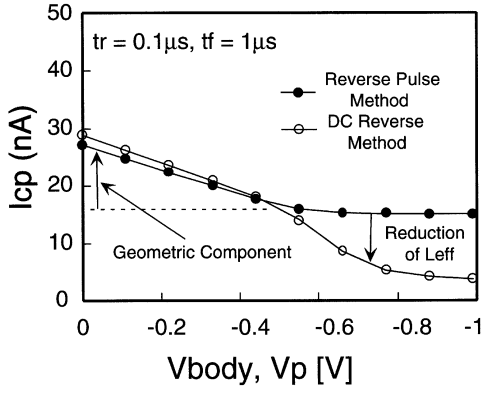

Fig. 7. Charge pumping current as a function of DC body bias V_{body} and body pulse top level V_p: The DC reverse and pulse reverse methods are compared. The horizontal axis is V_{body} for the DC reverse method and V_p for the reverse pulse method.

out the effect of shortening of the channel length and it is also expected that this shortening effect of the channel length will become even more significant as the devices are scaled down.

Since the geometric component is caused by the holes not having enough time to flow back to the body contact only during the rise time of the gate voltage, the reverse pulse bias is applied on the body contact only at the rise time to improve the situation in the proposed reverse pulse method. The waveforms of the pulse voltages applied to the gate and the body contacts used in the reverse pulse method are shown in Fig. 6(a). The body pulse bias is 'ON' only at the rise edge of the gate pulse and 'OFF' at all the rest of it. It is clear that the body pulse bias does not influence the device when the gate surface is accumulated and inverted. As can be seen from Fig. 6(b) where the body pulse top level dependence of the CP current is displayed, an increase in the top level V_p leads to a marked decline in the geometric current. When the top level $V_p = -0.6\,$V, the result shows the same effect in restraining the geometric component as when using the DC reverse bias at $V_{body} = -0.5\,$V. In addition, even when increasing the top level to $V_p = -0.8$V, the CP current does not decrease, remaining nearly constant as indicated in the reference data. It is obvious that the reverse pulse bias does not affect the effective channel length.

The comparison of both methods is illustrated in Fig. 7 where the recombined I_{cp} is plotted as a function of the DC reverse voltage V_{body} and the top level of the pulse bias V_p. The horizontal axis is V_{body} for the DC reverse method and V_p for the reverse pulse method. When V_{body} and V_p are 0 V, the large geometric component is observed. As V_{body} and V_p increase, both methods effectively suppress the geometric component until -0.5 V. However, when V_{body} and V_p exceed -0.5 V, the measured CP current using the DC reverse method decreases sharply due to the reduction of effective channel

length L_{eff} while that of the proposed reverse pulse method levels off. The results in Fig. 7 reveal that by using the reverse pulse method, one can not only suppress the geometric component in the CP current, but also avoid the effect of shortening of the channel length.

The reverse pulse method can be similarly used by applying the pulse bias to the source and drain contacts of the devices where mobile minority carriers (electrons for NMOS) are a major cause of the parasitic geometric current.

4. Conclusions

A new reverse pulse method to suppress the geometric component in the CP current in thin film SOI MOSFETs has been developed. Since the reverse pulse bias is applied to the body contact only at the rise time of the gate pulse, the electrical parameters of the device are not affected during the interface state recombination process (accumulation and inversion of the gate surface). The reverse pulse method shows an advantage over the DC reverse method in that it does not cause an undesirable effect from shortening of the channel length. Therefore, precisely measured CP current and consequently, an accurate evaluated interface state density of the devices can be obtained. This new method is also expected to be more powerful in scaled MOS devices where a slight reduction in the effective channel may lead to a significant decrease in the charge pumping current.

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