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FABRICATION OF GATE-ALL-AROUND MOSFET BY SILICON ANISOTROPIC ETCHING TECHNIQUE

TOSHIKAZU MUKAIYAMA[1], KEN-ICHI SAITO[1], HIROKI ISHIKURO[1], MAKOTO TAKAMIYA[1], TAKUYA SARAYA[1] and TOSHIRO HIRAMOTO[1,2]

[1]Institute of Industrial Science, University of Tokyo, 7-22-1 Roppongi, Minato-ku, Tokyo 106, Japan
[2]VLSI Design and Education Center, University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113, Japan

Abstract—A novel fabrication process of gate-all-around (GAA) MOSFETs using an anisotropic etching technique has been proposed. In this technology, the channel width of the GAA device is not limited by the lithography resolution and the density of the wire channel is doubled. The two-dimensional device simulation shows much better short channel immunity of GAA devices than that of single gate and double gate SOI MOSFETs. The simulation also shows that the new GAA devices we have proposed have higher current drivability than the conventional GAA and single gate SOI devices.

1. INTRODUCTION

As the channel length of MOS device decreases, the short channel effect becomes one of the serious problems. Single gate SOI[1] and double gate SOI MOSFETs[2] have been proposed for future short channel LSI devices. Gate-all-around (GAA) MOSFETs are also one of the candidates for scaled MOSFETs[3]. Figure 1 summarizes the structures of these devices. The single gate SOI MOSFET has the gate electrode at the top of the channel, while the double gate SOI MOSFET has the gate not only at the top but also at the bottom of the channel. In the GAA devices, on the other hand, the channel region is completely surrounded by the gate electrode. The channel potential is completely controlled by the gate and, therefore, much better immunity to the short channel effect is expected.

The GAA device has been studied as quantum effect devices due to the excellent 1D electron confinement[3,4]. The applications of the GAA device for VLSI MOSFETs have also been intensively studied for high short channel immunity[1,2,5,6]. The disadvantage of the GAA device for VLSI MOSFET is the small drain current drivability, because the wire channel width is very narrow. To overcome the problem of small drain current, wire channels are usually arranged in parallel as shown in Fig. 2. However, the density of the wire channels are limited by the lithography resolution and result in the insufficient current drivability. Therefore, it is strongly required to increase the wire channel density for high drain current.

In this paper, we propose a new fabrication technique of GAA devices, where the density of the wire channel is greatly increased. The fabrication process of the silicon wire using anisotropic etching and selective oxidation[7,8] has been applied to the GAA devices. The wire channel density is twice as high as that of the conventional silicon wire process. Therefore, the high density arrangement of wires can be accomplished. Two dimensional device simulation confirms a better short channel immunity and high drain current of the new GAA device than those of the double gate and single gate SOI devices.

2. GAA DEVICE FABRICATION PROCESS

The conventional fabrication process of the GAA device and our new fabrication process are shown in Figs 3 and 4. In the conventional silicon wire process, etching masks are patterned by the usual photo-lithography [Fig. 3(a)] and silicon is etched by dry etching [Fig. 3(b)]. Next, the silicon regions are narrowed by the additional process and silicon wires are formed as shown in Fig. 3(c). Buried oxide near the channel region are etched and free-standing silicon wires are formed. Then, gate oxidation and poly-silicon deposition are performed by a normal MOSFET process and the GAA structure is fabricated as shown in Fig. 3(d).

In our new fabrication process, we use an anisotropic etching technique to fabricate silicon wires. First, silicon nitride is patterned by the usual photo-lithography as shown in Fig. 4(a). Next, silicon is etched by anisotropic etching using tetramethyl-ammonium-hydroxide (TMAH) at 75°C. The etching rate of the (111) plane is so slow that the etching stops at the edge of the nitride and the (111) plane appears. Then, the (111) plane is covered by selective oxidation (200 Å) as shown in Fig. 4(b). Next, the silicon nitride is removed by hot phosphorus acid at 180°C and the anisotropic etching is performed again. The etching stops at the edge of the oxide as well as the first anisotropic

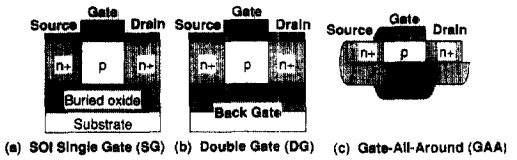

Fig. 1. Schematic views of: (a) single gate SOI device, (b) double gate SOI device and (c) gate-all-around device.

etching, thus two silicon wires are formed from one mesa as shown in Fig. 4(c). Buried oxide etching by HF, gate oxidation (200 Å) and poly-silicon deposition are performed and then the GAA structure is fabricated.

In our new process, the width of the wire channel is determined only by the thickness of the SOI layer and is not limited by the lithography resolution. It should also be noted that the density of wire channels is twice as large as that of the conventional process.

The SEM image of a fabricated GAA structure is shown in Fig. 5. The triangular channels surrounded by gate oxide and poly-silicon is successfully fabricated. The channel length, wire width and gate oxide thickness is 2 μm, 80 and 20 nm, respectively. The interval between wire channels is 300 nm.

3. GAA DEVICE SIMULATION

In order to investigate the advantage of GAA devices, short channel properties of the GAA device are simulated using a two-dimensional device simulator and compared with those of double gate and single gate SOI MOSFETs. The round channel is assumed and the cylindrical coordinates are used in the simulation of the GAA device. Schematic views of three devices are shown in Fig. 6. The channel diameter of the GAA device is set to the SOI thickness of double gate device and single gate devices. Simulation parameters are summarized in Table 1. The threshold voltage V_{th} is defined as a gate voltage V_{gs} when a drain current I_{ds} is $W/L \times 10^{-7}$ A/μm, where L and W are channel length and width, respectively. First, the electrical field distribution and the inversion charge are calculated using a device simulator and the effective electrical field of the channel E_{eff} is extracted from the conventional formula:

$$E_{eff} = \frac{Q_I/2 + Q_B}{\epsilon_s}, \qquad (1)$$

where Q_I is the inversion charge, Q_B is the depletion charge and ϵ_s is the dielectric constant of silicon.

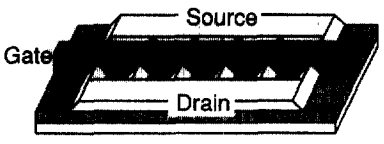

Fig. 2. A schematic view of the GAA VLSI MOSFET.

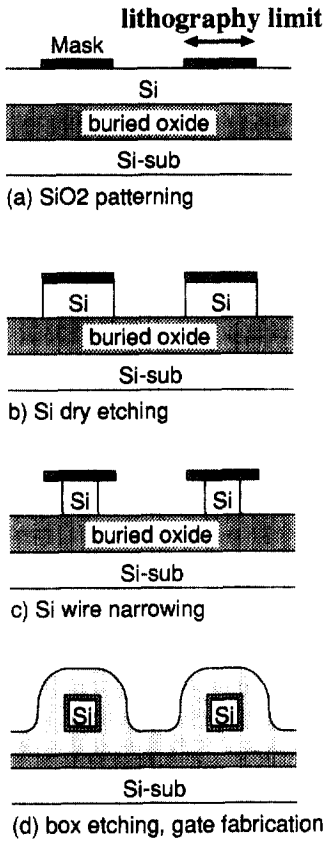

Fig. 3. The conventional fabrication process of the GAA devices.

Then, the mobility μ is determined by the following empirical relationship[9]:

$$(\mathrm{cm}^2/\mathrm{Vs})\ \mu = 3.25 \times 10^4 E_{eff}^{-1/3}\ (\mathrm{V/cm}) \qquad (2)$$

Fig. 7(a) shows the channel length dependence of the threshold voltage. The channel diameter and SOI thickness are 50 nm and the source drain voltage is 1.0 V in this case. Threshold voltages of the single gate and double devices rapidly go down as the gate length decreases. On the other hand, the threshold voltage of the GAA device does not drop even at 0.1 μm. Therefore, the GAA device suppresses the short channel effects much more than single and double gate devices. Figure 7(b) shows the channel length dependence of subthreshold swing S. S parameters of both the single gate and double gate devices are degraded, while in the GAA device it remains almost 60 mV/dec even at 0.1 μm. Thus, the GAA device shows the better immunity of the short channel effect.

The difference in the short channel effects in the three devices is well explained by the controllability of the channel potential by the gate electrode. In spite of the same channel diameter and the SOI thickness, the GAA device has a better short channel immunity than double and single gate device.

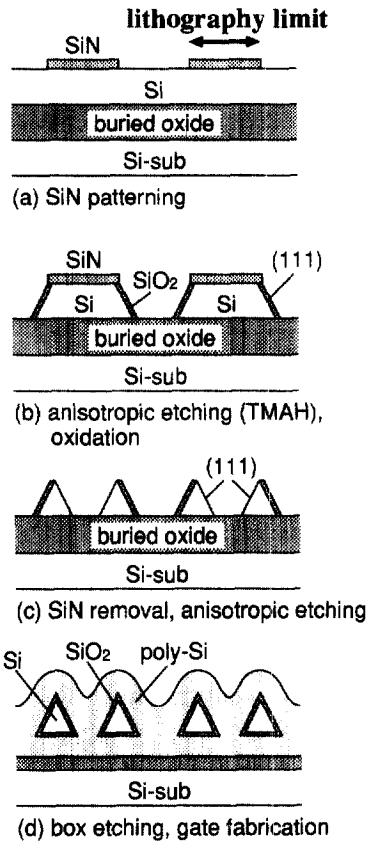

Fig. 4. The new fabrication process of the GAA devices.

Because the channel is surrounded by the gate, the potential of the channel region is controlled more strongly in the GAA channel structure.

From Fig. 7, which indicates that an acceptable channel length is 0.1 μm for the channel diameter of 50 nm, the minimum channel length in the GAA device is about twice as long as the channel diameter. Thus, the channel diameter must be less than half of the channel length.

The channel diameter and channel interval of the new and conventional GAA devices are compared in the followings. Take the case of the 0.1 μm generation. The gate length is then 0.1 μm. In the conventional GAA process, the channel diameter is 0.1 μm and the channel interval is 0.2 μm. However, the channel diameter should be less than half of the gate length as mentioned above. Therefore, the wire channel width of the conventional GAA devices must be narrowed down to 0.05 μm. Then, the ratio of the channel diameter to the channel interval is 1:4 and the channel density is 5 per μm. In the new GAA fabrication process, on the other hand, the channel diameter and the channel interval are independently determined. The channel diameter can be 0.05 μm by setting the SOI thickness properly. Although the channel interval is determined by the lithography, two wires are naturally formed in one mesa as shown in Fig. 4. Therefore, the interval can be 0.1 μm in the 0.1 μm generation. Then, the ratio of the channel diameter to the interval is 1:2 and the channel density is 10 per μm, which is doubled compared with the conventional GAA process.

Figure 8 shows the comparison of the drain current of the GAA device with the single gate device. The 0.1 μm generation is assumed. The new and conventional GAA devices are also compared. To make a fair comparison, the threshold voltage of the single gate device is set to the same as that of the GAA device (the SOI thickness of the GAA device is 50 nm, while that of the single gate device is 10 nm). In GAA devices, drain current is multiplied by the number of wire channels per 1 μm. The gate voltage is 1.0 V. It is found that the drain current of the conventional GAA device is smaller than that of the single gate. However, in the new GAA device, the drain current is doubled compared with that of the conventional GAA device and the

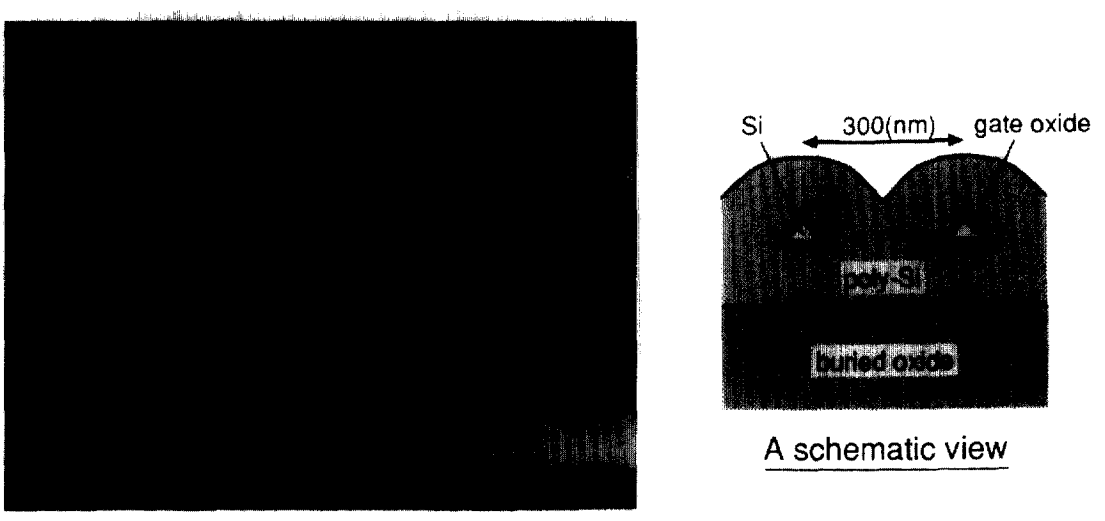

Fig. 5. A SEM image of a fabricated GAA device.

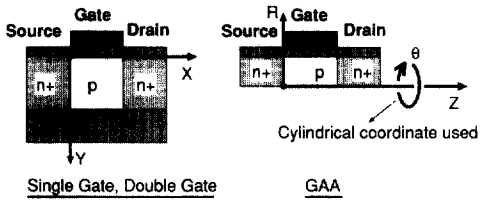

Fig. 6. Schematic views of the simulated single gate device, double gate device and GAA device.

Table 1. Device parameters of the simulated devices

Device parameters	
SOI thickness	50, 20 (nm)
Gate oxide thickness	10 (nm)
Channel concentration	1×10^{15} (cm^{-3})
Buried oxide thickness	100 (nm)

V_{th} definition: $V_{th} = V_{gs}$ [when $I_d = W/L \times 10^{-7}(A)$].

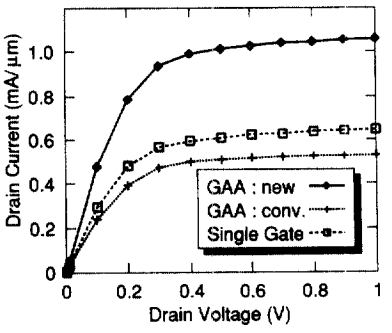

Fig. 8. A comparison of drain current of new GAA device, conventional GAA device and single gate device.

drain current is larger than that of the single gate, because the channel density is doubled.

4. CONCLUSIONS

A new fabrication process of GAA devices using an anisotropic etching technique has been proposed.

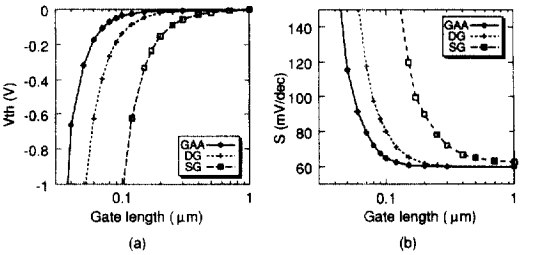

Fig. 7. A comparison of short channel effects of single gate, double gate, and GAA device: (a) the gate length dependence of the threshold voltage and (b) the gate length dependence of the subthreshold swing.

In the new fabrication process, the channel density can be doubled and the channel width can be determined only by the SOI thickness. It is shown that the GAA device has better short channel immunity than double gate and single gate SOI devices by the two dimensional device simulation. It is also shown that the current drivability is much enhanced by our new fabrication process.

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