Jpn. J. Appl. Phys. Vol. 38 (1999) pp. 2483–2486
Part 1, No. 4B, April 1999

High-Performance Accumulated Back-Interface Dynamic Threshold SOI MOSFET (AB-DTMOS) with Large Body Effect at Low Supply Voltage

Makoto TAKAMIYA[1,*], Takuya SARAYA[1], Tran Ngoc DUYET[1], Yuri YASUDA[1,2] and Toshiro HIRAMOTO[1,3]

[1]*Institute of Industrial Science, University of Tokyo, 7-22-1 Roppongi, Minato-ku, Tokyo 106-8558, Japan*
[2]*Faculty of Science and Engineering, Chuo University, Kasuga, Bunkyo-ku, Tokyo 112-8555, Japan*
[3]*VLSI Design and Education Center, University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan*

(Received October 6, 1998; accepted for publication December 10, 1998)

A high-performance accumulated back-interface dynamic threshold silicon-on-insulator metal-oxide-semiconductor field effect transistor (AB-DTMOS) with a large body effect at low supply voltage ($V_{dd} < 0.5$ V) is proposed for low-power applications. In AB-DTMOS, the back interface between the non-doped thin SOI and the buried oxide is accumulated by a large negative substrate bias, and the gate electrode is connected to this electrically induced body. AB-DTMOS realizes an ideal low/ultrahigh step channel profile electrically and achieves the maximum body effect. At fixed V_{th}, the body effect factor (γ) of AB-DTMOS is twice as large as that of the conventional uniformly doped channel DTMOS, because the channel depletion layer width of AB-DTMOS is half that of the conventional DTMOS. Experimental results show a steep subthreshold slope, a high current drive due to a large V_{th} shift, and a suppressed short channel effect.

KEYWORDS: dynamic threshold MOSFET (DTMOS), SOI MOSFET, body effect, low voltage, low power, high performance, accumulated back-interface

1. Introduction

The most effective approach for reducing power consumption of LSI is supply voltage scaling. The dynamic threshold metal-oxide-semiconductor field effect transistors (DTMOSs) are attractive for very low power applications due to the ideal subthreshold slope and the high current drive at very low supply voltage ($V_{dd} < 0.5$ V).[1–7] In DTMOS, the gate electrode is tied to the body. When the gate is turned on, V_{th} is lowered by ΔV_{th} due to the positive body bias and the current drive is enhanced. Therefore, in order to design a high-performance DTMOS, a large body effect for large ΔV_{th} is essential. In this paper, we propose a novel accumulated back-interface dynamic threshold silicon-on-insulator MOSFET (AB-DTMOS), in which a very large body effect is achieved by a thin SOI thickness.

2. AB-DTMOS

Figure 1 shows a schematic view of the proposed AB-DTMOS. The back interface between the non-doped thin SOI and the buried oxide is accumulated by a large negative back bias. The buried oxide thickness is determined by a balance between the source/drain parasitic junction capacitance and the back bias for the accumulation of back-interface. The gate electrode is connected to this electrically induced body. In the pMOS case, all the polarity shown in Fig. 1 is reversed. In CMOS application, the back gates below the buried oxide can be fabricated by the ion implantation through the buried oxide.[8,9] The body effect factors (γ) of the conventional DTMOS and AB-DTMOS are expressed as eqs. (1) and (2), respectively:

$$\gamma_{(\text{conventional DTMOS})} \equiv \left|\frac{\Delta V_{th}}{\Delta V_{bs}}\right| = \frac{C_D}{C_{fox}} \cong 3\frac{t_{fox}}{l_D} \quad (1)$$

$$\gamma_{(\text{AB-DTMOS})} = \frac{C_{SOI}}{C_{fox}} \cong 3\frac{t_{fox}}{t_{SOI}} \quad (2)$$

where C_{fox} is the gate oxide capacitance, C_D is the channel depletion capacitance, C_{SOI} is the SOI capacitance, l_D is the channel depletion layer width, t_{SOI} is the SOI thickness, and t_{fox} is the gate oxide thickness. In the conventional DTMOS, a uniformly doped channel profile is assumed, and the channel depletion layer width is reduced by the high channel doping. In AB-DTMOS, the channel depletion layer width is equal to the SOI thickness. Therefore, by thinning the SOI thickness, AB-DTMOS can reduce the channel depletion layer width and realize a larger γ, thus, achieving a higher current drive than the conventional DTMOS.

The accumulated back-interface devices with suppressed short channel effect have already been proposed as electrically thinned intrinsic channel (ETIC)-SOI MOSFETs,[10] in which the gate is not connected to the body. They have: (1) poor subthreshold slope (> 100 mV/dec) due to a small channel depletion layer width, (2) low current drive due to very high vertical electric field resulting from low mobility, and (3) severe floating body effect due to accumulated holes at the back interface. By connecting the gate to the body, AB-DTMOS overcomes all the above drawbacks and realizes: (1) an ideal subthreshold slope (60 mV/dec), (2) a high cur-

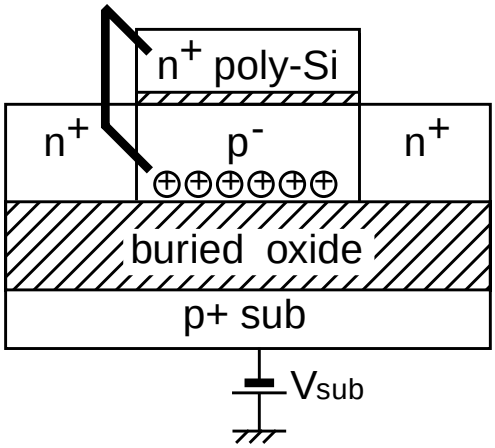

Fig. 1. A schematic view of AB-DTMOS. The back interface between the non-doped thin SOI and the buried oxide is accumulated by a large negative substrate bias. The gate electrode is connected to this electrically induced body.

*E-mail address: taka@nano.iis.u-tokyo.ac.jp

rent drive due to a large V_{th} shift and a high mobility, and (3) no floating body effect. Therefore, the AB-DTMOS has the advantages of both the ETIC-SOI MOSFET and the conventional DTMOS. In addition, AB-DTMOS suppresses the short channel effect better than ETIC-SOI MOSFET, because the drain depletion layer width is reduced by the forward body bias in DTMOS.

3. Experimental

The AB-DTMOS and the ETIC-SOI MOSFET are compared in the experiment. The devices measured are fully depleted (FD) SOI devices fabricated on a Separation by IMplanted OXygen (SIMOX) wafer.[11,12] The thicknesses of the gate oxide, SOI, and buried oxide are 10 nm, 40 nm, and 100 nm, respectively. An n^+ poly Si gate is used and the channel doping concentration is of the order of $10^{16}\,cm^{-3}$. The devices have body contact terminals. In order to show the advantages of AB-DTMOS, we have measured a single device in the three modes shown in Table I. When $V_{bs} = 0\,V$ and $V_{sub} = 0\,V$ (depleted back-interface), the devices operate in the FD SOI MOSFET mode. When $V_{bs} = 0\,V$ and $V_{sub} = -20\,V$ (accumulated back-interface), they operate in the ETIC-SOI MOSFET mode. When the gate is tied to the body ($V_{bs} = V_{gs}$) and $V_{sub} = -20\,V$, they operate in the AB-DTMOS mode. Figure 2 shows the subthreshold characteristics in the three modes. V_{th} of ETIC-SOI MOSFET is too high and that of FD SOI MOSFET is too low, but V_{th} of AB-DTMOS is just between them. Figure 3 shows the subthreshold characteristics of AB-DTMOS and ETIC-SOI MOSFET where V_{bs} is varied by 0.1 V steps. The body current of AB-DTMOS is also shown. AB-DTMOS has the same γ as ETIC-SOI MOSFET, because they have the identical device structures. Therefore γ of AB-DTMOS is derived from the V_{bs} dependence of V_{th} in ETIC-SOI MOSFET. Derived γ from Fig. 3 is as high as 0.8, because the ratio of the gate oxide thickness to the SOI thickness is high. Figures 4 and 5 show the V_{th} rolloff and the subthreshold slope degradation by the short channel effect. The definition of V_{th} is shown in the inset of Fig. 4. AB-DTMOS has an ideal subthreshold slope and suppresses the short channel effect very well. In Fig. 6, the on/off characteristics are compared. In this figure, the supply voltage is not 0.5 V but 1.5 V, because V_{th} of ETIC-SOI MOSFET is 0.9 V. In each device, the gate length is changed. AB-DTMOS shows a high current drive and a low off-current, while ETIC-SOI MOSFET shows a low current drive and FD SOI MOSFET shows a high off-current.

Table I. Three operation modes of the devices measured.

Operation mode	V_{bs}	V_{sub}
FD SOI MOSFET	0 V	0 V
ETIC-SOI MOSFET	0 V	−20 V
AB-DTMOS	$= V_{gs}$	−20 V

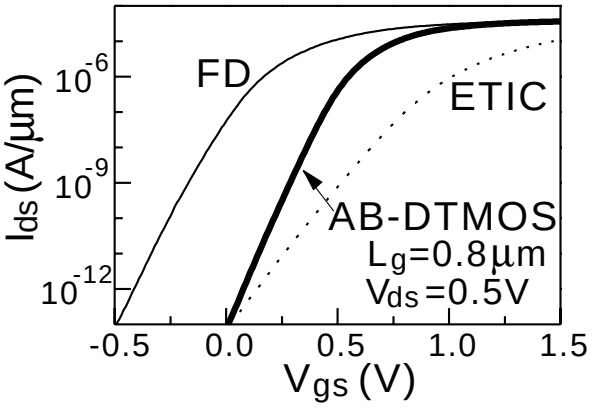

Fig. 2. Subthreshold characteristics of the FD SOI MOSFET, ETIC-SOI MOSFET, and AB-DTMOS shown in Table I. The gate length is 0.8 μm.

4. Comparison with the Conventional DTMOS

γ of AB-DTMOS and the conventional DTMOS are compared analytically. In the conventional DTMOS, a uniformly doped channel profile is assumed. V_{th} for both devices are expressed as a function of γ,

$$V_{th\,(\text{conventional DTMOS})} = 2\phi_{F1} - \frac{|V_{FB1}|}{1+2\gamma} \tag{3}$$

$$V_{th\,(\text{AB-DTMOS})} = 2\phi_{F2} - \frac{|V_{FB2}|}{1+\gamma} \tag{4}$$

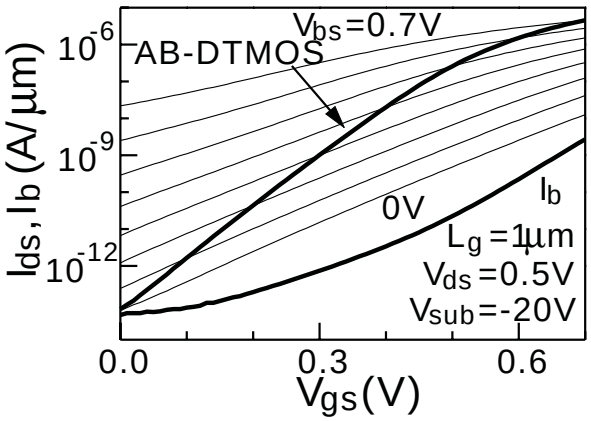

Fig. 3. Subthreshold characteristics of AB-DTMOS and ETIC-SOI MOSFET where body voltage (V_{bs}) is varied from 0 V to 0.7 V by 0.1 V steps. Body current (I_b) of AB-DTMOS is also shown. Derived γ is as high as 0.8.

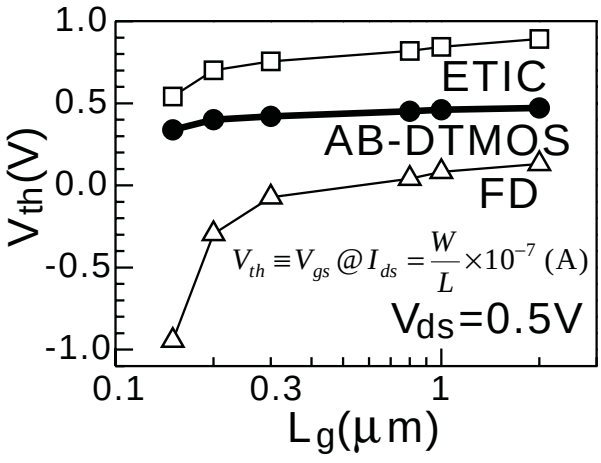

Fig. 4. Dependence of V_{th} on gate length. AB-DTMOS has appropriate V_{th} and suppresses the short channel effect well. The definition of V_{th} is shown in the inset.

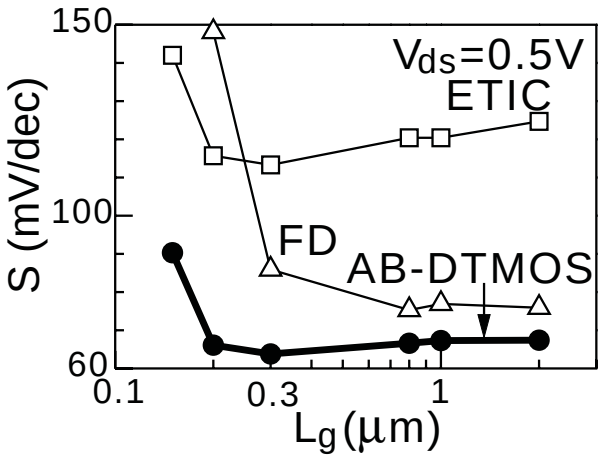

Fig. 5. Dependence of subthreshold slope on gate length. AB-DTMOS has an ideal subthreshold slope and suppresses the short channel effect well.

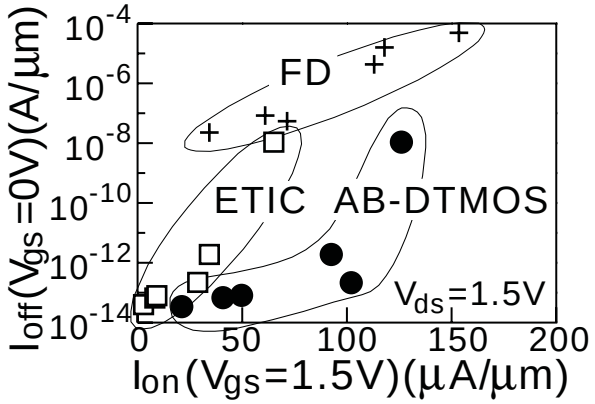

Fig. 6. On/off characteristics of FD SOI MOSFET, ETIC-SOI MOSFET, and AB-DTMOS. The gate length is varied. AB-DTMOS shows a high current drive and a low off-current. However, ETIC-SOI MOSFET shows a low current drive and FD SOI MOSFET shows a high off-current.

where ϕ_{F1} and ϕ_{F2} are Fermi potentials and V_{FB1} and V_{FB2} are work function differences. At a fixed V_{th}, it is expected that γ of AB-DTMOS will be twice as large as that of the conventional DTMOS, because the channel depletion layer width of AB-DTMOS is half that of the conventional DTMOS.[13] The reduction of the channel depletion layer width also leads to a suppressed short channel effect.

Figure 7 shows the dependence of V_{th} on γ calculated by simulation. To vary V_{th} and γ, the channel doping concentration is changed in the conventional DTMOS and the SOI thickness is changed in AB-DTMOS. In both devices, the increase in γ leads to an increase in V_{th}. As discussed above, AB-DTMOS has a larger γ at a given V_{th}. It should be noted that the experimental result ($V_{th} = 0.45$ V, $\gamma = 0.8$) fits the simulation very well. The retrograde channel profile has already been proposed in the conventional DTMOS for low V_{th} and large γ.[3] However, the retrograde channel profile always has a lower γ than that of AB-DTMOS at fixed V_{th}, because AB-DTMOS realizes an ideal low/ultrahigh step channel profile electrically and achieves a maximum γ.

The mobility of AB-DTMOS is compared with that of the conventional DTMOS. DTMOS operates at a lower vertical electric field than the conventional MOSFET, because the body is tied to the gate.[1,2] At a low vertical electric field,

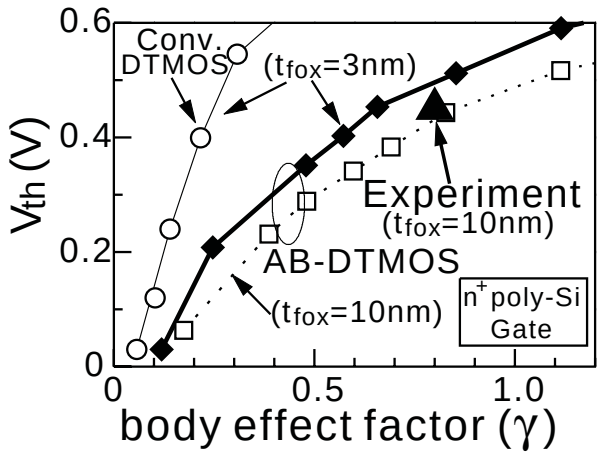

Fig. 7. Dependence of V_{th} on γ by the simulations for the conventional DTMOS (gate oxide thickness is 3 nm), and AB-DTMOS (gate oxide thickness is 3 nm or 10 nm). In the conventional DTMOS, a uniformly doped channel profile is assumed. Experimental data ($V_{th} = 0.45$ V, $\gamma = 0.8$) is also plotted. γ of AB-DTMOS is twice as large as that of the conventional DTMOS at a fixed V_{th}.

impurity scattering is dominant. An AB-DTMOS with a non-doped channel is possible, because the channel depletion layer width is determined by the SOI thickness and the channel impurity is not essential. Therefore, AB-DTMOS also shows a higher mobility than the conventional DTMOS due to a less impurity scattering. Both large γ and high mobility in AB-DTMOS result in a higher current drive.

5. Conclusions

We have proposed a high performance AB-DTMOS with a large body effect at low supply voltage. AB-DTMOS has a thin depletion layer width corresponding to the SOI thickness and an ideal low/ultrahigh channel profile, resulting in the maximum body effect. Experimental results show a steep subthreshold slope, a high current drive due to a large V_{th} shift, and a suppressed short channel effect.

Acknowledgements

This work was partly supported by Japan Society for the Promotion of Science (JSPS) Research for the Future Program and by Grant-in-Aid for Scientific Research on Priority Areas, "Ultimate Integration of Intelligence on Silicon Electronic Systems" from the Ministry of Education, Science, Sports, and Culture.

1) F. Assaderaghi, D. Sinitsky, S. Parke, J. Boker, P. K. Ko and C. Hu: Int. Electron Devices Meet. Tech. Dig. (1994) p. 809.
2) F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Boker, P. K. Ko and C. Hu: IEEE Trans. Electron Devices **44** (1997) 414.
3) C. Wann F. Assaderaghi, R. Dennard, C. Hu, G. Shahidi and Y. Taur: Int. Electron Devices Meet. Tech. Dig. (1996) p. 113.
4) F. Assaderaghi: *Ext. Abs. 1998 Int. Conf. Solid State Devices and Materials* (Business Center for Academic Societies Japan, Tokyo, 1998) p. 310.
5) H. Kotaki, S. Kakimoto, M. Nakono, T. Matsuoka, K. Adachi, K. Sugimoto, T. Fukushima and Y. Sato: Int. Electron Devices Meet. Tech. Dig. (1996) p. 459.
6) A. Shibata, T. Matsuoka, S. Kakimoto, H. Kotaki, M. Nakono, K. Adachi, K. Ohta and N. Hashizume: Symp. VLSI Technology (1998) p. 76.
7) T. Tanaka, Y. Momiyama and T. Sugii: Int. Electron Devices Meet.

Tech. Dig. (1997) p. 423.
8) I. Y. Yang, C. Vieri, A. Chandrakasan and D. A. Antoniadis: Int. Electron Devices Meet. Tech. Dig. (1995) p. 877.
9) T. Kachi, T. Kaga, S. Wakahara and D. Hisamoto: 1996 Symp. VLSI Technology (1996) p. 124.
10) T. Shimatani, S. Pidin and M. Koyanagi: *Ext. Abs. 1996 Int. Conf. Solid State Devices and Materials* (Business Center for Academic Societies Japan, Tokyo, 1996) p. 494.
11) M. Takamiya, T. Saraya, T. N. Duyet, T. Tanaka, H. Ishikuro, T. Hiramoto and T. Ikoma: Tech. Rep. IEICE SDM96-49 (1996) 81 [in Japanese].
12) T. Saraya, M. Takamiya, T. N. Duyet, T. Tanaka, H. Ishikuro, T. Hiramoto and T. Ikoma: IEEE Int. SOI Conf. Proc. (1996) p. 70.
13) K. Noda, T. Tsunami, T. Uchida, K. Nakajima, H. Miyamoto and C. Hu: IEEE Trans. Electron Devices **45** (1998) 809.