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# Measurement of Energetic and Lateral Distribution of Interface State Density in Fully-Depleted Silicon on Insulator Metal-Oxide-Semiconductor Field-Effect Transistors

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A new modification of the charge pumping (CP) technique based on the effect of reverse pulse bias on suppression of the geometric component is proposed in order to accurately determine the energetic and lateral distribution of interface state density ($D_{it}$) in fully-depleted silicon on insulator metal-oxide-semiconductor field-effect transistors (FD SOI MOSFETs). A comparison of the conventional CP techniques with the proposed method is also presented. It is demonstrated that using the proposed method, the precise estimation of the energetic and lateral distribution of $D_{it}$ can be simply obtained without interference from the geometry-dependent effect which often leads to the great difficulties in data interpretation in the conventional CP methods.

KEYWORDS: FD SOI MOSFET, charge pumping, geometric component, rise and fall time method, DC reverse bias, pulse reverse bias

## 1. Introduction

The interface between the silicon substrate and the gate oxide in the active region of a metal-oxide-semiconductor field-effect transistor (MOSFET) plays a crucial role in determining the device performances and affects the reliability and lifetime of the device. The measurement and characterization of the interface states are needed to understand the origin and physical properties of the interface states in a MOS system. Interface states can capture and emit charge carriers and the amount of charges in the interface states determines the device parameters.

The charge pumping (CP) technique[1–3] has evolved into a sensitive and reliable method to study the interface characteristics in a MOSFET. The major advantage of the CP technique is that it is available for direct measurement of the interface characteristics not only in a bulk MOSFET but also for characterizing both the front and back interface properties in a SOI MOSFET.[4,5]

The experimental setup for charge pumping measurements in a SOI MOSFET is shown in Fig. 1. The gate is connected to a pulse generator. The source and drain are connected together while the body is grounded through a DC ammeter. The principle of conventional CP is described in detail in refs. 2 and 3. When a gate pulse of sufficient amplitude to invert the surface is on, electrons flow to the surface from the source and drain. The surface states capture some of the inversion electrons and become negatively charged. When the pulse is off, the inversion layer electrons immediately flow back to the source and drain, while the captured ones are still retained by the interface states and recombine with the incoming holes from the body. Similarly, when the gate surface is pulsed from accumulation to inversion, the trapped holes recombine with electrons from the source and drain. These recombinations give rise to a DC current $I_{cp}$. By measuring this current, the interface state information can be obtained.

A major problem of the CP measurement on MOSFETs is the so-called "geometric component" of the CP current,[6,7] which occurs if all mobile carriers of one type, electrons (in NMOSFET) during the fall and holes during the rise of the gate pulse, are not removed rapidly enough before the arrival of the other type of carrier. The carriers that are left behind will recombine with carriers of the other type and therefore an additional component of CP current that does not involve the interface states arises. This parasitic component gives rise to an overestimation of interface state density ($D_{it}$). The geometric component is not often observed in bulk or partially-depleted (PD) SOI MOS transistors.

However, in FD SOI MOSFETs, particularly in very thin film SOI structures, where the resistivity of the body region is generally high, the CP current tends to have a very large geometry-dependent component[6] resulting in an overestimation of $D_{it}$. A detailed discussion of the geometric effect in FD SOI MOSFETs can be read in ref. 7. When the rise and fall times are relatively long, i.e. the measurement frequency is low, this undesirable component is negligible but the sensitivity is severely reduced due to a low signal/noise ratio of $I_{cp}$ and thus the use of the CP technique is limited to only large-area devices. Therefore, the new method to suppress this component and enhance the sensitivity is strongly required as the devices are scaled down. We have already developed a new measurement technique using the reverse pulse (RP) bias to suppress the geometric component in FD SOI MOSFET.[7] In the present work, we extend this method and apply it for the accurate measurements of energetic and lateral distributions of $D_{it}$ in FD SOI MOSFET by the RP charge pumping method.

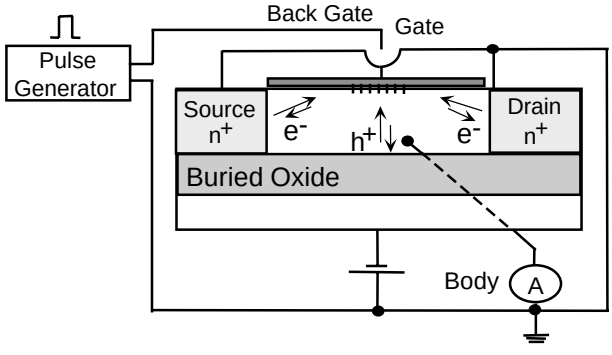


Fig. 1. Experimental setup for conventional charge pumping measurement on SOI MOSFETs.

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## 2. Device

The devices used in this study are fully-depleted SOI NMOSFETs as shown in Fig. 2. The thicknesses of the gate oxide, Si, and buried oxide films are 5 nm, 100 nm, and 98 nm, and the effective gate length and width are 2 $\mu$m and 20 $\mu$m, respectively. For source/drain and the main part of gate poly regions, phosphorus ions were implanted, while for the body contact, boron ions were used. It should be noted that boron ions were also implanted in the gate poly region near the body contact. More information on the fabricated device parameters is given in ref. 7.

## 3. Geometric Component and Reverse Pulse Method

Figures 3(a) and 3(b) show the waveform used in the RP method and the typical CP current characteristics obtained in the variable amplitude mode with different rise and fall times ($t_r$, $t_f$).[7] The observed two stepwise increases of $I_{cp}$ are the results of the two different $n^+$ and $p^+$ poly gate regions.[7] When $t_r$ and $t_f$ are 1 $\mu$s, no geometric component is observed and the $I_{cp}$ at the first step corresponds accurately to $D_{it}$. As $t_r$ decreases to 0.1 $\mu$s, the first step increases significantly due to the additional geometric component resulting from the inefficiency of hole collection by the body contact. As shown in Fig. 3 (b), by applying the RP bias ($V_p$) equal to $-1.6$ V to the body contact only during the rise time, the geometric component by holes is completely suppressed even if $t_r$ is 0.1 $\mu$s.

The result at a very low $V_p$ ($-2$ V) is nearly the same as that of $V_p = -1.6$ V, showing that the RP method also avoids the reduction of the effective channel length which is undesirably observed in the DC body bias technique.[6] The geometric component due to electrons, which is not observed in this sample, can also be suppressed by the RP bias to the source and drain only during the fall time.

## 4. Energetic Distribution of Interface State Density

The energy range of interface states contributing to $I_{cp}$ is determined by emission processes occurring in depletion and weak inversion, assuming all traps are filled with majority carriers during accumulation and with minority ones during inversion.[2] As shown in Fig. 4(b), when the gate surface is changed from inversion to accumulation, not all trapped electrons contribute to the CP recombination. Some of the trapped electrons located near the conduction band will be emitted during the fall time before the gate surface becomes accumu-

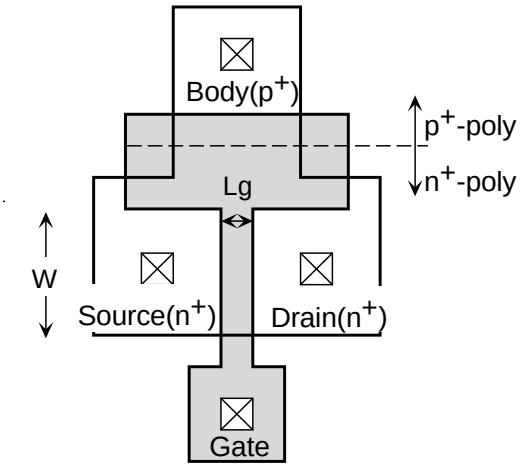


Fig. 2. Top view of the fabricated SOI devices.

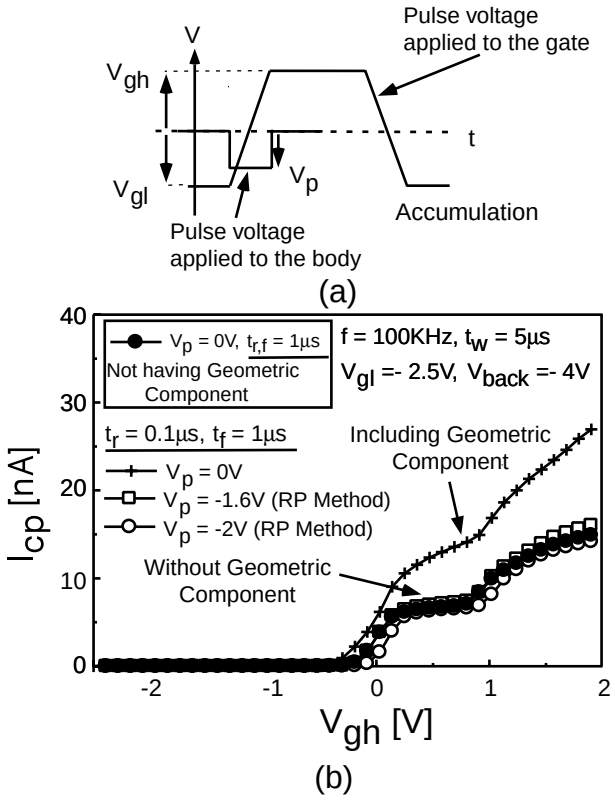


Fig. 3. (a) Illustration of pulse voltages applied to the gate and the body in the RP technique. (b) Charge pumping current as a function of the top level of the gate pulse under various rise and fall times in a FD SOI MOSFET. Results at a long $t_{r,f}$ (1 $\mu$s) do not have any geometric component.

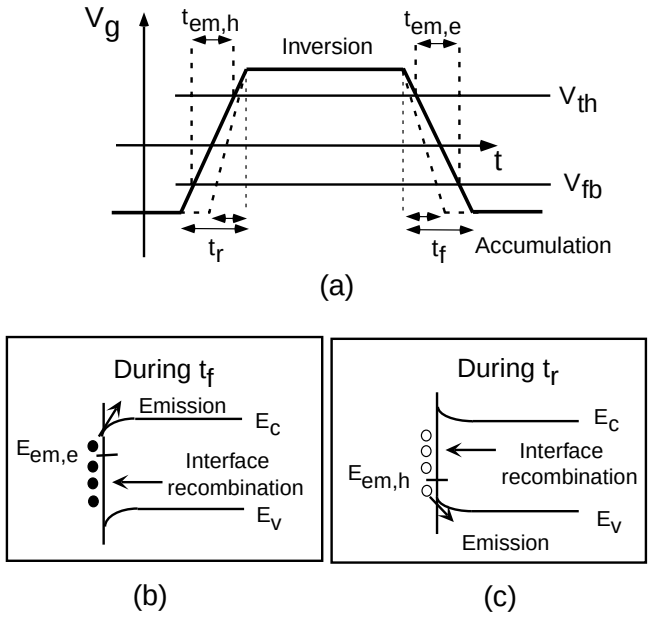


Fig. 4. (a) Waveform of applied gate pulse used in CP measurements. $t_{em,h}$ and $t_{em,e}$ determined by $t_r$ and $t_f$ are the times for trapped holes and electrons to be emitted when the gate surface is pulsed from accumulation into inversion and from inversion into accumulation, respectively. (b), (c) Illustrations of emission processes of the trapped electrons and holes during $t_f$ and $t_r$. Only traps having an energy between $E_{em,h} \sim E_{em,e}$ contribute to the $I_{cp}$.[2,8]

lated. The fall time of the gate pulse determines the electron emission level ($E_{em,e}$) and only the trapped electrons below it contribute to $I_{cp}$. Similarly, when the gate surface is pulsed from accumulation to inversion, there is a hole emission level ($E_{em,h}$) and only trapped holes located above it contribute to $I_{cp}$ as shown in Fig. 4(c). When $t_r$ and $t_f$ of the gate pulse and consequently the emission times of the trapped holes ($t_{em,h}$) and the trapped electrons ($t_{em,h}$) are long, the emission levels are shifted to the midst of the band gap. On the contrary, when $t_r$ and $t_f$ and correspondingly the times for these holes and electrons to be emitted are short, these levels are located near the band edges. The principle of the conventional $t_{r,f}$ method[8] is that by changing $t_r$ and $t_f$ of the gate pulse as illustrated in Fig. 4(a), the energy range that is attributed to the CP will change and from the derivative of the $I_{cp}$ with respect to these times, the energy distribution of $D_{it}$ can be calculated.

Figure 5 shows the $t_r$ and $t_f$ dependences of $I_{cp}$ in a FD SOI MOSFET. When $t_f$ is 1 $\mu$s and $t_r$ is varied, $I_{cp}$ increases rapidly at $t_r = 0.1\,\mu$s due to the geometric component, indicating that an accurate energetic distribution cannot be obtained. The geometric component due to the electrons does not occur in this device because the channel length (2 $\mu$m in this case) is short enough for the inversion electrons to flow back to the source and drain during the fall time of the gate pulse. Therefore, when $t_r$ is 1 $\mu$s and $t_f$ is varied, $I_{cp}$ just increases gradually because of an increase in an energy range which can be scanned by the gate pulse with different $t_f$. The result using the RP method is also demonstrated in this figure. The reverse pulse bias is applied to the body contact in order to improve the hole response and subsequently effectively suppress the geometric effect. The parasitic geometric component is negligible and no rapid increase in $I_{cp}$ is observed even at $t_r = 0.1\,\mu$s.

$D_{it}$ obtained from the derivative of $I_{cp}$ with respect to the $t_r$ and $t_f$ can be written as follows[9]

$$D_{it}(E_{em,h}) = -\frac{t_r}{qA_gkTf}\cdot\frac{dI_{cp}}{dt_r} \quad (1)$$

$$D_{it}(E_{em,e}) = -\frac{t_f}{qA_gkTf}\cdot\frac{dI_{cp}}{dt_f} \quad (2)$$

where $q$ is the electron charge, $A_g$ is the channel area of the transistor and $f$ is the frequency of the gate pulse.

The following expressions of $E_{em,h}$ and $E_{em,e}$ can be derived according to the theory of emission of carriers from the surface states.[2]

$$E_{em,h} = E_i + kT\ln\left(v_{th}\sigma n_i\left|\frac{V_{th}-V_{bf}}{\Delta V_g}\right|t_r\right) \quad (3)$$

$$E_{em,e} = E_i - kT\ln\left(v_{th}\sigma n_i\left|\frac{V_{th}-V_{bf}}{\Delta V_g}\right|t_f\right) \quad (4)$$

where $E_i$ and $n_i$ are the intrinsic Fermi energy and concentration, $v_{th}$ is the thermal velocity of the carriers, $V_{th}$ and $V_{bf}$ are the threshold and flat band voltages of a device.

In the RP method, the reverse bias applied to the body contact leads to an increase in $V_{th}$ and a decrease in $V_{bf}$. As a result, the time for the trapped holes to be emitted becomes longer compared with that of the conventional method. It should be noted that a change in $V_{th}$ and $V_{bf}$ by the reverse bias can be simply estimated using the conventional variable base CP mode.[2]

Using eqs. (1)–(4), the energetic distribution of $D_{it}$ with and without the RP body bias can be evaluated as shown in Fig. 6. When the RP method is not used, the extracted $D_{it}$ increases rapidly near the valence band edge. However, by applying to the RP bias $V_p = -1.6$ V, an accurate $D_{it}$ can be evaluated. As explained above, due to the reverse bias at the rise time, the hole emission time becomes longer, therefore, the measurable energy range is shifted to the midst of the energy gap in the RP method.

As shown in Figs. 5 and 6, when $t_r$ larger than 0.3 $\mu$s is used, the influence of the geometric effect is avoidable for the devices used in this study. However, the long rise and fall times of the gate pulse cannot be freely chosen in the high frequency measurements that are essential for scaled devices. Therefore, the proposed RP method will become more important as the device size shrinks.

## 5. Lateral Distribution of Interface State Density

The lateral profile of $D_{it}$ can be obtained by applying the DC reverse bias[9,10] to the source and drain or the body contact. The principle of this DC technique is to use charge pumping to detect the integrated amount of interface traps

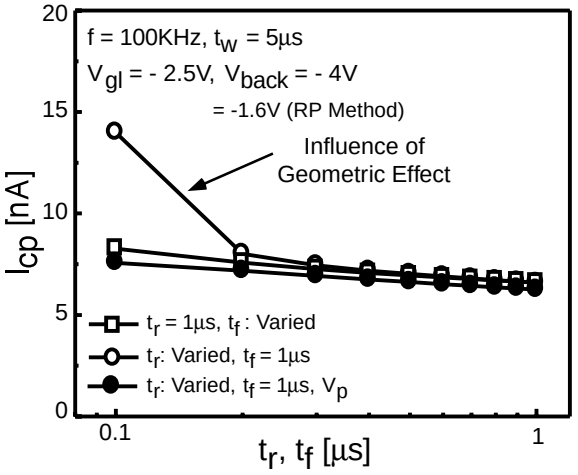


Fig. 5. Rise and fall time dependence of $I_{cp}$ in a FD SOI MOSFET. Accurate rise time dependence of $I_{cp}$ is obtained when applying a reverse pulse bias of $V_p = -1.6$ V to the body.

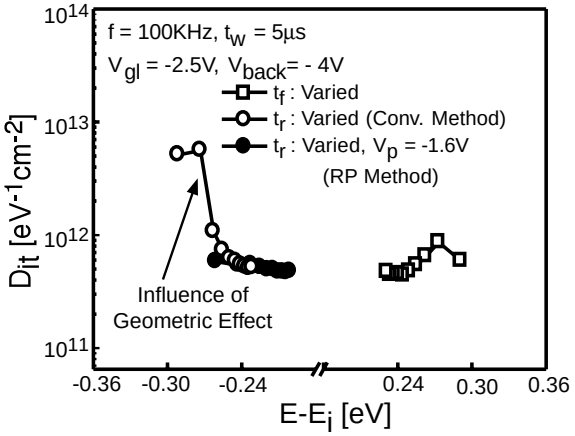


Fig. 6. Energetic distribution of interface state density with and without the body reverse pulse bias. An overestimation of $D_{it}$ in the conventional method is resolved by applying the reverse pulse bias to the body.

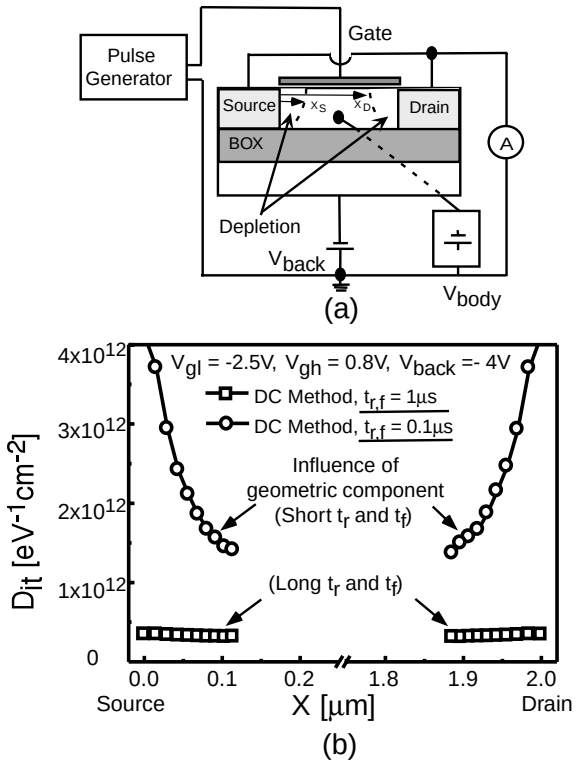


Fig. 7. (a) Experimental setup for determining lateral distribution of $D_{it}$ in the DC reverse bias method. The DC reverse bias is applied to the body contact to vary the depletion layer widths near the source and drain. (b) Interface state density as a function of distance between the source and drain. The DC reverse technique is inapplicable when $t_r$ and $t_f$ are short.

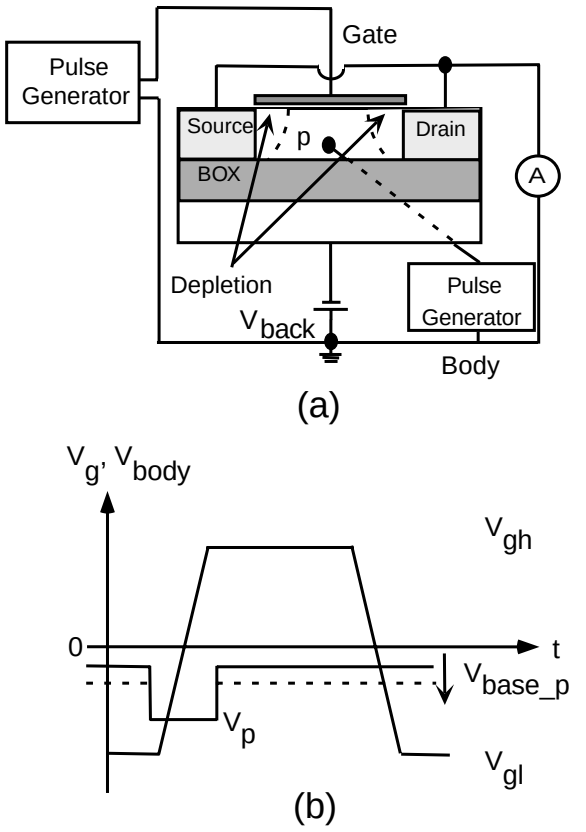


Fig. 8. (a) Experimental setup for determining lateral distribution of $D_{it}$ in the proposed RP method. Instead of the DC bias, the reverse pulse bias is applied to the body contact. (b) Waveform of the pulse biases applied to the gate and the body in the RP technique. $V_p$ is fixed to suppress the geometric component while $V_{base\_p}$ is varied in order to control the depletion layer width.

while varying the size of the region from which the interface traps can contribute, by modulating the source and drain depletion widths.

In our experiment, the reverse bias $V_b$ is applied to the body contact to control the depletion widths as illustrated in Fig. 7(a). In general, the CP current is given by[11)]

$$I_{cp} = f \cdot q \cdot W \int_{X_S}^{X_D} q\Delta\Psi_s dx \tag{5}$$

where

$$X_S = \sqrt{\frac{2\epsilon_{si}\epsilon_0}{qN_A}} \times \left[(V_b + 2\Phi_F)^{1/2} - (2\Phi_F)^{1/2}\right] \tag{6}$$

$$X_D = L_{eff} - \sqrt{\frac{2\epsilon_{si}\epsilon_0}{qN_A}} \times \left[(V_b + 2\Phi_F)^{1/2} - (2\Phi_F)^{1/2}\right] \tag{7}$$

$\Delta\Psi_s$ is the change of surface potential, $f$ is the frequency of the gate pulses, $\Phi_F$ is the built-in potential, $L_{eff}$ and $W$ are the effective length and width of a device.

With a floating source contact and a different body bias, the source end of the depletion region $X_S$ in the channel is fixed, but the drain depletion edge increases. After measuring the $I_{cp}$ given by eq. (5), the lateral distribution $D_{it}$ near the drain end can be obtained by straightforward calculation as follows

$$D_{it}(X_D) = \frac{1}{fqW\Delta\Psi_s(X_D)} \times \left(\frac{dX_D}{dV_b}\right) \cdot \left(\frac{dI_{cp}}{dV_b}\right) \tag{8}$$

The distribution of $D_{it}$ near the source end can be similarly obtained by floating the drain contact and varying the body bias.

The experimental results are shown in Fig. 7(b). When $t_{r,f}$ $(= 1\,\mu s)$ is long enough for holes to flow back to the body during the rise of the gate pulse, a precise value for the lateral distribution can be estimated. However, in the short $t_r$ and small DC body bias, the geometric component leads to an overestimation of $D_{it}$.

To overcome this difficulty, instead of using the DC bias, a reverse pulse bias is applied to the body contact as illustrated in Fig. 8(a). Figure 8(b) shows the new RP waveform used in the proposed method, where the top level ($V_p$) of the RP body bias is kept constant during the rise time to suppress the ge-

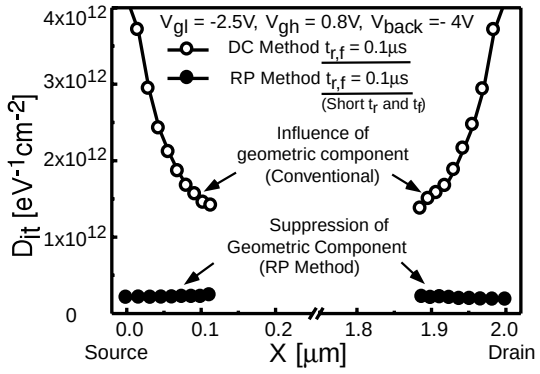


Fig. 9. Comparison between the measured lateral distributions of $D_{it}$ by the DC and the proposed RP methods for a very short $t_{r,f}$ $(0.1\,\mu s)$. An accurate result of $D_{it}$ is obtained by the proposed RP technique while the overestimation of $D_{it}$ is evaluated in the conventional DC method.

ometric effect and its base level ($V_{base\_p}$) is changed in order to vary the depletion widths. This waveform expands the depletion regions while suppressing the geometric component. Therefore, the lateral $D_{it}$ distribution can be accurately determined.

Figure 9 shows the lateral profiles of $D_{it}$ obtained by the DC reverse bias and the present RP bias methods for $t_r$ and $t_f$ being as short as 0.1 $\mu$s. In the DC method the extracted $D_{it}$ is dramatically overestimated due to the geometric component. However, in the proposed RP method, the geometric component is not involved even when $t_r$ and $t_f$ are 0.1 $\mu$s. This method is sensitive with a high frequency and can be applied to the scaled FD SOI MOSFETs.

## 6. Conclusions

A new method for determining energetic and lateral distributions of the interface state densities is proposed. The main advantage of this method is that it allows us to accurately measure the interface state properties in FD SOI MOSFETs where the conventional CP method is inapplicable due to the parasitic geometric component. The proposed method can be expected to be more powerful in scaled FD SOI devices, in which a high frequency CP pulse, and consequently a small rise and fall time must be used to improve the signal/noise ratio.

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