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# Low Power and Low Voltage MOSFETs with Variable Threshold Voltage Controlled by Back-Bias

**Toshiro HIRAMOTO**[†,††a)], ***Member and*** **Makoto TAKAMIYA**[††], ***Nonmember***

**SUMMARY** We have studied the characteristic trade-offs in low power and low voltage MOSFETs from the viewpoint of back-gate control and body effect factor. Previously reported MOSFET structures are classified into four categories in terms of back-gate structures. It is shown that a MOSFET with a fixed back-bias has only a limited current drive at low voltage irrespective of device structures, while current drive of a dynamic threshold MOSFET with body tied to gate is more enhanced with increasing body effect factor. We have proposed a new dynamic threshold MOSFET, electrically induced body (EIB) DTMOS, which has a very large body effect factor at low threshold voltage and high current drive at low supply voltage.

***key words:*** *MOSFET, low power, low voltage, variable threshold voltage, back-bias, body effect, DTMOS, SOI*

## 1. Introduction

Low power technology has become one of the mainstream technologies in VLSI device design. The power of high-end microprocessors is now more than 40 W. According to the International Technology Roadmap for Semiconductors (ITRS) [1], the power will be more than 180 W in 2014 in microprocessors with heat sink. In order to reduce the power, the supply voltage should be reduced down to less than 0.6 V in 2014. Moreover, the rapid spread of battery-operated portable systems strongly demands a radical reduction of not only active power but also stand-by power. Very high-speed devices with ultra-low power will be essential for most of the VLSI applications in the future. Using conventional MOSFETs, however, it will be very hard to meet all the requirements of high-performance VLSIs.

One of the most promising ways to attain both high speed and low stand-by power at low supply voltage is to vary the threshold voltage of MOSFETs by changing back-bias. Many devices and circuits for the variable threshold voltage configurations have been reported previously for ultra-low power applications [2]–[13]. In particular, the dynamic threshold MOSFET (DTMOS) configuration where the gate electrode is directly connected to the body or well region [6]–[13] has many advantages including ideal subthreshold swing, high current drive, and better short channel effect immunity. The control of the threshold voltage will be inevitable for high-performance and low-voltage VLSIs with ultra-low power consumption.

The body effect factor $\gamma$ is one of the most important parameters in a MOSFET with controlled threshold voltage. In order to change the threshold voltage by small back-bias, a large body effect factor is required. In conventional MOS circuits, however, a small body effect factor has been generally preferable because a large body effect degrades the current drive and circuit performance. Therefore, the optimum device design would not be necessarily the same for conventional MOSFETs and variable threshold devices. It strongly depends on whether the body effect is positively utilized or not.

In this paper, characteristics of low power and low voltage MOSFETs with variable threshold voltage controlled by back bias are studied. In particular, special focus is placed on the body effect factor $\gamma$, and the advantages and disadvantages of back-bias control are discussed in terms of the body effect factor. First, the trade-offs in low voltage MOSFETs are reviewed. Next, MOSFET structures are classified into four categories in terms of the back-gate configurations and possible device structures with back-gates are reviewed. Then, the limitations of conventional MOSFETs with a fixed back-bias are pointed out and the advantages of the dynamic threshold configuration are demonstrated by means of two-dimensional device simulation. Finally, a new dynamic threshold MOSFET with a large body effect factor is analyzed and its superiority is shown.

## 2. Trade-Offs in Low Voltage MOSFETs

In this section, the characteristic trade-offs in conventional MOSFETs are discussed. First, the general relation between power consumption and circuit speed is considered. Next, the short channel effect and current drive in a MOSFET with a fixed back-bias are discussed from the viewpoint of the body effect factor.

### 2.1 Power and Speed

The total power $P_{\text{total}}$ and gate delay $t_{\text{pd}}$ of a CMOS circuit are given by

$$P_{\text{total}} = P_{\text{active}} + P_{\text{stand-by}}$$

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[†]The author is with VLSI Design and Education Center, The University of Tokyo, Tokyo, 113-8656 Japan.
[††]The authors are with Institute of Industrial Science, The University of Tokyo, Tokyo, 106-8558 Japan.
a) E-mail: hiramoto@nano.iis.u-tokyo.ac.jp

$$= fC_{\rm load}{V_{\rm dd}}^2 + I_{\rm leak}V_{\rm dd} \quad (1)$$

$$t_{\rm pd} \propto \frac{C_{\rm load}V_{\rm dd}}{I_{\rm on}} \propto \frac{V_{\rm dd}}{(V_{\rm dd}-V_{\rm th})^{\alpha}} \quad (2)$$

where $P_{\rm active}$ is active power, $P_{\rm stand-by}$ stand-by power, $f$ operation frequency, $C_{\rm load}$ total load capacitance, $V_{\rm dd}$ supply voltage, $I_{\rm leak}$ total leakage current, $I_{\rm on}$ current drive of MOSFET, and $V_{\rm th}$ threshold voltage of the device. $\alpha$ is a factor depending on the carrier velocity saturation and is about 1.3–1.5 in advanced MOSFETs [14]. Based on Eq. (1), the most effective way to reduce the total power is to reduce the supply voltage.

However, the reduction of the supply voltage causes the reduction of gate drive ($V_{\rm dd}$ - $V_{\rm th}$), and hence, the severe degradation of circuit speed, as shown in Eq. (2). Although lowering the threshold voltage enhances gate drive, it leads to an exponential increase in subthreshold off-current and stand-by power. If the threshold voltage is defined as gate voltage when drain current is $10^{-7}$ A/$\mu$m, the off-current is given by

$$\frac{I_{\rm off}}{W_{\rm g}} = 10^{-7-\frac{V_{\rm th}}{S}}\ {\rm A}/\mu{\rm m} \quad (3)$$

where $S$ is subthreshold factor and $W_{\rm g}$ gate width. In order to suppress the off-current at a given threshold voltage, $S$ should be reduced. However, the smallest limit of $S$ at room temperature is 60 mV/dec and this value is not scaled. At very low supply voltage, therefore, it is very hard to attain both the high speed and low stand-by current.

### 2.2 Body Effect Factor and Subthreshold Factor

In the following subsections, the body effect factor in a device with a fixed back-bias is considered. When the body effect factor $\gamma$ is defined as the ratio of threshold voltage shift to back-bias, $\gamma$ is given by

$$\gamma \equiv \left|\frac{\Delta V_{\rm th}}{\Delta V_{\rm bs}}\right| = \frac{C_{\rm d}}{C_{\rm ox}} \cong 3\frac{t_{\rm ox}}{l_{\rm d}} \quad (4)$$

where $V_{\rm bs}$ is the back-bias, $C_{\rm d}$ depletion layer capacitance, $C_{\rm ox}$ gate capacitance $t_{\rm ox}$ gate oxide thickness, and $l_{\rm d}$ depletion layer width. When the gate oxide thickness is constant, a device with thinner depletion layer width (i.e. with higher impurity concentration in the case of bulk MOSFET) has larger $\gamma$.

The subthreshold factor S at room temperature is given by

$$S = 60\frac{dV_{\rm g}}{d\psi_{\rm s}} = 60\left(1+\frac{C_{\rm d}}{C_{\rm ox}}\right) \cong 60\left(1+3\frac{t_{\rm ox}}{l_{\rm d}}\right)\ {\rm mV/dec} \quad (5)$$

where $\psi_{\rm s}$ is surface potential, when the gate length is long enough and the short channel effect can be neglected. From Eqs. (4) and (5), the relationship between the body effect factor and subthreshold factor is given by

$$S = 60\,(1+\gamma)\ {\rm mV/dec} \quad (6)$$

This equation shows that a device with a larger body effect factor has a larger subthreshold factor and that the ideal subthreshold factor (60 mV/dec) can be achieved when the body effect factor is zero.

### 2.3 Short Channel Effect and Body Effect Factor

The short channel effect is strongly affected by the depletion layer width. If the gate oxide thickness and the source/drain junction depth are constant, a device with thinner depletion layer width has better short channel effect immunity. From Eq. (4), therefore, the short channel effect is closely related to the body effect factor. A device with larger $\gamma$ has better short channel effect immunity.

### 2.4 Current Drive and Body Effect Factor

One more severe trade-off in a MOSFET with a fixed back-bias is the relationship between current drive and body effect factor. It is well known that current drive of a device with a higher body effect factor is degraded by the bulk charge effect. Moreover, the mobility is also degraded due to the high vertical electric field because the device has thin depletion layer width. Current drive further decreases because threshold voltage should be set higher to suppress the off-current due to larger subthreshold swing.

Figure 1 illustrates the relations among the subthreshold swing, body effect factor, short channel effect, and current drive. A device with ideal subthreshold swing has very small body effect factor and high current drive, but has worse short channel effect. On the other hand, a device with better short channel effect has larger body effect factor, but has worse subthreshold swing and smaller current drive.

Some of the above-mentioned trade-offs in a MOSFET with a fixed back-bias can be overcome by dynamic control of threshold voltage by changing back-bias. Detailed simulation results in devices with a fixed back-bias and a variable back-bias will be shown in Sect. 4.

## 3. Classification of MOSFETs by Back-Bias

In this section, MOSFETs are classified into four categories according to back-gate structures and back-gate potentials. For simplicity, only the back-gate structure and potential are considered. Figure 2 shows the classification of MOSFETs. Schematic cross-sections and equivalent capacitance circuits are shown. Some of the

reported device structures are classified and their qualitative characteristics are discussed.

### 3.1 Four Basic Structures

There are two basic back-gate structures, as shown in Fig. 2. The first structure is "bulk," where the well or body works as a back-gate and the back-gate is faced to the channel via the depletion layer capacitance. The depletion layer width is usually determined by the impurity concentration and its profile. This category includes conventional bulk MOSFETs, delta-doped MOSFETs [15], and partially depleted (PD) SOI MOSFETs. An electrically induced body (EIB) structure [12] that is discussed later is also classified into this category. The second structure is basically a fully depleted (FD) SOI structure although there are many variations. There is a buried oxide layer under the channel and the back-gate is faced to the channel via FD SOI capacitance $C_{\rm SOI}$ and buried oxide capacitance $C_{\rm box}$.

On the other hand, the way of applying back-biases to the back-gate is also classified into two categories. The back-bias is fixed in the first category as is generally used. In the second category, the back-gate is tied to the front gate and the device acts as a DTMOS or a double gate (DG) MOSFET.

Then, all the device would be classified into four categories, as shown in Fig. 2. The four categories are respectively named as "conventional MOS," "FD SOI MOS," "DTMOS," and "DG MOS." In the following sections, characteristics of classified MOSFETs are analyzed. In some variable threshold voltage configurations, two back-biases are used so that the threshold voltage is low in the active mode and high in the standby mode. This two-back-bias configuration is often called as variable threshold MOSFET (VTMOS) [2]. The VTMOS configuration is eliminated in the analysis in this paper, because the characteristics strongly depend on the difference in two back-biases. Detailed investigations of the VTMOS configuration will be reported elsewhere [16].

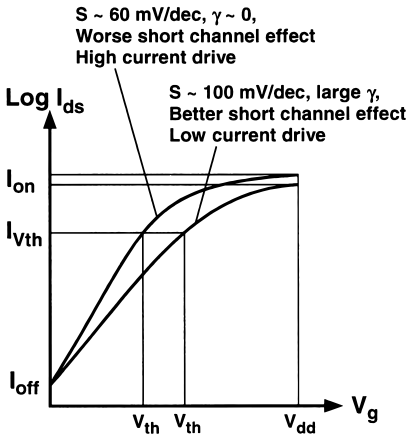



**Fig. 1** A schematic illustration of the relationships among the subthreshold swing, body effect factor, short channel effect, and current drive.

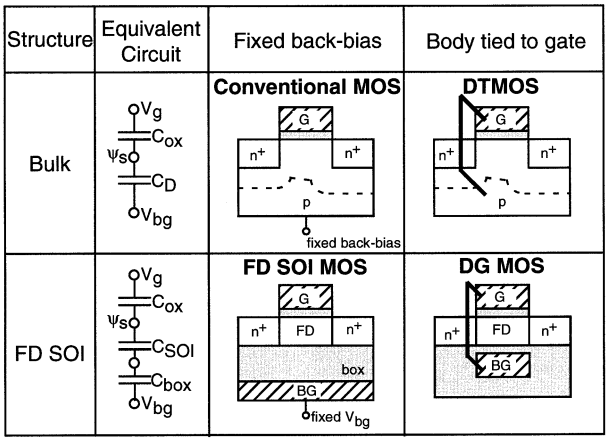



**Fig. 2** Classification of MOSFETs in terms of back-gate structures and back-gate potentials. Schematic cross-sections and equivalent capacitance circuits are shown.

### 3.2 Variations of Conventional MOSFETs

Figure 3 shows some variations of "conventional MOS." A bulk MOSFET with uniform well impurity concentration (uniform bulk MOSFET) is a typical structure in this category. The depletion layer width of uniform bulk MOS is affected only by the channel impurity concentration. The well acts as a back-gate.

A delta-doped MOSFET [15] has a steep channel concentration profile, where a surface layer with low concentration is on a layer with high concentration.

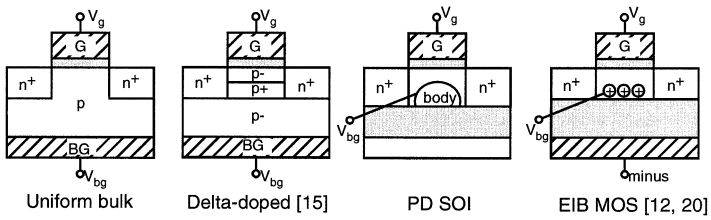



**Fig. 3** Schematic cross-sections of variations of "conventional MOS." Uniformly doped bulk MOSFET, delta-doped MOSFET, PD SOI MOSFET, and EIB MOSFET are shown.

Although many types of MOSFETs with channel engineering have been reported including retrograde channel, super steep retrograde channel [17], and ground plane [18], the characteristics of these MOSFETs are just between the uniform bulk MOSFET and delta-doped MOSFET. In a delta-doped MOSFET, the depletion layer width roughly corresponds to the thickness of the surface layer with low concentration. It is reported that at a given threshold voltage, the depletion layer width of delta-doped MOSFET is half of that of uniform bulk MOSFET [15]. Therefore, the delta-doped MOSFET generally has better short channel effect immunity and larger body effect factor but worse subthreshold swing and smaller current drive.

A PD SOI MOSFET is classified into this category because the body is faced to the channel via the depletion layer capacitance and the equivalent circuit is the same as that of a bulk MOSFET. The body acts as a back-gate in PD SOI MOSFETs. When the body is floating, characteristics vary drastically [19]. The floating body PD SOI MOSFET is out of the range of this paper.

One way to increase the body effect factor is to make an EIB structure as shown in the figure [12], [13], [20]. Large substrate bias is applied to SOI substrate to induce carriers in back $Si/SiO_2$ interface and this electrically induced body acts as a back-gate. Since the back-gate is faced to the channel via the depletion layer, the EIB structure is also categorized in the "conventional" MOSFET. The depletion layer corresponds to the thickness of SOI layer. Therefore, the body effect factor can be very large if the SOI thickness is very thin.

### 3.3 Variation of DTMOS

If the back-gates of above mentioned devices are tied to gate electrodes, they become DTMOS. Figure 4 shows variations of DTMOS structures. Bulk DTMOS [8]–[10], PD DTMOS [6], [7], [11], and EIB-DTMOS [12], [13] are shown in the figure. Since the back-bias follows the gate voltage, the surface potential also follows the gate voltage and ideal subthreshold swing can be obtained in DTMOS as shown in Eq. (5).

### 3.4 Variations of FD SOI MOSFETs

Figure 5 shows examples of FD SOI MOSFETs. Quite a few structures using FD substrate or buried back-gates have been reported as shown in the figure. In FD SOI MOS, one of the concerns is the suppression of short channel effect [19], [21], [22]. Basically, the discussions and Eqs. (1)–(6) in Sect. 2 apply to FD SOI MOS. In this case, the depletion layer capacitance $C_{\rm d}$ in the equations should be replaced to the serial connection of SOI capacitance $C_{\rm SOI}$ and buried oxide capacitance $C_{\rm box}$. When the buried oxide is thick, subthreshold swing is good and body effect factor is small, but the

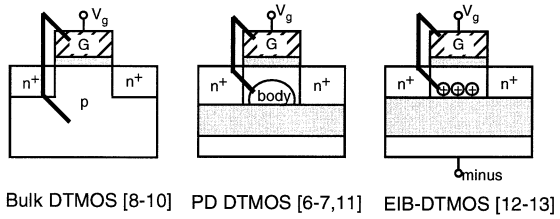



**Fig. 4** Schematic cross-sections of variations of DTMOS. Bulk DTMOS, PD DTMOS, and EIB-DTMOS are shown.

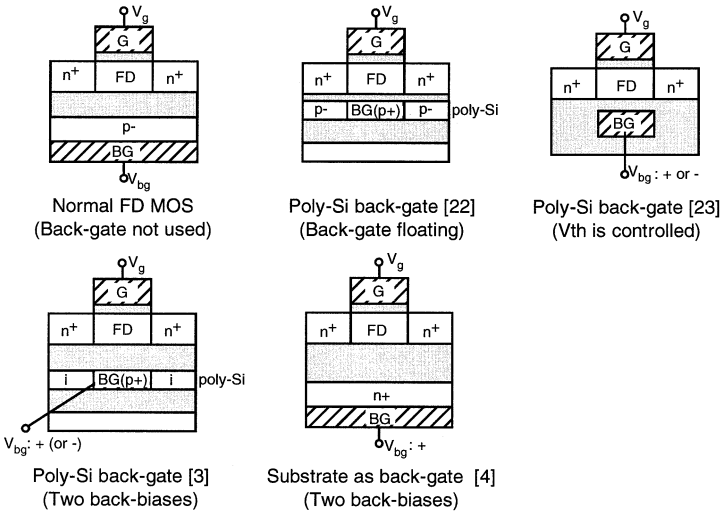



**Fig. 5** Schematic cross-sections of examples of FD SOI MOSFETs. Normal FD SOI MOSFET and some other structures with buried back-gates are shown.

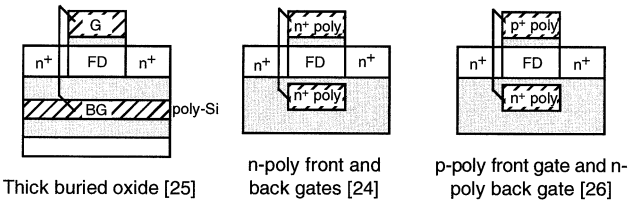



**Fig. 6** Schematic cross-sections of examples of DG MOSFETs.

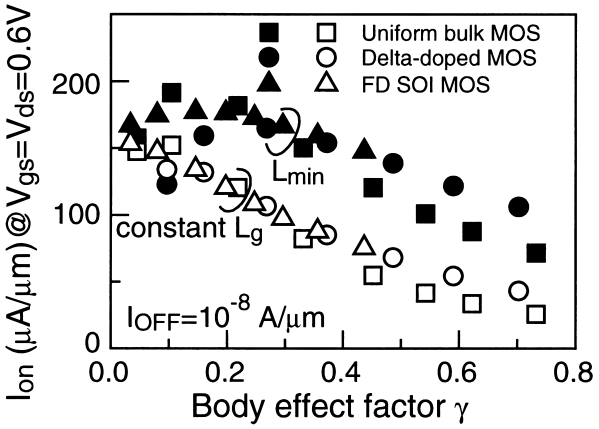



**Fig. 7** Simulated current drive of uniform bulk MOSFET, delta-doped MOSFET, and FD SOI MOSFET with fixed back-bias as a function of body effect factor. The supply voltage is 0.6 V. Gate oxide thickness is 3 nm and junction depth is 15 nm. The off-current is set to a constant value of $10^{-8}$ A/$\mu$m by adjusting the gate workfunction. Two cases of constant $L_g$ (0.2 $\mu$m) and $L_g = L_{min}$ are shown. $L_{min}$ is defined as gate length at which the threshold voltage roll-off is 0.1 V.

short channel effect is worse. The SOI thickness should be thin to suppress the short channel effect. Although some devices have very thin buried oxide to suppress the short channel effect, the devices show large subthreshold swing and current drive is degraded. Some devices are also focused on the control of threshold voltage [23] and variable threshold using two back-biases [3], [4].

### 3.5 Variations of DG SOI MOSFETs

Figure 6 shows examples of DG SOI MOSFETs [24]–[26]. The main interest in DG MOS lies in the enhanced current drive, ideal subthreshold swing, and suppression of short channel effect. DG MOS has a different operation principle and higher current drive than DTMOS, because DG MOS has two conducting channels in a front interface and a back interface. The discussions and equations in Sect. 2 are not necessarily valid in DG SOI, and the body effect factor bears less meaning. Moreover, it is still very hard to fabricate self-aligned DG structures [24], [27]. This structure is eliminated in the following discussion in this paper. Detailed analysis has been reported in Ref. [19].

## 4. Characteristics of a Fixed Back-Bias and Dynamic Back-Bias Configurations

In this section, the characteristics of classified device structures are calculated by a two-dimensional device simulator [28]. It is shown that the basic characteristics are primarily determined by the body effect factor $\gamma$, irrespective of device structures. It is found that in order to obtain higher current drive, the body effect factor should be small in a fixed back-bias while it should be as high as possible in a DTMOS configuration.

### 4.1 Limitation of MOSFETs with a Fixed Back-Bias

Figure 7 shows the current drive of MOSFETs with fixed back-bias as a function of body effect factor. The off-current is set to a constant value of $10^{-8}$ A/$\mu$m by adjusting the gate workfunction. Uniform bulk MOS, delta-doped MOS, and FD SOI MOS are shown, where well impurity concentration, thickness of low concentration layer, and buried oxide thickness are varied, respectively, to change the body effect factor. Two cases are considered. One is the case where gate length $L_g$ is constant. The other is where the short channel effect is considered and $L_g$ is set to $L_{min}$ at which the threshold voltage roll-off is 0.1 V.

It should be noted that the simulated data of current drive do not so much depend on device structures but almost only on body effect factor. This result indicates that current drive and short channel effect are primarily decided by the body effect factor. The further reduction of current drive observed in uniform bulk MOS at large body effect factor is caused by the enhanced impurity scattering due to high impurity concentration at the surface. When channel length is constant, current drive monotonously decreases with increasing body effect factor, as is qualitatively explained in Sect. 2.

When $L_g$ is set to $L_{min}$, there is a maximum value of the current drive. In a device with very small body effect factor, current drive is small because $L_{min}$ is long due to severe short channel effect. As body effect factor increases, $L_{min}$ become shorter and current drive increases. When body effect factor increases further, the effects of a decrease in $L_{min}$ and a degradation of current drive due to large body effect are balanced, and finally current drive is degraded at a higher body effect factor. This behavior and explanation are basically the same as the discussion in Ref. [29].

These results expose the limitation of a MOSFET with a fixed back-bias. When gate length is constant, current drive can not exceed that of a device with $\gamma = 0$. Even if the short channel effect is suppressed and gate length is reduced, the large increase in current drive is not expected and the current drive becomes even worse with increasing the body effect factor. In order to at-

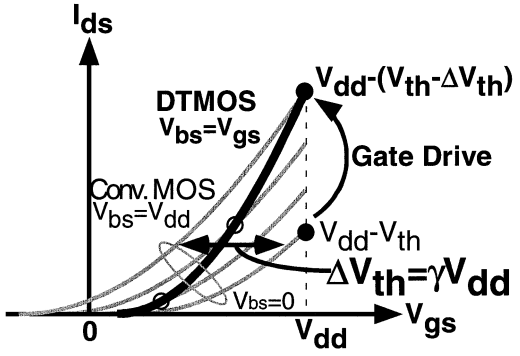



**Fig. 8** Schematic characteristics of DTMOS.

tain higher current drive with fixed off-current at very low supply voltage, a dynamic control of threshold voltage by back-bias is strongly required.

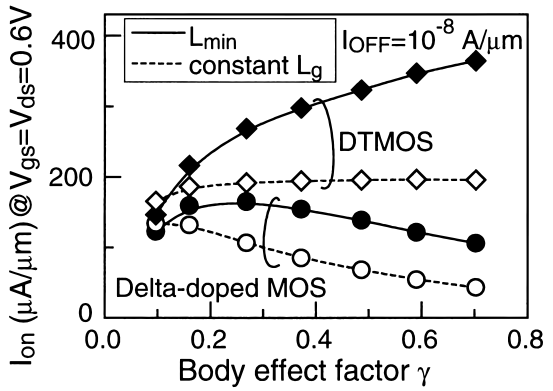
### 4.2 Operation Principle of DTMOS

Figure 8 shows schematic characteristics of DTMOS. Since the body is tied to the gate electrode, threshold voltage decreases due to the body effect as the gate voltage increases. When the gate voltage is $V_{\rm dd}$, the threshold voltage shift is given by

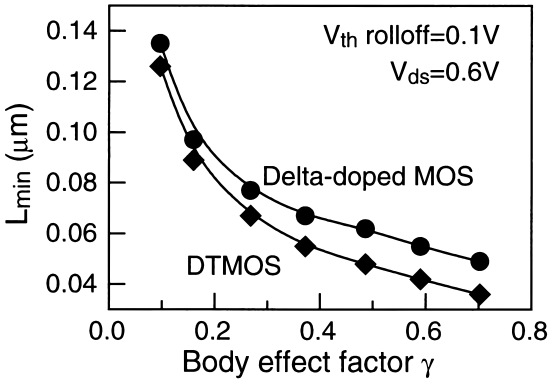
$$\Delta V_{\rm th} = \gamma V_{\rm dd} \tag{7}$$

and the gate drive increases by $\gamma V_{\rm dd}$. In order to increase the current drive, therefore, the body effect factor should be as high as possible. Since the body potential follows the gate potential, the vertical field is low and the mobility degradation is suppressed. The circuit speed degradation in the serially stacked MOSFETs is also avoided. Even when body effect factor is large, subthreshold swing is always ideal (60 mV/dec).

Figure 9 (a) shows simulated current drive of DTMOS as a function of body effect factor. Delta-doped impurity profile is assumed. Current drive of delta-doped MOS with a fixed back-bias is also shown in the figure for comparison. Figures 9 (b) and (c) show $L_{\rm min}$ and subthreshold factor as a function of body effect factor. It is clearly shown that the current drive is drastically improved by connecting the body to the gate. In DTMOS with a constant $L_{\rm g}$, current drive is almost constant, because the improvement by large body effect factor and the degradation by higher vertical electric field are balanced. On the other hand, current drive monotonously increases with increasing body effect factor when $L_{\rm g} = L_{\rm min}$, because the $L_{\rm min}$ decreases with increasing body effect factor due to suppressed short channel effect as shown in Fig. 9(b). These results clearly demonstrate that trade-offs in a device with a fixed back-bias are solved in the DTMOS configuration and that both the high current drive and small off-current can be achieved in DTMOS with a large body effect factor.




(a)

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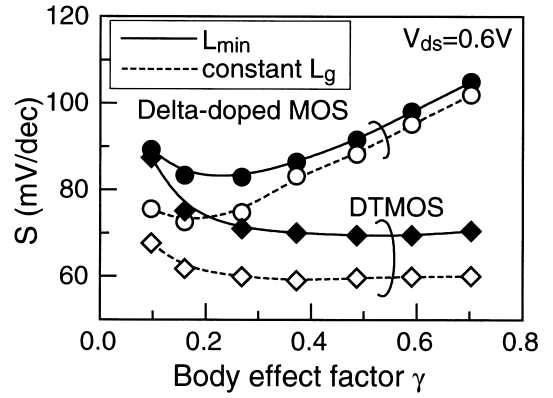


(c)

**Fig. 9** (a) Simulated current drive of DTMOS as a function of body effect factor. An impurity profile of delta-doping is assumed. The supply voltage is 0.6 V. Gate oxide thickness is 3 nm and junction depth is 15 nm. The off-current is set to a constant value of $10^{-8}$ A/$\mu$m by adjusting the gate workfunction. Two cases of constant $L_{\rm g}$ (0.2 $\mu$m) and $L_{\rm g} = L_{\rm min}$ are shown. Delta-doped MOS with a fixed back-bias is also shown. (b) $L_{\rm min}$ and (c) subthreshold factor as a function of body effect factor.

## 5. DTMOS with a Very High Body Effect Factor

In this section, a new DTMOS, EIB-DTMOS, with a very high body effect factor at low threshold voltage

is proposed. The high performance of EIB-DTMOS is demonstrated.

### 5.1 Threshold Voltage and Body Effect Factor

A very high body effect factor is easily realized in uniformly doped DTMOS with a very high impurity concentration. However, there is a remaining trade-off in DTMOS: the relationship between threshold voltage and body effect factor. Since the operation voltage of DTMOS should be low due to forwarded pn junction current, threshold voltage should also be low in DTMOS. In uniformly doped DTMOS, body effect factor is given by

$$\gamma \cong 3\frac{t_{\rm ox}}{l_{\rm d}} \propto t_{\rm ox}\sqrt{N_{\rm A}} \tag{8}$$

where $N_{\rm A}$ is impurity concentration. This equation indicates that as body effect factor increases, threshold voltage also increases when the gate work function is fixed. A large body effect factor with low threshold voltage is hard to attain in uniformly doped DTMOS. The body effect factor in previously reported DTMOS is around 0.2–0.3, because threshold voltage is set to a small value [6], [8]. Then, threshold voltage shift at the supply voltage of 0.5 V is about 0.1–0.15 V from Eq. (7) and the improvement of current drive is not sufficient.

### 5.2 EIB-DTMOS

We have proposed EIB-DTMOS [12], [13] as a solution to this trade-off. Figure 10 shows a schematic structure of EIB-DTMOS. The advantage of EIB-DTMOS is that body effect factor and threshold voltage are separately determined. The body effect is determined by the SOI thickness while threshold voltage is determined by the doping concentration and its polarity in the body. When the body has the opposite polarity as source and drain (i.e. the body is p-type in NMOS), it acts as an inversion mode where threshold voltage is higher than the intrinsic body. On the other hand, when the body has the same polarity as source and drain, it acts as an accumulation mode where threshold voltage is lower.

Figure 11 shows the relation between body effect factor and threshold voltage in uniformly doped DTMOS and an inversion mode EIB-DTMOS with a slightly B-doped body region. In both devices, threshold voltage increases with increasing body effect factor. At a fixed threshold voltage, however, EIB-DTMOS has about two times as large body effect factor as uniformly doped DTMOS. This is because the depletion layer width of EIB-DTMOS is half of that of uniformly doped DTMOS [13]. An experimental datum of inversion mode EIB-DTMOS is also shown in the figure [13]. The experiment and simulation are in good agreement.

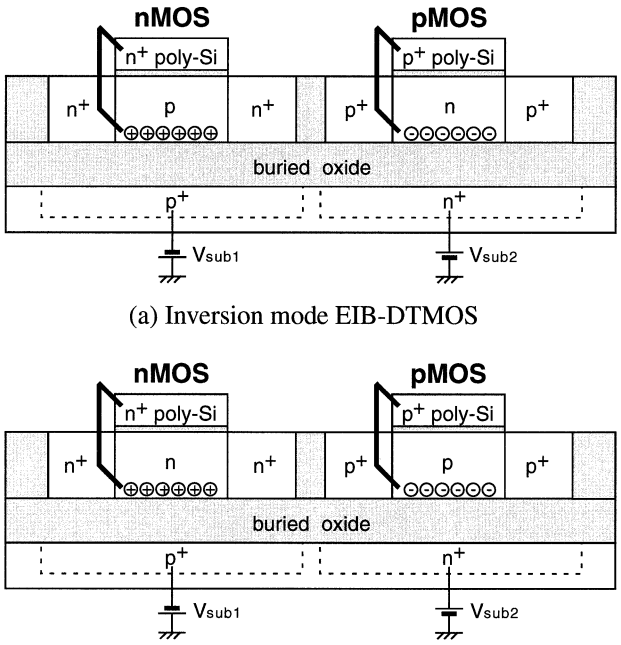


**Fig. 10** Schematic cross-sections of EIB-DTMOS. Inversion mode EIB-DTMOS and accumulation mode EIB-DTMOS are shown. Different substrate biases, $V_{\rm sub1}$ and $V_{\rm sub2}$, are applied to NMOS and PMOS, respectively. $V_{\rm sub1}$ and $V_{\rm sub2}$ are supplied from the front via contact holes through the buried oxide.

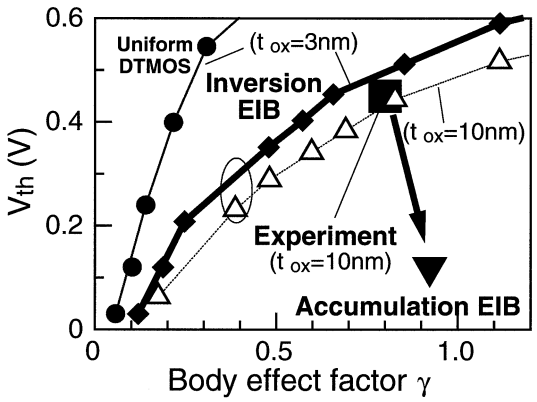


**Fig. 11** Relation between body effect factor and threshold voltage obtained by simulation in DTMOS. Uniformly doped DTMOS and an inversion mode EIB-DTMOS with a slightly B-doped body region are shown. An experimental datum is plotted. An accumulation mode EIB-DTMOS is also plotted.

### 5.3 Accumulation Mode EIB-DTMOS

Even in the inversion mode EIB-DTMOS, a large body effect factor is not achieved in low threshold voltage and one can not take full advantage of high current drive of DTMOS. This problem is solved by an accumulation mode EIB-DTMOS [12]. When the impurity concentration in the body (the same polarity as source/drain)

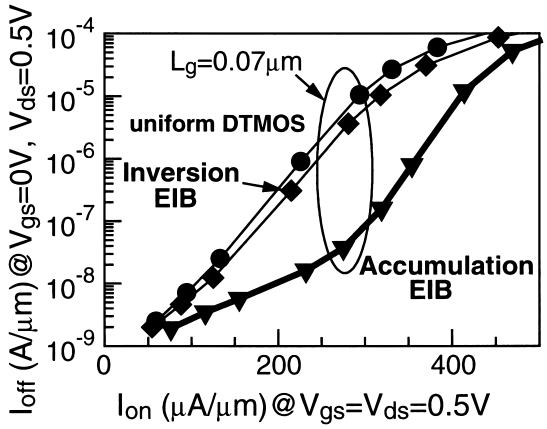


**Fig. 12** Relation between current drive and off-current in uniformly doped DTMOS, inversion mode DTMOS, and accumulation mode DTMOS. Threshold voltage is fixed at $L_g = 0.5$ $\mu$m, and $L_g$ is varied. Gate oxide thickness is 3 nm and junction depth is 15 nm.

is high enough, threshold voltage can be reduced down to 0.1 V, while the body effect factor is set to as high as 0.9 with very thin SOI thickness, as shown in Fig. 11. Figure 12 shows the relation between current drive and off-current in uniformly doped DTMOS, inversion mode DTMOS, and accumulation mode DTMOS [12]. Thanks to very large body effect factor and suppressed short channel effect due to thin SOI thickness, the accumulation mode EIB-DTMOS shows high current drive at very low off-current.

The superior ac characteristics of accumulation mode EIB-DTMOS have been also confirmed by mixed-mode device simulation [12]. Since DTMOS generally has additional gate capacitance between body and channel and parasitic capacitance between body and source/drain, the improvement of gate delay is more enhanced when load capacitance is larger. One of the disadvantages of DTMOS using SOI is high body resistance by which the body potential does not follow the gate voltage, resulting in degradation of gate delay. To avoid this effect, bulk DTMOS with smaller well resistance has been proposed [8]–[10]. In EIB-DTMOS, since the body is electrically formed, the body resistance is higher than uniformly doped DTMOS and bulk DTMOS. This problem can be resolved by parallel connection of divided MOSFETs to achieve smaller ratio of channel width to channel length [12]. Detailed analysis of body resistance in EIB-DTMOS will be reported elsewhere [30].

## 6. Conclusions

Characteristics of low voltage MOSFETs are reviewed from the viewpoint of back-gate structures and body effect factor. Previously reported device structures are classified into four categories and the limitation of a MOSFET with a fixed back-bias is shown. It is also shown that in dynamic threshold MOSFET where the body is tied to the gate, the improvement of current drive is more enhanced with increasing body effect factor. For a very large body effect factor at low threshold voltage, a new dynamic threshold MOSFET with electrically induced body using thin SOI layer is proposed and its superiority is demonstrated.

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**Toshiro Hiramoto** received the B.S., M.S. and Ph.D. degrees in electronics from University of Tokyo in 1984, 1986, and 1989, respectively. In 1989, he joined Device Development Center, Hitachi Ltd., Ome, Japan, where he was engaged in device and circuit design of ultra-fast BiCMOS SRAM. Since 1994, he has been an Associate Professor in Institute of Industrial Science, University of Tokyo, Tokyo, Japan. He has been also an Associate Professor in VLSI Design and Education Center, Univerisity of Tokyo, Tokyo, Japan since 1996. His research interests include low power device design, sub-100 nm CMOS devices, SOI MOSFETs, silicon single electron devices, and quantum effects in scaled MOSFETs.

**Makoto Takamiya** was born in Hyogo, Japan, in 1973. He received the B.S. and M.S. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1995 and 1997, and is now working towards the Ph.D. degree in Institute of Industrial Science, University of Tokyo. He has been engaged in the research of low power SOI CMOS devices. His research interests include scaling of MOSFET's into sub- 0.1 $\mu$m region and ultra low-voltage MOSFET's. He received the Young Researcher Award of 1999 International Conference on Solid State Devices and Materials.