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Optimum Conditions of Body Effect Factor and Substrate Bias in Variable Threshold Voltage MOSFETs

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The effects of body effect factor (γ) and substrate bias (V_{bs}) in a variable threshold voltage metal oxide semiconductor field effect transistor (VTMOS) have been systematically examined by device simulation. The characteristics of a VTMOS are significantly affected by the value of γ and the V_{bs} difference (ΔV_{bs}) between the active mode and the standby mode. Optimal γ and ΔV_{bs} to obtain higher on-current in the active mode and lower off-current in the standby mode are derived. When off-current in the active mode is limited, a larger ΔV_{bs} and smaller γ are preferable to obtain a higher drive current. When γ is fixed, $|\Delta V_{bs}|$ should be as large as the breakdown and leakage current permits. When ΔV_{bs} is fixed for some reason, such as breakdown, the optimum γ depends on the relationship between ΔV_{bs} and V_{dd}: γ should be larger when a large $|\Delta V_{bs}|$ can be applied, while it should be smaller when the $|\Delta V_{bs}|$ is small. The scalability of VTMOS is also discussed and it is found that channel engineering is strongly required in a scaled VTMOS. These results will greatly help in designing ultra-low power VTMOS VLSIs, and the VTMOS could be expected to survive in the 50 nm generation depending on the scaling scenario and applications.

KEYWORDS: body effect, variable threshold voltage metal oxide semiconductor field effect transistor (VTMOS), substrate bias, low power, active mode, standby mode, channel engineering

1. Introduction

The variable threshold voltage metal oxide semiconductor field effect transistor (VTMOS) has recently attracted much attention for ultra-low power very large scale integration (VLSI) applications at low supply voltage (V_{dd}).[1–3] Utilizing the body effect, the substrate bias (V_{bs}) is controlled to shift the threshold voltage (V_{th}), and a high V_{th} in the stand-by mode and low V_{th} in the active mode are obtained. V_{th} fluctuations between chips are also suppressed by V_{bs} control.[1)] The V_{th} shift (ΔV_{th}) is given by

$$\Delta V_{th} = \gamma |\Delta V_{bs}| = \gamma |V_{bs}(s) - V_{bs}(a)|, \quad (1)$$

where γ is the body effect factor, ΔV_{bs} the difference of substrate bias between the active mode and the standby mode, $V_{bs}(s)$ the substrate bias in the standby mode, and $V_{bs}(a)$ the substrate bias in the active mode. Therefore, γ and ΔV_{bs} are the most important device parameters in relation to VTMOS and their optimization is essential to take full advantage of VTMOS. However, no study has previously been made on the optimum conditions of γ and ΔV_{bs}.

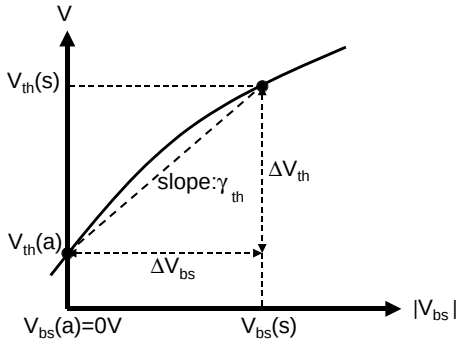
In this study, the dependence of VTMOS performance on γ and ΔV_{bs} is systematically investigated by device simulation and the optimum conditions are discussed. It is found that ΔV_{bs} should be as large as possible, while the optimum value of γ depends on the relationship between ΔV_{bs} and V_{dd}. The scalability of VTMOS is also discussed. It is found that engineering of the doping profiles in the channel region (channel engineering)[4)] is strongly required in scaled VTMOS.

2. Simulation and Results

2.1 Definition of the body effect factor

In this study, the body effect factor γ is defined as

$$\gamma \equiv \frac{|\Delta V_{th}|}{|\Delta V_{bs}|} = \frac{|V_{th}(s) - V_{th}(a)|}{|V_{bs}(s) - V_{bs}(a)|} = \frac{C_d}{C_{ox}}, \quad (2)$$



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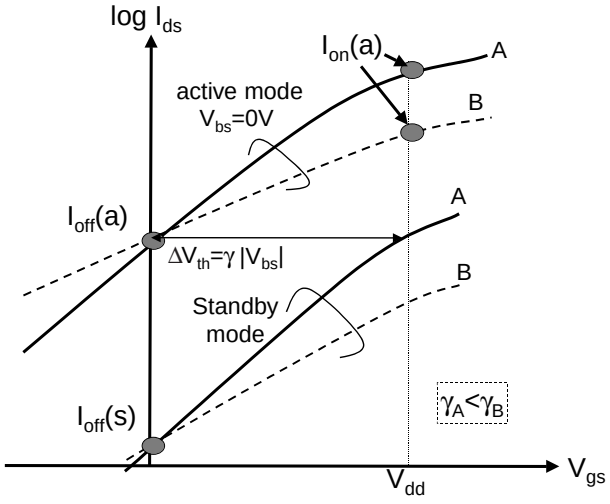

(b)

Fig. 1. (a) A schematic of the relationship among ΔV_{th}, ΔV_{bs} and γ in a value of VTMOS. γ is given by the slope of $\Delta V_{th}/\Delta V_{bs}$. (b) Schematic of the characteristics of a VTMOS with different at γ (device A has smaller γ than device B). The off-current in the standby mode (I_{off}(s)) is set constant at 10^{-13} A/μm. The off-current in the active mode (I_{off}(a)) is also set to be the same in this figure. Device A has higher on-current (I_{on}(a)) due to the smaller S factor and higher mobility but requires large $|\Delta V_{bs}|$ to attain low I_{off}(s) due to the small γ.

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where V_{th}(s) and V_{th}(a) are the threshold voltage in the standby and active modes, respectively, C_d is the depletion capacitance and C_{ox} is the gate oxide capacitance, so that ΔV_{th} is given by eq. (1).[5] Generally, ΔV_{th} is dependent on the square root of ΔV_{bs} and the body effect factor is given by[6]

$$\gamma' = \frac{\sqrt{2q\varepsilon N_A}}{C_{ox}}, \tag{3}$$

where q is the electric charge, ε is the permittivity in silicon and N_A is the channel doping concentration. However, γ' in eq. (3) is valid only in MOSFETs with uniform channel concentration. Moreover, the relation between ΔV_{th} and γ' is not clear. Therefore, we adopted the definition of eq. (2). Figure 1(a) shows a schematic of the relationship among γ, ΔV_{bs}, and ΔV_{th}. γ is given by a slope of $\Delta V_{th}/\Delta V_{bs}$. Please note that the value of γ changes with ΔV_{bs} when ΔV_{th} is not proportional to ΔV_{bs} as shown in the figure. However, eq. (1) is always valid when the definition of eq. (2) is used.

On the other hand, subthreshold swing (S factor) is given at room temperature by

$$S = 60\left(1 + \frac{C_d}{C_{ox}}\right)[\text{mV/dec}]. \tag{4}$$

Then, the relation between γ and S is given from eqs. (2) and (4) as

$$S = 60(1+\gamma)[\text{mV/dec}]. \tag{5}$$

This equation indicates that a device with larger γ has a larger S factor.

2.2 Qualitative predictions

Figure 1(b) shows a schematic of the characteristics of VTMOS's with different value of γ. Device A has a smaller γ than device B. When the off-current in the standby mode (I_{off}(s)) is the same for the two devices, device A requires a larger $|\Delta V_{bs}|$ to attain a certain ΔV_{th} due to smaller γ than device B. However, device A with a smaller γ will have a higher on-current (I_{on}(a)) as shown in Fig. 1(b). This is because device A has a steeper S swing (hence low V_{th}) and higher mobility due to the weaker vertical electric field. Therefore, the optimal value of γ is not clear from this the qualitative discussion alone. More detailed discussion based on device simulation[7] is presented in the following subsections.

2.3 Simulated device structures

Figure 2 shows a schematic of the device structures used in the simulation. Figure 2(a) shows the uniformly doped MOSFET (uniform MOS) where the channel doping profile is uniform. Uniform MOS generally has a small γ due to the large depletion layer width. Figure 2(c) shows the delta-doped MOSFET (delta MOS) where the channel doping profile is step-like as shown in figure.[8] Delta MOS has a γ twice as large as uniform MOS, because the depletion layer width of delta MOS is half of that of the uniform MOS at a fixed V_{th}.[8] On the other hand, the state-of-the-art MOSFETs with high

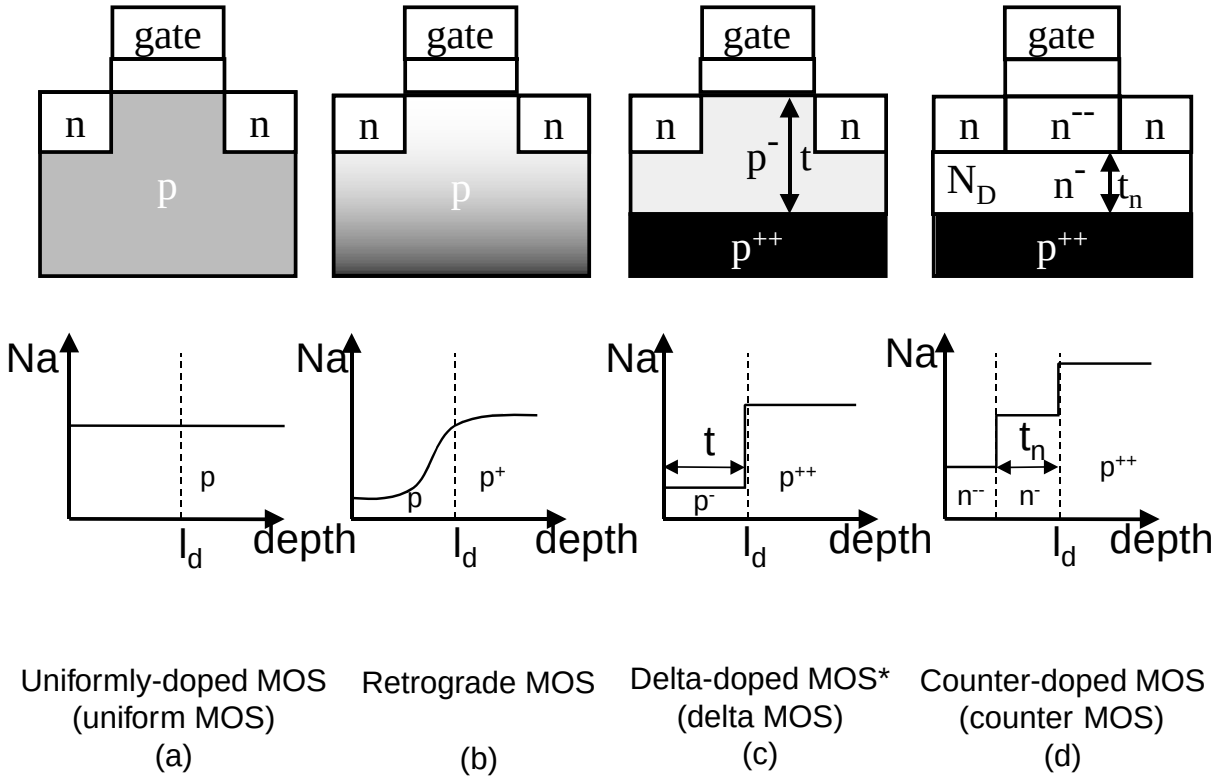
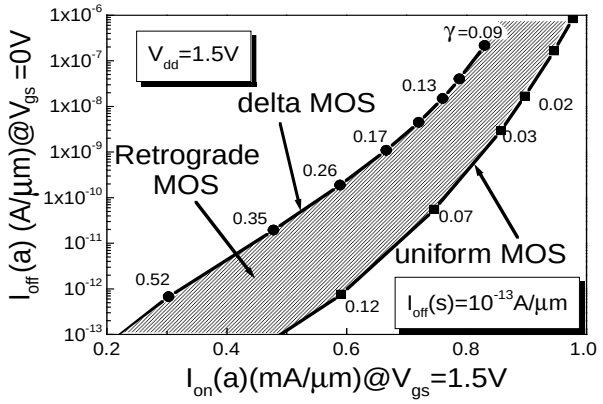


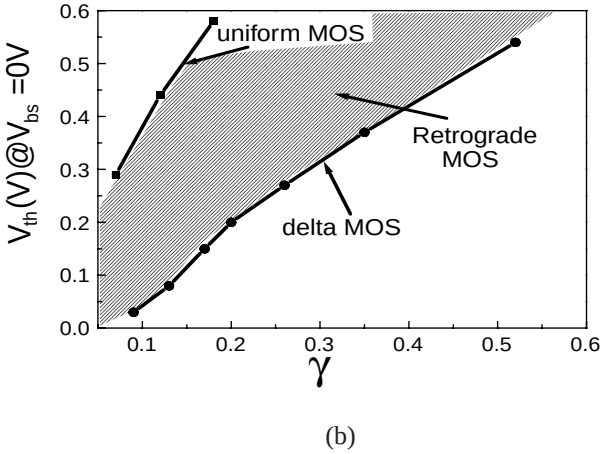
Fig. 2. Schematic of the device structures used in the device simulation. Gate length is 0.18 μm, gate oxide thickness is 3 nm, source/drain junction depth is 50 nm, and supply voltage is 1.5 V (a) Uniformly doped MOSFET (uniform MOS), in which the channel concentration is varied to change γ and V_{th}. (b) Retrograde channel MOSFET with a low doping concentration at the surface and a high concentration in depth (retrograde MOS). Although this structure is not simulated in this study, the characteristics are intermediate between those of uniform MOS and delta MOS. (c) Delta-doped MOSFET[8] (delta MOS), in which the thickness (t) of the low concentration layer is varied to vary γ and V_{th}. (d) Counter-doped MOSFET (counter MOS), in which the thickness (tn) and concentration (ND) of the middle layer is varied to change γ and V_{th} over a wide range.

short channel effect immunity have a gradual channel profile with a low concentration at the surface and high concentration in depth due to the channel engineering as shown in Fig. 2(b), which is generally referred to as a MOSFET with a retrograde channel profile (retrograde MOS).[9] Although the characteristics of a retrograde MOS depend on the actual channel profile, they are intermediate between those of a uniform MOS and delta MOS.[5,9] Therefore, we first simulated the characteristics of these two extreme device structures: uniform MOS and delta MOS. In uniform MOS, the channel concentration is varied to change the value of γ and V_{th}. In delta MOS, the thickness of the low concentration layer (t) is varied to change the value of γ and V_{th}.

Figure 3(a) shows the relation between the off-current in the active mode (I_{off}(a)) and I_{on}(a), and Figure 3(b) shows the relation between V_{th} and γ of the two devices. The numbers indicated in Fig. 3(a) are the values of γ. The device parameters used are based on the 180-nm technology node in the International Technology Roadmap for Semiconductors (ITRS).[10] Uniform MOS has a higher I_{on}(a) but the required $|\Delta V_{bs}|$ would be extremely high due to the very small γ. The retrograde MOS covers the area between the two lines. It is suggested from Fig. 3(b) that the covered range of γ and V_{th} is limited when only uniform MOS and delta MOS are simulated. In order to investigate the effect of γ systematically over a wider range of I_{on}(a) and I_{off}(a), therefore, counter-doped MOSFETs (counter MOS) are also simulated. Figure 2(d) shows the structure of the counter MOS where the polarity of channel doping is the opposite near the surface. The counter MOS has a lower V_{th} (higher I_{off}(a)) than uniform MOS and delta MOS due to the counter-doping, and a larger γ at a fixed V_{th}. γ is varied over a wide range by changing the thickness of the counter-doped layer and V_{th} is varied by changing the concentration of the counter doped layer.



(a)



(b)

Fig. 3. (a) Relation between I_{off}(a) and I_{on}(a) in a uniform MOS and delta MOS. I_{off}(s) of each device is fixed at 10^{-13} A/μm. The value of γ each device are shown. (b) Relation between V_{th} and γ in a uniform MOS and delta MOS. The channel-engineered MOSFETs, such as retrograde MOS, cover the area between the two lines. $|V_{bs}|$ and γ cannot be varied widely by using only uniform, retrograde or delta MOS.

2.4 Simulation conditions and method

The off-current in the standby mode (I_{off}(s)) is set at 10^{-13} A/μm, and the on-current in the active mode (I_{on}(a)) is compared in this study. The same results are obtained when I_{on}(a) is fixed and I_{off}(s) is compared. V_{bs} in the active mode (V_{bs}(a)) is set to 0 V in the simulation, since V_{bs}(a) is usually almost 0 V in the VTMOS.[1] Therefore, ΔV_{bs} corresponds to V_{bs} in the standby mode (V_{bs}(s)) in this study. The I–V characteristics are simulated for a device parameter set at $V_{bs} = 0$ (active mode), and the on-current (I_{on}(a)), off-current (I_{off}(a)), and V_{th} in the active mode are derived. Then, V_{bs} is applied (the standby mode), and ΔV_{bs} is obtained so that I_{off}(s) is 10^{-13} A/μm in the standby mode. Then, ΔV_{th} is derived from V_{th}'s in the active and standby modes, and γ is obtained from eq. (2). The simulation is carried out for various device parameters. I_{on}(a), I_{off}(a), γ, ΔV_{bs} are derived for each parameter set by the above-mentioned method. Then, I_{on}(a) and I_{off}(a) of each device are plotted in a I_{off}(a)-I_{on}(a) plane, and contour lines of γ and ΔV_{bs} are obtained.

2.5 Simulated results

Figure 4 shows the device simulation results. I_{off}(s) is fixed at 10^{-13} A/μm. This figure shows the contour lines of V_{bs} (solid lines) and γ (dashed lines) as a function of I_{off}(a) and I_{on}(a). Since this figure is rather complicated, we discuss the results in the following three boundary conditions.

2.5.1 Constant I_{off}(a)

In the first boundary condition, I_{off}(a) is set at a constant value in addition to the constant I_{off}(s). When V_{th} is extremely

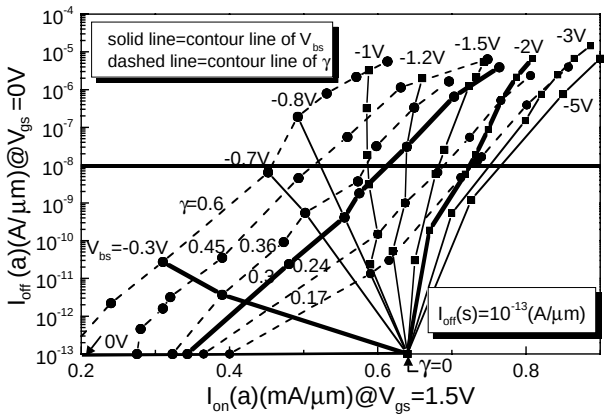


Fig. 4. Contour lines of V_{bs} (solid lines) and γ (dashed lines) in a VTMOS as a function of I_{off}(a) and I_{on}(a). I_{off}(s) is set at 10^{-13} (A/μm). I_{off}(a) $= 10^{-8}$ A/μm under the first boundary condition (constant I_{off}(a)), $\gamma = 0.3$ under the second boundary condition (constant γ), and $\Delta V_{bs} = -2$ V and -0.3 V under the third boundary condition (constant ΔV_{bs}) are shown by bold lines.

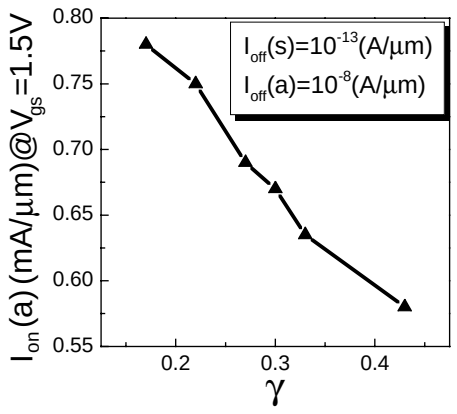
low, I_{off}(a) becomes very large and the circuits consume a lot of power and sometimes do not work properly.[11,12] Therefore, I_{off}(a) should be limited to a certain maximum value. This condition roughly corresponds to a constant V_{th}. Figure 5 shows the simulation results of VTMOS under the condition of fixed I_{off}(s) and I_{off}(a). Figure 5(a) shows the relation of I_{on}(a) and γ to obtain a constant I_{off}(s) of 10^{-13} A/μm and constant I_{off}(a) of 10^{-8} A/μm, and Figure 5(b) shows the ΔV_{bs} dependence of I_{on}(a) under this condition. This condition is shown by a horizontal line in Fig. 4. Under this condition, $|\Delta V_{bs}|$ should be large and a device with relatively small γ is preferable, as shown in Fig. 5.

2.5.2 Constant γ

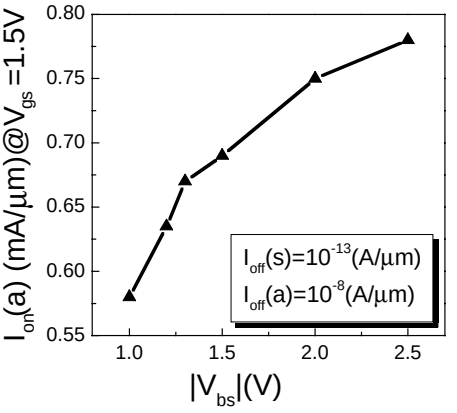
The second boundary condition is a constant γ. When the device is fixed, γ is also fixed. The relation between I_{off}(a) and I_{on}(a) is expressed in the corresponding contour line of γ, as shown in Fig. 4 with $\gamma = 0.3$ as an example. It is evident from the contour lines that $|\Delta V_{bs}|$ should be as large as possible to achieve a higher I_{on}(a), although I_{off}(a) also increases. In actual devices, $|\Delta V_{bs}|$ is usually limited by junction leakage current or junciton breakdown. Under this condition, $|\Delta V_{bs}|$ should be set to a value as large as is permitted by the leakage or breakdown.

2.5.3 Constant $|\Delta V_{bs}|$

The third boundary condition is a constant $|\Delta V_{bs}|$. As mentioned above, $|\Delta V_{bs}|$ is limited by leakage current or breakdown of the pn junctions and the maximum $|\Delta V_{bs}|$ strongly depends on the device structures and process. Please note that all the contour lines of ΔV_{bs} converge to one point in Fig. 4. This point corresponds to the device with $\gamma = 0$. The line of $|\Delta V_{bs}| = 0$ V is also shown in Fig. 4. When $|\Delta V_{bs}| = 0$ V, I_{off}(a) equals to I_{off}(s) and only I_{on}(a) changes because $\Delta V_{th} = 0$ V. It should be also noted that at a certain value of ΔV_{bs}, I_{on}(a) becomes constant regardless of the value of γ, as shown in Fig. 4. This ΔV_{bs} is defined as V_o. In this case, V_o is about -1.2 V. When $|\Delta V_{bs}|$ is larger than $|V_o|$, for example $\Delta V_{bs} = -2$ V, a larger I_{on}(a) is obtained for larger γ. On the other hand, when $|\Delta V_{bs}|$ is smaller than $|V_o|$, for example $\Delta V_{bs} = -0.3$ V, a larger I_{on}(a) is obtained for a smaller γ. Figure 6 shows the same results in a different way, where the contour lines of I_{on}(a) are shown as a function of ΔV_{bs} and γ. The slope of the contour lines changes from positive to negative at $|\Delta V_{bs}| = |V_o|$. When $|\Delta V_{bs}|$ is larger than $|V_o|$, the slope is negative. Thus, a higher I_{on}(a) is achieved for larger γ. However, when $|V_{bs}|$ is smaller than $|V_o|$, the result is the opposite.



(a)



(b)

Fig. 5. Simulation results for the first boundary condition: constant I_{off}(a). I_{off}(s) is also constant (10^{-13} A/μm). (a) Relation between I_{on}(a) and γ. (b) Relation between I_{on}(a) and $|\Delta V_{bs}|$. To obtain larger I_{on}(a), γ should be small and $|\Delta V_{bs}|$ should be large under the condition of constant I_{off}(a).

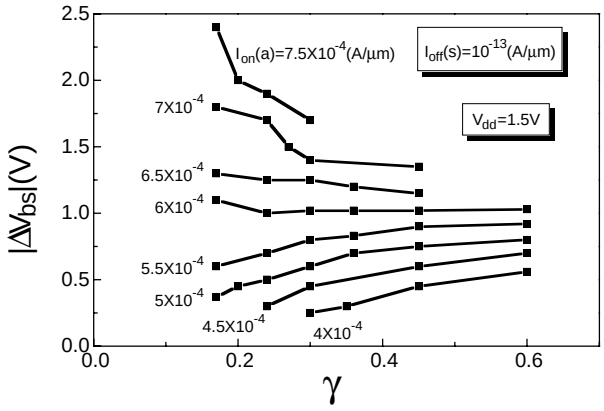


Fig. 6. Contour lines of I_{on}(a) in a VTMOS as a function of $|\Delta V_{bs}|$ and γ. The V_{dd} is 1.5 V. When $|\Delta V_{bs}|$ is larger than 1.2 V, a higher I_{on}(a) is obtained for larger γ. On the other hand, when $|\Delta V_{bs}|$ is less than 1.2 V, higher I_{on}(a) is obtained for smaller γ.

2.5.4 Optimum condition of γ

This interesting result is well explained qualitatively as follows. Figure 7 shows a schematic of the relation between I_{on}(a) and γ. I_{off}(s) is fixed. In a normal MOSFET ($V_{bs} = 0$ V), I_{on}(a) decreases with increasing γ due to degradation of the S factor and smaller mobility.[5] The slope of the I_{on}(a)-γ curve is negative. When V_{bs} is applied, I_{on}(a) increases and the increase of I_{on}(a) is larger for larger γ. Therefore, when V_{bs} is sufficiently large, I_{on}(a) becomes larger for larger γ and the slope of the I_{on}(a)-γ curve becomes positive. The value of $|V_o|$ is slightly smaller than that of V_{dd} as shown in Fig. 6. The reason is discussed qualitatively in the following.

Here, let us consider a device with $\Delta V_{bs} = -V_{dd}$ and a device with $\Delta V_{bs} = V_{dd}$. Note that the device with $\Delta V_{bs} = V_{dd}$ is the dynamic-threshold MOS (DTMOS) where the gate is connected to the body.[13] Although the V_{dd} of the DTMOS should be lower than the forward voltage of the pn junction, it has been reported that the I_{on}(a) of a DTMOS increases with increasing γ.[5,14] On the other hand, the device with $\Delta V_{bs} = -V_{dd}$ would show almost the same characteristeics as

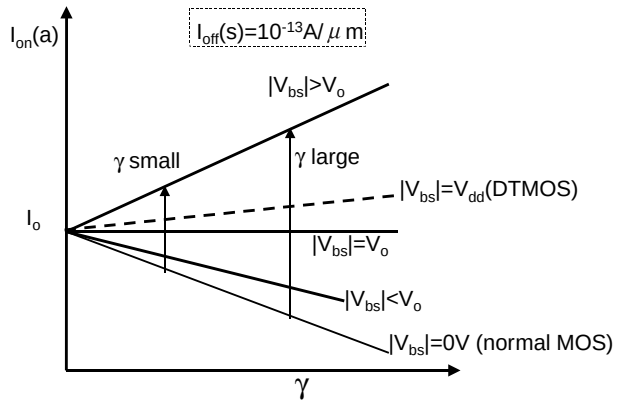


Fig. 7. Schematic of the relationship between I_{on}(a) and γ that qualitatively explains the optimum condition of γ under the condition of constant $|\Delta V_{bs}|$. Four solid lines show the VTMOS. The dashed line shows the DTMOS. Since a larger I_{on}(a) is obtained for larger γ in DTMOS, $|V_o|$ is slightly smaller than Vdd. When $|\Delta V_{bs}| > |V_o|$, a larger I_{on}(a) is obtained larger γ, while when $|\Delta V_{bs}| < |V_o|$, a larger I_{on}(a) is obtained for smaller γ.

this DTMOS when the V_{bs} dependence of γ is linear. Therefore, the device with $\Delta V_{bs} = -V_{dd}$ roughly corresponds to the dashed line in Fig. 7. The horizontal line in Fig. 7 corresponds to $V_{bs} = V_o$. Therefore, $|V_o|$ is slightly smaller than V_{dd}. As shown in this figure, I_{on}(a) becomes larger with increasing γ when $|\Delta V_{bs}|$ is larger than $|V_o|$, while I_{on}(a) becomes smaller with increasing γ when $|\Delta V_{bs}|$ is smaller than $|V_o|$.

3. Scalability of VTMOS

One of the major concerns about regarding a VTMOS is its scalability.[15] We discuss the scalability of VTMOS's in this section. The device parameters in each technology generation are mainly based on ITRS.[10] Two scaling scenarios of VTMOS's are considered in this study: V_{th} in the active mode (V_{th}(a)) is scaled like other device parameters in the first scenario, while V_{th}(a) is kept constant in the second one.

3.1 A Scaling scenario with scaled V_{th}

In the first scaling scenario, V_{th}(a) is scaled. The other device parameters are also scaled based on ITRS.[10] Figure 8(a) shows the variation of γ with the technology generation. The supply voltage V_{dd} and V_{th}(a) in each generation are shown in the figure. The channel-engineered MOS, such as retrograde channel MOS, is just between the two lines (the lines of uniform MOS and delta MOS). Figure 8(a) indicates that γ becomes larger by the channel engineering. However, in this scenario, γ decreases as the device is scaled.

Figure 8(b) shows the variation of ΔV_{bs} that is required to obtain $I_{off}(s) = 10^{-13}$ A/μm. ΔV_{bs} rapidly increases in uniform MOS, as also in delta MOS. This is a serious problem because the breakdown voltage would decrease as the device is scaled. It must be noted that the required V_{bs} is greatly suppressed by the channel engineering.

The advantage of channel-engineered MOS is not only in the large γ but also the V_{bs} dependence of γ. Figure 9 shows V_{th} as a function of V_{bs} in a uniform MOS and delta MOS. In the uniform MOS, ΔV_{th} is proportional to the square root of V_{bs}, and the effect of back bias is not effective. In the delta MOS, on the other hand, ΔV_{th} is almost proportional to V_{bs}.

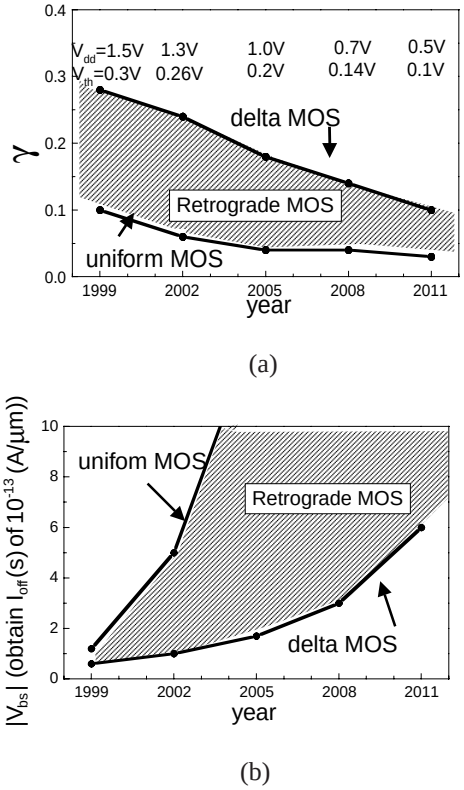


Fig. 8. Scalability of VTMOS in the scaling scenario with scaled V_{th}. (a) Variation of γ in each generation. (b) Required $|\Delta V_{bs}|$ to obtain an I_{off}(s) of 10^{-13} A/μm. γ becomes larger by the channel engineering and the required $|\Delta V_{bs}|$ can be suppressed by channel engineering.

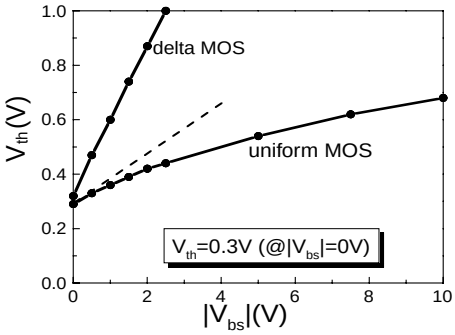
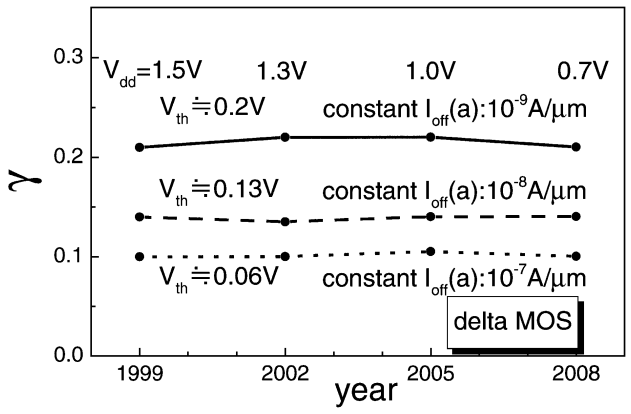


Fig. 9. Relation between V_{th} and $|V_{bs}|$. In a uniform MOS, ΔV_{th} is proportional to the square root of V_{bs}. In delta MOS, ΔV_{th} is almost proportional to V_{bs}. Channel profile should be as steep as in the delta MOS, and a super steep channel profile is strongly desired in scaled VTMOS.

This is because in delta MOS, the depletion layer width is kept almost constant even if V_{bs} is applied. Therefore, the channel profile of VTMOS should be as steep as that of the delta MOS, and a super steep channel profile is strongly desired.

3.2 A Scaling scenario with constant V_{th}

In the second scenario, I_{off}(a), and hence V_{th}(a), are kept constant, while other parameters such as V_{dd}, gate length and gate oxide thickness are scaled according to ITRS.[10] In VTMOS, V_{th}(a) can be extremely low because subthreshold leakage is suppressed in the standby mode. Therefore, this scenario is more practical than the first scenario. Figure 10 shows the variation of γ and the required ΔV_{bs} for a



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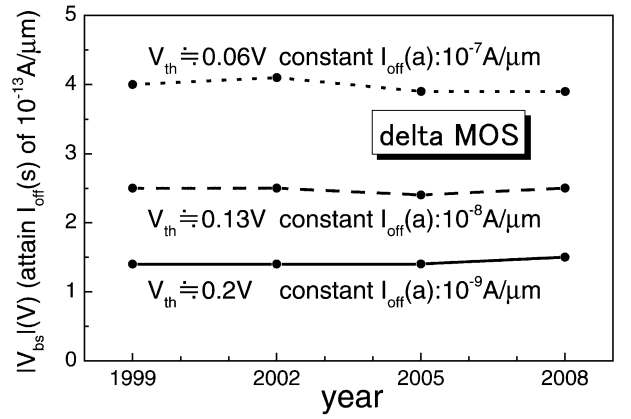

(b)

Fig. 10. Scalability of VTMOS in the scenario with constant V_{th}. (a) Variation of γ in each generation. (b) Required $|\Delta V_{bs}|$ to obtain I_{off}(s) of 10^{-13} A/μm. The advantage of the constant V_{th} scenario is that γ is kept almost constant and the required $|\Delta V_{bs}|$ remains almost the same. However, the disadvantage is that I_{on}(a) becomes too small due to the constant V_{th}. The best scaling scenario for a VTMOS would depend on the application.

delta MOS. The uniform MOS is not shown here because the required ΔV_{bs} is too large. In this scenario, the depletion layer width should decrease rapidly in order to keep V_{th} constant. Therefore, γ is kept almost constant, and the required ΔV_{bs} is also almost constant. This is a great advantage for VTMOS. However, a disadvantage of this scenario is that I_{on}(a) is greatly degraded due to constant V_{th}(a) as the device is scaled.

These discussions suggest that the scalability of VTMOS depends on the scaling scenario and it also depends on the applications. In the 50 nm generation with very low supply voltage, all the requirements for scaled devices, such as high speed, low standby off-current, low active off-current, will not fulfilled by normal MOSFETs without threshold control. VTMOS will certainly satisfy more requirements than normal MOSFETs and will survive in the 50 nm generation depending on the scaling scenario and applications.

4. Conclusions

The effects of γ and ΔV_{bs} in a VTMOS have been systematically examined by simulation under a condition of fixed off-current in the standby mode, and the optimal γ and ΔV_{bs} are derived to obtain a higher on-current in the active mode by means of device simulation. When off-current in the active mode is limited, a larger $|\Delta V_{bs}|$ and smaller γ are preferable to obtain a higher drive current. When γ is fixed, $|\Delta V_{bs}|$ should be as large as is permitted by the breakdown and leakage current. When ΔV_{bs} is fixed for some reason, such as the breakdown, the optimum γ depends on the relationship between $|\Delta V_{bs}|$ and V_{dd}. The same optimal conditions are obtained for a lower off-current and fixed on-current. The scalability of a VTMOS is also discussed and it is found that channel engineering is required in scaled VTMOS. These results are expected to be of great help in designing ultra-low power VTMOS VLSIs, and the VTMOS will survive in the 50 nm generation depending on the scaling scenario and applications.

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