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Optimum Device Parameters and Scalability of Variable Threshold CMOS (VTCMOS)

T. Hiramoto[1,2], M. Takamiya[1], H. Koura[1], T. Inukai[1], H. Gomyo[1], H. Kawaguchi[1], and T. Sakurai[1,3]
[1]Institute of Industrial Science, University of Tokyo, Roppongi, Minato-ku, Tokyo 106-8558, Japan
[2]VLSI Design and Education Center, University of Tokyo, Hongo, Bunkyo-ku, Tokyo 113-8656, Japan
[3]Center for Collaborative Research, University of Tokyo, Roppongi, Minato-ku, Tokyo 106-8558, Japan
Phone/Fax: +81-3-3402-0873, E-mail: hiramoto@nano.iis.u-tokyo.ac.jp

1. Introduction

Variable threshold voltage CMOS (VTCMOS) is one of the most promising device/circuit schemes for low power VLSI applications [1-3]. The threshold voltage (V_{th}) is shifted by substrate bias (V_{bs}) using body effect, and high V_{th} in the stand-by mode and low V_{th} in the active mode are attained. The V_{th} shift (ΔV_{th}) is given by

$$\Delta V_{th} = \gamma |\Delta V_{bs}|, \qquad (1)$$

where γ is the body effect factor [4,5]. Therefore, γ and ΔV_{bs} are the most important device parameters in VTCMOS. However, the optimum device design for VTCMOS has not been generally recognized and the scalability of VTCMOS is an issue of great concern for future applications. In this study, the optimum device design for VTCMOS is systematically investigated by device simulation and the scalability of VTCMOS is discussed. It is suggested that, while VTCMOS aiming at ultra-low stand-by current does not maintain its advantage as the device and the supply voltage are scaled, VTCMOS will be an essential device/circuit scheme aiming at high-speed applications.

2. Characteristics of VTCMOS

The main target of VTCMOS is to reduce the stand-by current (I_{off}) while maintaining the circuit speed ("low power mode"). When the stand-by current is fixed, on the other hand, the on-current (I_{on}) can be enhanced by body effect in VTCMOS [5] ("high-speed mode"). The characteristics of these two modes are illustrated in Fig. 1. In order to investigate the VTCMOS performances, two dimensional device simulation [6] is performed assuming uniformly doped, delta-doped, and counter doped MOSFETs [5]. The device parameters are based on the International Technology Roadmap for Semiconductors (ITRS) [7]. Fig. 2 shows the dependences of VTCMOS characteristics on γ and $|\Delta V_{bs}|$ at the 180 nm technology node. It is suggested in both modes that

(1) $|\Delta V_{bs}|$ should be set as large as the junction leakage permits.

(2) When the values of γ and V_{th} can be designed at a fixed V_{bs}, the optimum γ depends on the relationship between supply voltage (V_{dd}) and $|\Delta V_{bs}|$.

At the 180 nm technology node, V_{dd} is sufficiently high and both low power mode and high-speed mode can be attained.

3. Scaling of VTCMOS

When the device size and V_{dd} are scaled, the VTCMOS characteristics significantly differ from the 180 nm technology node. Three scaling scenarios are shown in Fig. 3 and required $|\Delta V_{bs}|$ is shown in Fig. 4.

3.1. Low power mode: In the battery-operated portable system, the stand-by current should be less than 0.1 pA/μm. Then, V_{th} in the stand-by mode should be higher than 0.5 V and ΔV_{th} should be larger as V_{dd} is scaled (Scenario A), as shown in Fig. 3. Required $|\Delta V_{bs}|$ increases rapidly and would exceed breakdown voltage, as shown in Fig. 4. The scaling scenario of low power mode will fail in the future.

3.2. High-speed mode: On the other hand, the advantage of VTCMOS will be kept even when ΔV_{th} is constant (Scenario B) or is reduced (Scenario C), because on-current enhancement is determined by $\Delta V_{th}/V_{dd}$. While Scenario B will fail due to constant $|\Delta V_{bs}|$, Scenario C where the current enhancement ratio ($\Delta I_{on}/I_{on}$) is constant will take full advantage because required $|\Delta V_{bs}|$ is reduced in proportion to V_{dd}. Fig. 5 shows the dependences of VTCMOS characteristics on γ and $|\Delta V_{bs}|$ at the 35 nm technology node in Scenario C. To reduce the junction leakage current by back-bias, positive V_{bs} is applied. The positive V_{bs} will become very effective when V_{dd} is scaled down to lower than 0.6 V. Forwarded pn-junction current is negligible because it flows in the enhancement mode. Scenario C can attain high on-current in the enhancement mode while suppressing the off-current in the normal mode.

4. Device/Circuit Scheme in the future

In VTCMOS in the high-speed mode (Scenario C), the stand-by power will be huge and we certainly need another measure to suppress the stand-by current. Fig. 6 shows a schematic of the device/circuit scheme where high-speed mode VTCMOS is combined with leak cut-off switch such as BGMOS [8] and SCCMOS [9]. The high-speed scheme and the low stand-by scheme should be merged when the device and V_{dd} are scaled in the future.

5. Conclusion

The optimum device parameters and scalability of VTCMOS have been discussed. Although the scaling scenario of low stand-by current VTCMOS will fail, high-speed VTCMOS will take advantage in the combination with a low stand-by scheme.

Acknowledgment

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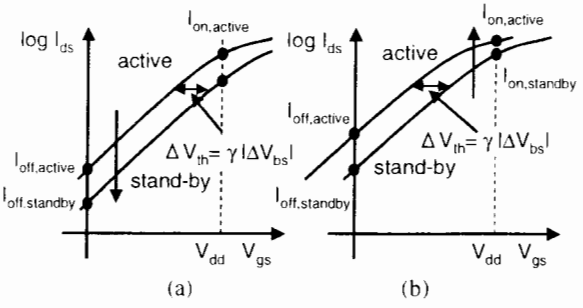


Fig. 1. Schematics of VTCMOS characteristics in the two modes. (a) Low power mode where I_{off} is reduced while maintaining I_{on}. I_{off} in the stand-by mode ($I_{off,standby}$) is suppressed compared with that in the active mode ($I_{off,active}$) using body effect. V_{bs} in the active mode ($V_{bs,active}$) is 0 V in this study. (b) High-speed mode where I_{on} is enhanced while maintaining I_{off}. I_{on} in the active mode ($I_{on,active}$) can be enhanced compared with that in stand-by mode ($I_{on,standby}$).

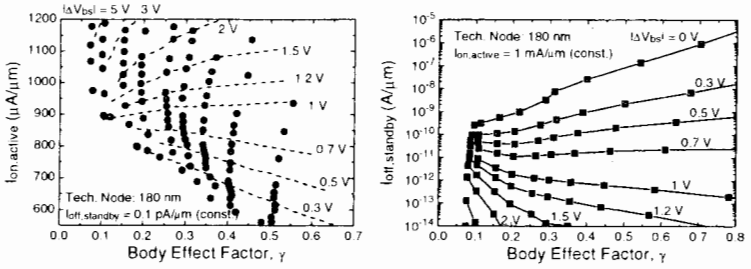
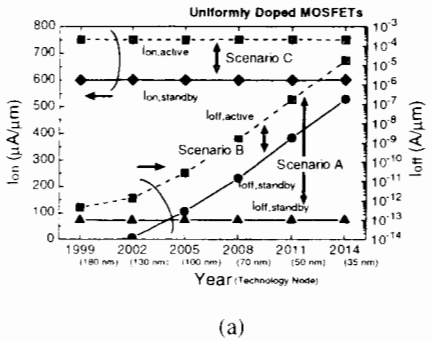


Fig. 2. VTCMOS characteristics as a function of γ and $|\Delta V_{bs}|$ at the 180 nm technology node. (a) High-speed mode. $I_{off,standby}$ is fixed to the constant value (0.1 pA/μm). $V_{bs,active}$ = 0 V in this case. When $|\Delta V_{bs}|$ is small, a device with smaller γ gives larger $I_{on,active}$ than that with larger γ. In contrast, when $|\Delta V_{bs}|$ is large, a device with larger γ gives larger $I_{on,active}$ although $I_{off,active}$ also increases. (b) Low power mode. $I_{on,active}$ is fixed to the constant value (1 mA/μm). $V_{bs,active}$ = 0 V. When $|\Delta V_{bs}|$ is small, a device with smaller γ gives smaller $I_{off,standby}$, which is similar to the high-speed mode.



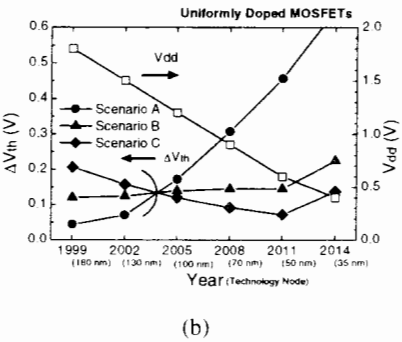


Fig. 3. Three scaling scenarios of VTCMOS. Scenario A: $I_{off,standby}$ is constant (= 0.1 pA/μm) (low power mode). Scenario B: $I_{off,standby}/I_{off,active}$ is constant (= 0.01) (high-speed mode). Scenario C: current enhancement $\Delta I_{on}/I_{on}$ is constant (= 0.2) (high-speed mode). $I_{on,active}$ is set to 750 μA/μm and $V_{bs,active}$ = 0 V in all cases. Uniformly doped MOSFETs are assumed. Device parameters at each technology node are based on ITRS. (a) Relationship between I_{on} and I_{off}. (b) Relationship between V_{dd} and ΔV_{th}. ΔV_{th} rapidly increases in Scenario A. ΔV_{th} is roughly constant in Scenario B. ΔV_{th} decreases in proportion to V_{dd} in Scenario C.

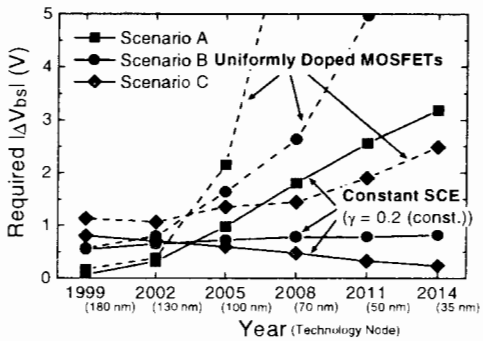
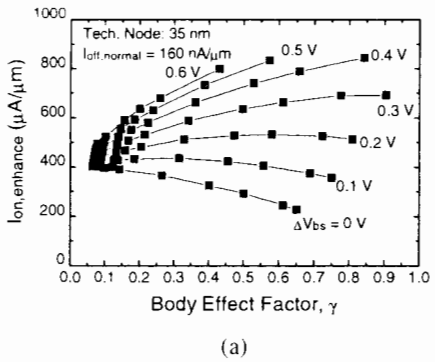


Fig. 4. Required $|\Delta V_{bs}|$ in three scenarios at each technology node. Broken lines show the simulation results for uniformly doped MOSFETs, where γ decreases as the device is scaled. Solid lines show devices with constant short channel effect (γ = 0.2). Even in the latter case, Scenarios A and B will fail due to large $|\Delta V_{bs}|$ compared with V_{dd}.



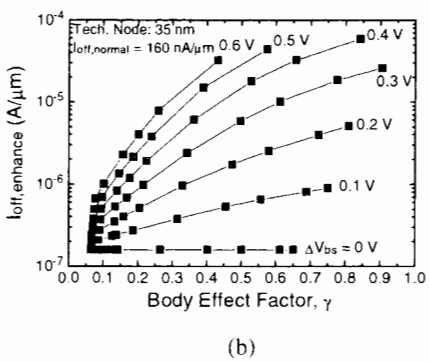


Fig. 5. VTCMOS characteristics in the high-speed mode as a function of γ and $|\Delta V_{bs}|$ at the 35 nm technology node. Here, the two modes are denoted by enhancement and normal modes, instead of active and stand-by modes. Positive V_{bs} is applied in the enhancement mode and V_{bs} in the normal mode ($V_{bs,normal}$) is set to 0 V. I_{off} in the normal mode ($I_{off,normal}$) is fixed to 160 nA/μm. When $|\Delta V_{bs}|$ is sufficiently large, I_{on} in the enhancement mode ($I_{on,enhance}$) increases dramatically, although $I_{off,enhance}$ also increases.

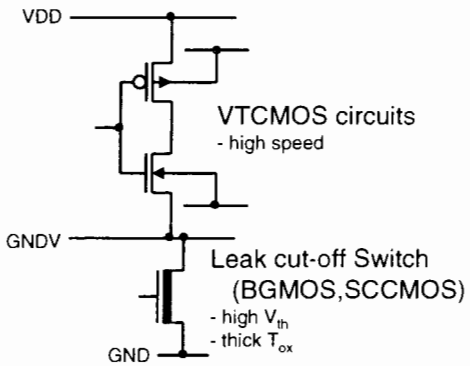


Fig. 6. A device/circuit scheme in the future, where the high-speed VTCMOS and leak cut-off switch such as BGMOS [8] or SCCMOS [9] are combined. VTCMOS enhances I_{on} and leak cut-off switch reduces I_{off}.