Separation of Effects of Statistical Impurity Number Fluctuations and Position Distribution on Vth Fluctuations in Scaled MOSFETs

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***Abstract*—We have investigated the effect of the statistical "position" distribution of dopant atoms on threshold voltage (V_{th}) fluctuations in scaled MOSFETs. The effects of impurity "number" fluctuations and impurity "position" distribution are successfully separated in two-dimensional simulation for fully-depleted (FD) SOI MOSFETs. It is found that the contribution by the position distribution is closely related to the charge sharing factor (CSF) and the effect of the impurity position distribution becomes dominant as CSF is degraded. Consequently, the contribution ratio of the impurity position distribution is kept almost constant when the device is properly scaled.**

***Index Terms*—Charge sharing factor, depletion region, FD SOI MOSFET, impurity, number fluctuation, position distribution, scaling, threshold voltage.**

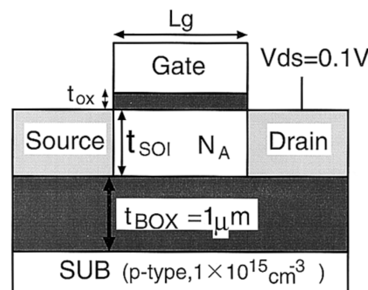

Fig. 1. Device structure of fully depleted SOI MOSFET assumed in this study. V_{ds} is 0.1 V to decrease the short channel effect except for the V_{ds} dependence, and the buried oxide thickness (t_{BOX}) is 1 μm to decrease the effect of impurity in the substrate.

I. Introduction

THE THRESHOLD voltage (V_{th}) fluctuations due to the statistical impurity fluctuations in the channel is one of the most serious problems in scaled MOSFET [1], because the V_{th} fluctuations increase as the device is scaled down. The statistical V_{th} fluctuations have been widely studied by experiments [2]–[4] and simulations [5]–[12]. In these studies, the effects of impurity "number" fluctuations are generally discussed. It has been also pointed out that the V_{th} fluctuations are caused not only by the impurity "number" fluctuations but also by the impurity "position" distribution [2], [3], [6]–[8], [10]. In an extremely scaled MOSFET where the number of impurities is reduced, the slight change of the impurity "position" would cause a large change in the device characteristics [7]. Therefore, it is very important to quantitatively evaluate the effect of impurity "position" distribution and clarify the origin of V_{th} fluctuations due to the "position" distribution. The variation of the V_{th} fluctuations with device scaling is also of great interest.

Some models of the V_{th} fluctuations which include both the "position" distribution and the "number" fluctuations have been already studied [13]–[15]. However, these works have discussed only "total" V_{th} fluctuations and the effects of impurity number and position have not been separated. Although some simulation works deal with the relation between the V_{th} fluctuations and the impurity position in the depth direction [10], [12], the lateral impurity position distribution are not considered.

In this work, we have separated the impurity "number" fluctuations and impurity "position" distribution, and investigated their effects on the V_{th} fluctuations by means of two-dimensional (2-D) [16] and three-dimensional (3-D) device simulations [17]. It is found, for the first time, that the effect of the impurity position distribution on V_{th} fluctuations depends on the charge sharing factor (CSF) and the V_{th} fluctuations due to the impurity "position" distribution originate from the impurity number fluctuations in gate-controlled depletion region.

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II. Simulation Mehtod

In this section, the simulation method and conditions are described. In order to investigate the effects of channel impurity number fluctuations and impurity position distribution, the two effects should be separated. In conventional bulk MOSFETs, it is very hard to separate these two effects, because the depletion layer width (l_d) is varied by changing the channel impurity position distribution, and the impurity number in the depletion layer can not be kept constant. In FD SOI MOSFET's, on the other hand, l_d corresponds to the SOI thickness and the impurity number can be kept constant. Therefore, the effects of impurity number and position fluctuations on V_{th} fluctuations can be separated and we can independently set the impurity number and position fluctuations in the simulation [18]. Fig. 1 shows the structure of an FD SOI MOSFET.

In order to introduce the statistical impurity fluctuations into the simulation, the channel of a MOSFET is divided into small cells [Δx, Δy and Δz in the direction of the length (L_g), depth

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TABLE I
DEVICE PARAMETERS OF FULLY DEPLETED SOI MOSFET USED IN THE SIMULATION

Device	t_{ox} (nm)	t_{SOI} (nm)	$\overline{N_A}(cm^{-3})$
A	5	50	2×10^{17}
B	2	10	1×10^{18}
C	2	10	5×10^{16}
D	2	10	1×10^{17}
E	2	10	5×10^{18}
F	2	5	1×10^{18}
G	2	20	1×10^{18}
H	5	10	1×10^{18}
I	10	10	1×10^{18}

and width (W_g), respectively] and impurities are distributed to these cells at random, so that the possibility that each impurity atoms is distributed is the same for all the divided cells. Two cases are simulated for FD SOI MOSFET. In the first case, both impurity number fluctuations and impurity position distribution are considered. This case corresponds to the total V_{th} fluctuations ($\sigma V_{th,\,total}$). In the second case, only the impurity position distribution are considered and the impurity number is kept constant. This case corresponds to the V_{th} fluctuations due to the position distribution ($\sigma V_{th,position}$). In the first case, we choose the impurity number that follow Poisson distribution with an average channel concentration of $\overline{N_A}$ and the impurities are distributed into cells at random [6]. In the second case, the channel impurity number is kept constant and only the impurity positions are chosen at random. A impurity number in each cell (n') is converted into a concentration $[N_A' = n'/(\Delta x\,\Delta y\,\Delta z)]$. In the case of 2-D simulation, Δz is equal to W_g [9]. In order to investigate W_g dependence in 2-D simulation, Δz is varied. Table I shows the device parameters assumed in this study. The standard deviation of $V_{th}(\sigma V_{th})$ of each structure is derived from 800 or 200 samples in 2-D simulation and 100 samples in 3-D simulation. The drain voltage (V_{ds}) is 0.1 V to decrease the short channel effect (SCE), except for the simulation of the V_{ds} dependence. V_{th} is derived from a current criteria of $10^{-7}W_g/L_g(A)$.

III. SIMULATION RESULTS

In this section, the contribution by the impurity position distribution are described.

First, the contribution ratio of the effect of impurity position distribution to the total V_{th} fluctuations should be defined. The total V_{th} fluctuations due to the statistical channel impurity fluctuations are given by

$$(\sigma V_{th,\,total})^2 = (\sigma V_{th,position})^2 + (\sigma V_{th,\,number})^2 \tag{1}$$

where $\sigma V_{th,\,number}$ is standard deviation of V_{th} in which only the impurity number fluctuations are included and the impurities are uniformly distributed over each cell resulting in no position distribution. This is because the impurity number and position fluctuations are independent events. The contribution ratio $R_{position}$ by position distributions to the total fluctuations is defined as

$$R_{position} = \left(\frac{\sigma V_{th,position}}{\sigma V_{th,\,total}}\right)^2. \tag{2}$$

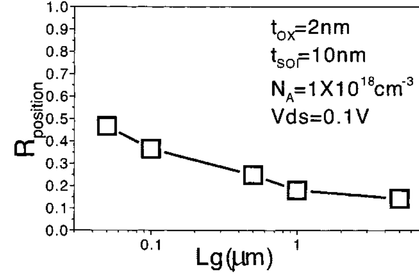

Fig. 2. Dependence of $R_{position}(= (\sigma V_{th,\,position}/\sigma V_{th,\,total})^2)$ on gate length (L_g). Device B is used.

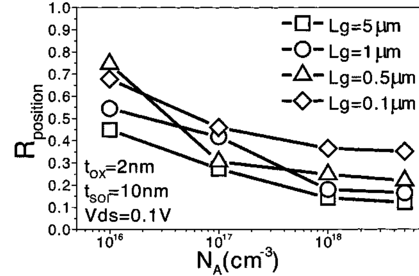

Fig. 3. Dependence of $R_{position}(= (\sigma V_{th,\,position}/\sigma V_{th,\,total})^2)$ on channel concentration (N_A). Device B, C, D, and E are used.

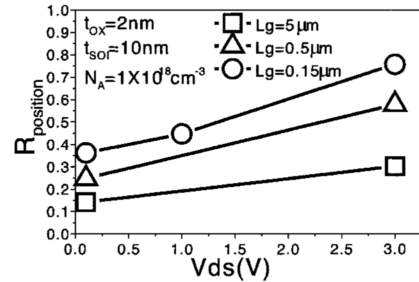

Fig. 4. Dependence of $R_{position}(= (\sigma V_{th,\,position}/\sigma V_{th,\,total})^2)$ on drain voltage (V_{ds}).

The validity of the 2-D simulation has been confirmed by comparing the 2-D simulation results with the experimental data and the 3-D simulation data [18]. We also examined the effects of the way of dividing into small cells. We find that σV_{th} does not depend on how to divide the channel into cells in simulation. Therefore, cell sizes are defined as $L_g/40(\Delta x)$, $t_{\rm SOI}/10(\Delta y)$ and $W_g/10(\Delta z)$, and are equal to spacing. These results are in agreement with the results by Stolk *et al.* [9].The dependence of $R_{position}$ on device parameters of FD SOI MOSFETs is investigated by the 2-D simulation. The device parameters investigated are gate length (L_g), gate width (W_g), SOI thickness ($t_{\rm SOI}$), gate oxide thickness (t_{OX}), channel concentration (N_A), and drain voltage (V_{ds}).

Figs. 2–4 show the simulation results. $R_{position}$ does not depend upon W_g, $t_{\rm SOI}$ and t_{OX} (not shown in the figure). In 2-D simulation, the effect of impurity position distribution along the

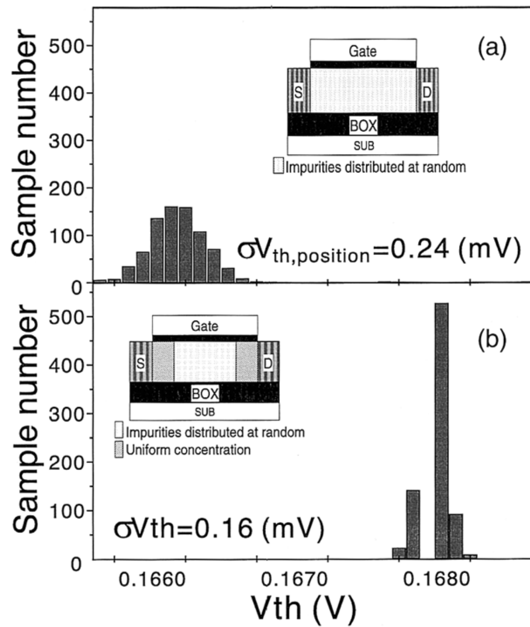

Fig. 5. Distribution of V_{th} in two kinds of devices with the same impurity number. The device parameters used are those of Device B in Table I. (a) Impurities are distributed at random in the whole channel. The standard deviation corresponds to $\sigma V_{th,\,position}$. (b) Impurities are distributed in region controlled by gate and impurities are uniformly doped near source and drain. The difference in the average V_{th} is obtained which is in agreement with [11].

channel width is not taken into account. In order to investigate the W_g dependence in more detail, we have also perform the 3-D simulation. The obtained $\sigma V_{th,\,total}$ and $\sigma V_{th,\,position}$ are almost the same as those in 2-D simulation, and W_g dependence of $R_{position}$ has not been found in 3-D simulation. The current percolation due to the 3-D effect will have more influence on V_{th} fluctuations in scaled devices and should be investigated further.

It is found from Figs. 2–4 that $R_{position}$ has dependence on L_g, N_A and V_{ds}. $R_{position}$ increases as L_g and N_A decrease. It is also found that $R_{position}$ depends on V_{ds} in a fixed device as shown in Fig. 4. The absolute value of σV_{th} increases as V_{ds} increase. Moreover, when L_g is small, more dependence on V_{ds} is found. This is in good agreement with the experiment [3]. It should be noted that these dependences on device parameters are quite similar to those of charge sharing. $R_{position}$ is larger when the device has more short channel effects due to charge sharing. It appears from these results that the effect of impurity position distribution is determined by the charge sharing. As the impurity position distributes, the impurity number in the source and drain-controlled depletion region fluctuates and therefore, V_{th} fluctuates.

IV. Impurity Position Distribution and Charge Sharing

In order to investigate the relationship between the charge sharing and statistical position distribution, two kinds of devices are simulated as shown in Fig. 5. Here, the charge sharing factor (CSF) is defined as

$$\begin{aligned}\text{CSF} &= \frac{\text{Impurity number in gate controlled depletion region}}{\text{Total impurity number}}\\ &= \frac{\text{Area of gate controlled depletion region}}{\text{The whole channel area}}.\end{aligned} \tag{3}$$

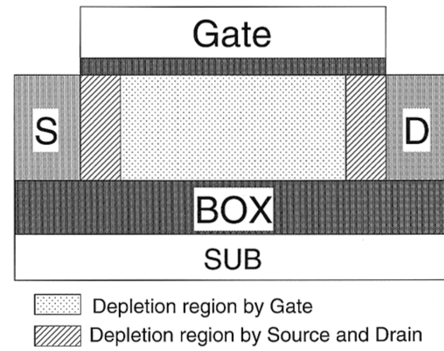

Fig. 6. Schematic of depletion region controlled by source and drain.

In both devices, channel impurity number is set constant. In the first device, all the impurities in channel are distributed at random and therefore, CSF of individual devices would be fluctuated by the statistical impurity position fluctuations. In the second device, on the other hand, the regions near source and drain are uniformly doped and impurities are distributed at random at the rest of the channel. In this device, CSF would not be fluctuated because there is no position distribution near source and drain region. Fig. 5 shows the V_{th} distributes largely in the first device, while only a slight V_{th} distribution is obtained in the second device. This result clearly indicates that the V_{th} fluctuations due to the impurity position distribution originate from the CSF fluctuations in the channel depletion region near source and drain of the individual devices.

A simple charge sharing model for FD SOI MOSFET is considered in order to evaluate the quantitative relationship between $R_{position}$ and CSF in MOSFETs with various device parameters. The charge sharing regions controlled by source and drain are given approximately by rectangles as shown Fig. 6 (This approximation in FD SOI MOSFET is confirmed by simulation not shown here). Hence, CSF is given by

$$(1 - \overline{\text{CSF}}) \cong \frac{\overline{X_d}}{L_g} \propto \frac{1}{L_g\sqrt{\overline{N_A}}} \tag{4}$$

where X_d is depletion layer width by source and drain. The averages of CSF, X_d and N_A should be considered because 800 samples are simulated in a fixed device parameter to obtain $\sigma V_{th,\,total}$ and $\sigma V_{th,\,position}$, respectively. In this equation, the effect of drain voltage is ignored, because V_{ds} is fixed at 0.1 V in this study except for the simulation of V_{ds} dependence.

Fig. 7 shows the relation between $R_{position}$ and $L_g\sqrt{\overline{N_A}}$. All the simulated devices in Table I are plotted. It should be noted that most of devices are plotted on one line. On the other hand, when the simulated data are plotted as a function of gate length or average channel impurity number (not shown in the figure), the plots largely distribute. Therefore, Fig. 7 strongly indicates that $R_{position}$ is primarily determined by the charge sharing. It is also clearly found from Fig. 7 that the effect of position distribution becomes dominant as CSF is degraded ($L_g\sqrt{\overline{N_A}}$ decreases) and the device has more short channel effects. This is because, when CSF is degraded, impurity number in drain-controlled depletion region is larger and consequently is fluctuated more largely.

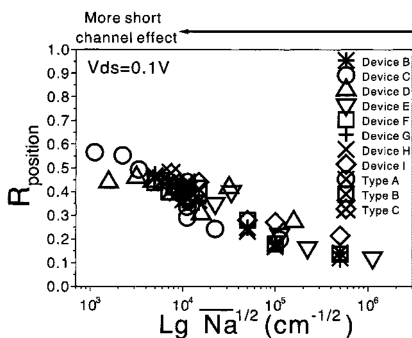

Fig. 7. Relation between $R_{position}(=(\sigma V_{th,\,position}/\sigma V_{th,\,total})^2)$ and $L_g\sqrt{N_A}$. All simulated devices in Table I are plotted. In Device B–I, gate length is varied. In type A–C of Table II, all parameters are scaled.

TABLE II
SCALING METHODS OF FD SOI MOSFET FOR THE SIMULATION.

	L	W	t_{ox}	t_{SOI}	N_A
Type A	$\frac{1}{K}$	$\frac{1}{K}$	$\frac{1}{K}$	$\frac{1}{K}$	K^2
Type B	$\frac{1}{K}$	$\frac{1}{K}$	1	$\frac{1}{K}$	K
Type C	$\frac{1}{K}$	$\frac{1}{K}$	$\frac{1}{K}$	$\frac{1}{K}$	$K^{\frac{3}{2}}$

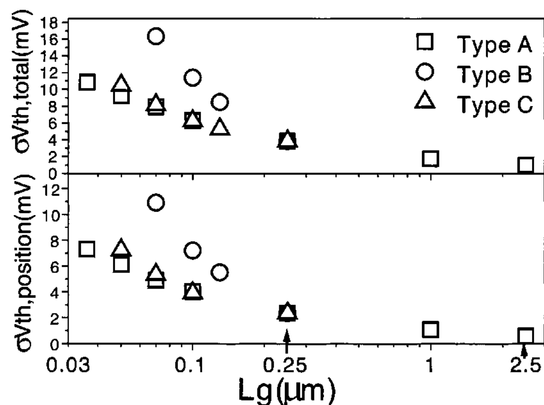

Fig. 8. Variation of the absolute value of σV_{th} with scaling in FD SOI MOSFETs. The standard device parameters used are Device A at $L_g = 0.25$ μm in Table I. This device is scaled by the scaling methods summarized in Table II.

V. VARIATION OF $R_{position}$ WITH SCALING

Finally, the variation of $R_{position}$ with device scaling is examined. Table II shows three different scaling methods in FD SOI MOSFETs. Fig. 8 shows the absolute value of $\sigma V_{th,\,total}$ and $\sigma V_{th,\,position}$. $\sigma V_{th,\,total}$ includes both the impurity number and position fluctuations. $\sigma V_{th,\,position}$ includes only the impurity position distribution. Both σV_{th} increase as the device is scaled down.

Fig. 9 shows $R_{position}$ when the device size is scaled. Although the absolute value of σV_{th} increases, $R_{position}$ is almost constant as the device is scaled down. This is because the charge sharing factor is almost constant when the device is properly scaled . Therefore, it is concluded that the effect of impurity position distribution would not dominate the total V_{th} fluctuations as long as the device is properly scaled, although the increase in the absolute value of total σV_{th} would be a serious problem in the future. These results in FD SOI MOSFETs would be also applicable to the bulk MOSFETs.

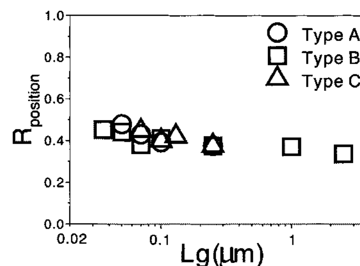

Fig. 9. Variation of $R_{position}(=(\sigma V_{th,\,position}/\sigma V_{th,\,total})^2)$ with device scaling.

VI. CONCLUSIONS

The effects of the statistical channel impurity position distribution on V_{th} fluctuations are investigated. The effects of impurity number fluctuations and impurity position distribution are successfully separated in 2-D simulation for FD SOI MOSFETs. It is found that the contribution ratio of impurity position distribution to the total fluctuations is determined by charge sharing in the depletion region and the effect of position distribution becomes dominant as the charge sharing factor is degraded. It is also suggested that the contribution ratio of the position distribution is almost kept constant when the device is properly scaled down.

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