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Optimum Device Parameters and Scalability of Variable Threshold Voltage Complementary MOS (VTCMOS)

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The optimum device parameters of variable threshold voltage complementary metal oxide semiconductor (VTCMOS) have been investigated by means of device simulation and its scalability has been discussed. The optimum body effect factor depends on the relationship between the substrate bias and the supply voltage. It is shown that the VTCMOS scheme aiming at extremely low stand-by power will fail as the device size and the supply voltage are scaled. The advantage of VTCMOS will be its high speed, and the VTCMOS will be essential in high-speed circuits operating at a low supply voltage in combination with another low stand-by power scheme such as the insertion of leak cut-off switches.

KEYWORDS: variable threshold voltage complementary metal oxide semiconductor (VTCMOS), body effect factor, substrate bias, lowpower, high-speed, scalability, metal oxide semiconductor fieldeffect transistor (MOSFET)

1. Introduction

Strong demands for high-speed and low-power very large scale integrations (VLSIs) are rapidly growing for portable product applications. It is well known that there is a severe trade-off between high-speed and low-power in metal-oxide-semiconductor field-effect transistors (MOSFETs). In order to suppress the active power, the supply voltage (V_{dd}) should be suppressed. The threshold voltage (V_{th}) should also be reduced to maintain the high speed. Then, the stand-by power will increase exponentially due to the increased subthreshold current. One of the solutions to this problem is the variable threshold voltage complementary metal oxide semiconductor (VTCMOS) scheme.[1–3)]

In the VTCMOS scheme, V_{th} of MOSFETs is controlled by substrate bias (V_{bs}) using the body effect. V_{th} is set to a high value in the stand-by mode and is set to a low value in the active mode to attain high speed and low stand-by power at the same time. The characteristics of VTCMOS are strongly related to the V_{th} shift (ΔV_{th}), which depends on the body effect factor γ and the substrate bias change ΔV_{bs}. Therefore, γ and ΔV_{bs} are the most important device parameters in VTCMOS. However, the optimum device design for VTCMOS has not been generally recognized and the scalability of VTCMOS is an issue of great concern for future applications.

In this study, the optimum device design for VTCMOS is systematically investigated by device simulation and the scalability of VTCMOS is discussed. It is suggested that, while VTCMOS aiming at ultra-low stand-by current does not maintain its advantage as the device and the supply voltage are scaled, VTCMOS will be an essential device/circuit scheme aiming at high-speed applications.

2. Optimum Device Parameters

2.1 Definition of body effect factor

In this study, the body effect factor γ is defined by[4,5)]

$$\gamma \equiv \frac{|\Delta V_{th}|}{|\Delta V_{bs}|}, \tag{1}$$

instead of the usual definition in device textbooks which is applicable only to the MOSFET with uniformly doped channel profile. The definition of eq. (1) can be applied to all MOS structures with any channel impurity profile, including retrograde MOSFET, delta-doped MOSFET, counter-doped MOSFET, and silicon-on-insulator (SOI) MOSFET. Then, the threshold voltage shift ΔV_{th} is given by

$$\Delta V_{th} = \gamma |\Delta V_{bs}|, \tag{2}$$

and is directly related to the body effect factor and substrate bias change. Therefore, a larger body effect factor results in a larger threshold voltage shift. On the other hand, the subthreshold factor S is also related to γ, and a MOSFET with a larger body effect factor has a degraded subthreshold swing.[4,5)] Therefore, these two effects would determine the optimum condition of γ once V_{bs} is determined.

2.2 Two modes in VTCMOS

The main target of VTCMOS has been considered as the reduction of the stand-by off-current (I_{off}) while maintaining the circuit speed. Figure 1(a) illustrates the characteristics of VTCMOS aiming at a low stand-by current. While maintaining a high drive current by low threshold voltage in the active mode, the substrate bias is changed in the negative direction to raise the threshold voltage resulting in the decrease in the subthreshold current at stand-by mode. We call this configuration the "low-power mode". In addition, there is another advantage of VTCMOS: speed enhancement. When the stand-by current is fixed, the on-current (I_{on}) can be largely enhanced by the body effect in VTCMOS. This configuration is illustrated in Fig. 1(b). In the active mode, the substrate bias is changed in the positive direction to reduce the threshold voltage resulting in the enhancement of on-current. This is called the "high-speed mode". Therefore, VTCMOS has two modes with different objectives.

2.3 Simulation results

In order to investigate the VTCMOS performances in the two modes, two-dimensional device simulation[6)] was per-

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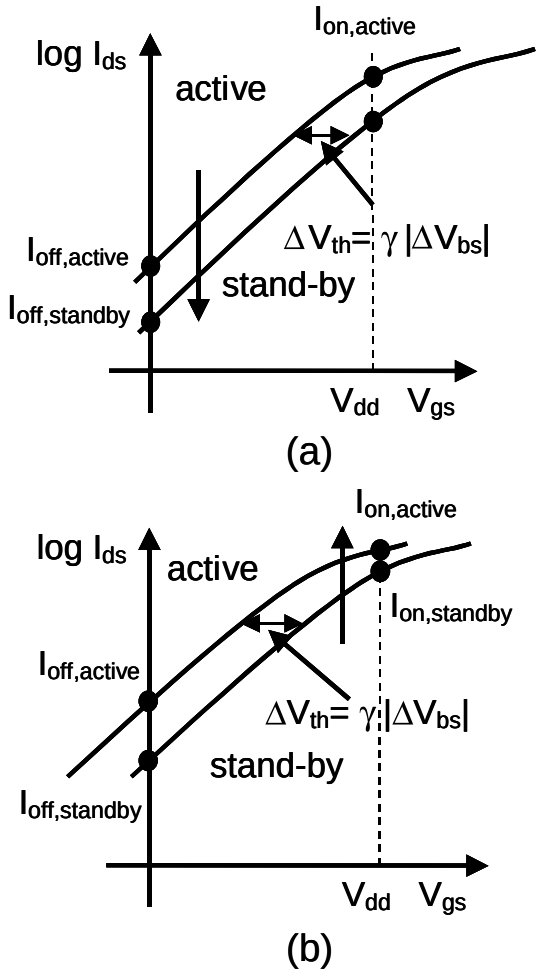

Fig. 1. Schematics of VTCMOS characteristics in the two modes. (a) Low-power mode where I_{off} is reduced while maintaining I_{on}. I_{off} in the stand-by mode ($I_{off,standby}$) is suppressed compared with that in the active mode ($I_{off,active}$) using body effect. V_{bs} in the active mode ($V_{bs,active}$) is 0 V in this study. (b) High-speed mode where I_{on} is enhanced while maintaining I_{off}. I_{on} in the active mode ($I_{on,active}$) can be enhanced compared with that in stand-by mode ($I_{on,standby}$).

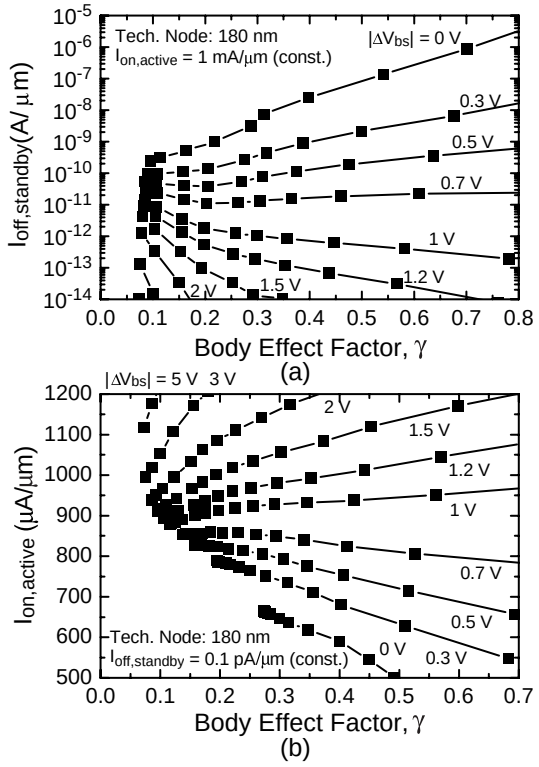

Fig. 2. VTCMOS characteristics as a function of γ and $|\Delta V_{bs}|$ at the 180 nm technology node. (a) Low-power mode. $I_{on,active}$ is fixed at a constant value (1 mA/μm). $V_{bs,active} = 0$ V. There is a critical voltage V_o, where the optimum γ changes. V_o is about 0.7–1.0 V in this case. When $|\Delta V_{bs}|$ is larger than V_o, a device with larger γ gives smaller $I_{off,standby}$, which is similar to the result in the high-speed mode. (b) High-speed mode. $I_{off,standby}$ is fixed at a constant value (0.1 pA/μm). $V_{bs,active} = 0$ V in this case. When $|\Delta V_{bs}|$ is smaller than V_o, a device with smaller γ gives larger $I_{on,active}$ than that with larger γ. In contrast, when $|\Delta V_{bs}|$ is larger than V_o, a device with larger γ gives larger $I_{on,active}$ although $I_{off,active}$ also increases.

formed assuming uniformly doped, delta-doped, and counter doped MOSFETs.[5] The device parameters are based on the International Technology Roadmap for Semiconductors (ITRS).[7] Figure 2 shows the dependences of VTCMOS characteristics on γ and $|\Delta V_{bs}|$ at the 180 nm technology node. The supply voltage is 1.8 V. The characteristics of the low-power mode are shown in Fig. 2(a) where the on-current is fixed and the stand-by off-current is derived as a function of γ and $|\Delta V_{bs}|$. The high-speed mode is shown in Fig. 2(b) where the off-current is fixed and on-current is derived as a function of γ and $|\Delta V_{bs}|$.

In the devices with $V_{bs} = 0$ V, which are normal MOSFETs, the stand-by off-current increases (Fig. 2(a)) or the active on-current decreases (Fig. 2(b)) as γ increases, because subthreshold factor S is degraded. However, by applying V_{bs}, lower stand-by off-current or higher active on-current can be achieved. It is suggested in both modes that $|\Delta V_{bs}|$ should be set as large as the junction leakage permits. It is also shown that when the values of γ and V_{th} can be designed at a fixed V_{bs}, the optimum γ depends on the relationship between a certain voltage V_o and $|\Delta V_{bs}|$, where V_o is about 50–70% of the supply voltage V_{dd}.[5] As shown in Figs. 2(a) and 2(b), smaller off-current and larger on-current can be attained in a device with larger γ when $|\Delta V_{bs}|$ is larger than V_o (about 0.7–1 V in both modes) in the low-power mode and in the high-speed mode, respectively. V_o is an important parameter in VTCMOS. VTCMOS can take full advantage when applied $|\Delta V_{bs}|$ is larger than V_o. At the 180 nm technology node, V_{dd} is sufficiently high. Therefore, both low-power mode and high-speed mode are applicable. The optimum guidelines for γ and $|\Delta V_{bs}|$ are the same for both the modes.

3. Scalability of VTCMOS

3.1 Scaling scenarios

In this section, the scalability of VTCMOS is discussed. When the device size and V_{dd} are scaled, the VTCMOS characteristics significantly differ from those of the 180 nm technology node. Three scaling scenarios are assumed and discussed in the following subsections. The scaling scenarios assumed are summarized in Fig. 3. In all Scenarios, $I_{on,active}$ is set constant (750 μA/μm) with $V_{bs,active} = 0$ V. Consequently, $I_{off,active}$ rapidly increases as technology advances.

Scenario A is based on the low-power mode. In order to attain extremely low stand-by power, the low off-current of 0.1 pA/μm is targeted. Scenarios B and C are based on the high-speed mode. In Scenario B, the reduction ratio of off-current is set to a constant value of two orders of magnitude,

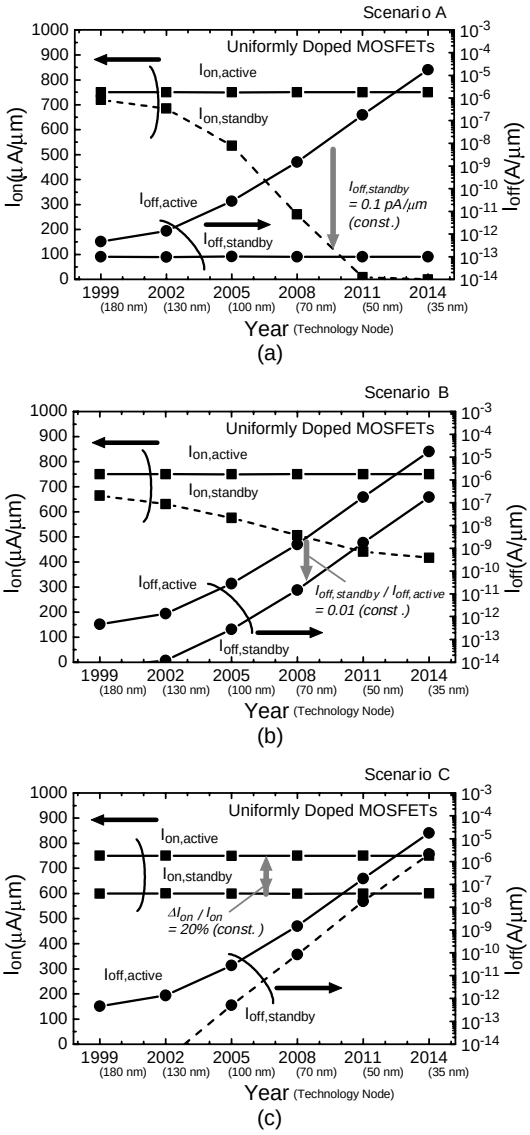

Fig. 3. Three scaling scenarios of VTCMOS. (a) Scenario A: $I_{\mathrm{off,standby}}$ is constant (=0.1 pA/μm) (low-power mode). (b) Scenario B: $I_{\mathrm{off,standby}}/I_{\mathrm{off,active}}$ is constant (=0.01) (high-speed mode). (c) Scenario C: current enhancement $\Delta I_{\mathrm{on}}/I_{\mathrm{on}}$ is constant (=0.2) (high-speed mode). $I_{\mathrm{on,active}}$ is set to 750 μA/μm and $V_{\mathrm{bs,active}} = 0$ V in all cases. Uniformly doped MOSFETs are assumed. Device parameters at each technology node are based on ITRS. The simulation results ($I_{\mathrm{on,standby}}$ in Scenarios A and B, and $I_{\mathrm{off,standby}}$ in Scenario C) derived under the assumption in each Scenario are also shown by a broken line.

in which the threshold voltage shift ΔV_{th} is roughly constant. In Scenario C, the enhancement ratio of on-current is set to a constant value of 20%. The required ΔV_{th} and $|\Delta V_{\mathrm{bs}}|$ are simulated at each technology node, assuming uniformly doped channel MOSFETs. MOSFETs with a constant value of γ ($\gamma = 0.2$) are also assumed when the required $|\Delta V_{\mathrm{bs}}|$ is discussed.

3.2 Low-power mode

In the battery-operated portable system, the stand-by current required is less than 0.1 pA/μm. Then, V_{th} in the stand-by mode should be higher than 0.5 V. The low-power mode of VTCMOS aims at this kind of low stand-by current. Figures 4 and 5 show the required ΔV_{th} and $|\Delta V_{\mathrm{bs}}|$ at each technology node. In Scenario A, ΔV_{th} becomes larger as V_{dd} is scaled,

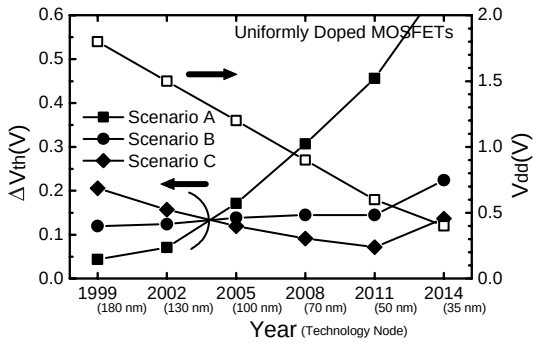

Fig. 4. Relationship between V_{dd} and ΔV_{th}. ΔV_{th} rapidly increases in Scenario A. ΔV_{th} is roughly constant in Scenario B. ΔV_{th} decreases in proportion to V_{dd} in Scenario C.

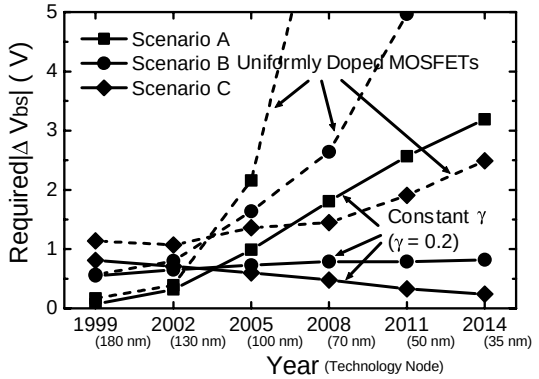

Fig. 5. Required $|\Delta V_{\mathrm{bs}}|$ in three scenarios at each technology node. Broken lines show the simulation results for uniformly doped MOSFETs, where γ decreases as the device is scaled. Solid lines show devices with a constant body effect factor ($\gamma = 0.2$), which roughly corresponds to constant short channel effect. Even in the latter case, Scenarios A and B will fail due to large $|\Delta V_{\mathrm{bs}}|$ compared with V_{dd}.

and $|\Delta V_{\mathrm{bs}}|$ increases rapidly and would exceed breakdown voltage. Therefore, the scaling scenario of low-power mode will fail in the future. One of the reasons for this failure is the reduction of the body effect factor in the uniformly doped channel MOSFETs[5] as the device is scaled. When γ is degraded, the short channel effect immunity is also degraded.[4] In the ideal device scaling, γ should be kept constant in order to suppress the short channel effect. Therefore, a channel engineered MOSFET with a larger γ is strongly required in normal MOSFETs as well as in VTCMOS in the future.[5] However, even when γ can be kept constant (0.2), the required $|\Delta V_{\mathrm{bs}}|$ will increase due to the increase of ΔV_{th}, as shown in Fig. 5, and Scenario A will fail.

3.3 High-speed mode

The high-speed mode of VTCMOS gives up the suppression of off-current but aims at a high on-current in the active mode. Scenario B has almost constant ΔV_{th} and Scenarios C has ΔV_{th} proportional to V_{dd}, as shown in Fig. 4. Since the enhancement of on-current is roughly determined by $\Delta V_{\mathrm{th}}/V_{\mathrm{dd}}$, Scenario B has a rapidly growing enhancement ratio and Scenario C maintains a constant enhancement ratio of on-current. However, the required $|\Delta V_{\mathrm{bs}}|$ should be also scaled with V_{dd}, considering the breakdown voltage. Therefore, Scenario B will fail due to constant $|\Delta V_{\mathrm{bs}}|$, as shown in Fig. 5, even when γ can be kept constant (0.2). On the other hand, in

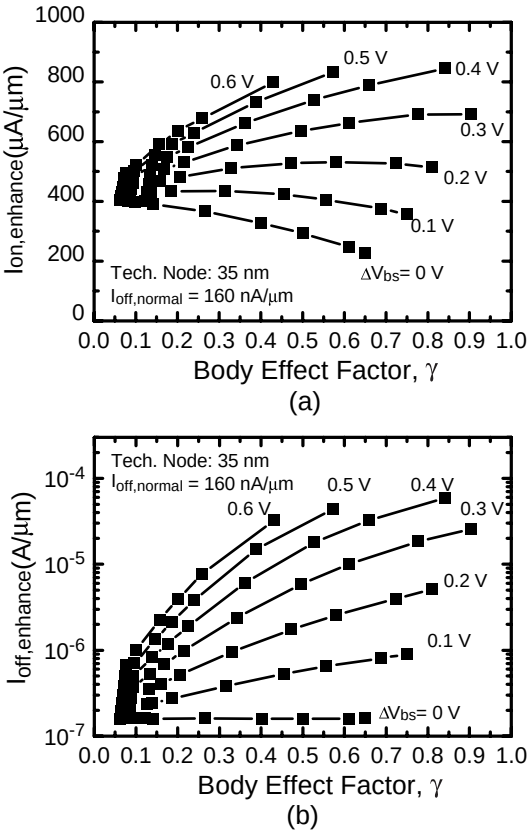

Fig. 6. VTCMOS characteristics in the high-speed mode as a function of γ and $|\Delta V_{bs}|$ at the 35 nm technology node. Here, the two modes are denoted by enhancement and normal modes, instead of active and stand-by modes. Positive V_{bs} is applied in the enhancement mode and V_{bs} in the normal mode ($V_{bs,normal}$) is set to 0 V. I_{off} in the normal mode ($I_{off,normal}$) is fixed at 160 nA/μm. When $|\Delta V_{bs}|$ is sufficiently large compared with V_o (V_o is about 0.2 V in this case), I_{on} in the enhancement mode ($I_{on,enhance}$) increases markedly, although $I_{off,enhance}$ also increases.

Scenario C, since the required ΔV_{th} decreases, the explosion of the required $|\Delta V_{bs}|$ in the uniformly doped channel MOSFETs is greatly suppressed. Furthermore, the required $|\Delta V_{bs}|$ in a MOSFET with constant γ decreases in proportion to V_{dd} as the device is scaled. Considering the scaling of breakdown voltage, Scenario C with a channel engineered MOSFET will maintain the advantage of VTCMOS.

The above results suggest that Scenario C will be the only way in which the VTCMOS can survive as device and supply voltage are scaled. It is also suggested that γ should be kept at a high value by utilizing a steep channel profile. Although the stand-by off-current cannot be suppressed, VTCMOS can enhance the circuit speed and the enhancement ratio of the speed can be maintained even if the device is scaled.

4. Device/circuit Scheme in the Future

Figure 6 shows the dependences of VTCMOS characteristics on γ and $|\Delta V_{bs}|$ at the 35 nm technology node in Scenario C. The supply voltage is assumed to be 0.4 V. In the high-speed mode, "stand-by" and "active" are not suitable mode names. We rename the modes as "normal" and "enhancement" modes, respectively. To reduce the junction leakage current by back-bias, V_{bs} is 0 V in the normal mode and the positive V_{bs} is applied in enhancement mode.[8,9] The positive V_{bs} will become highly effective when V_{dd} is scaled down to lower than 0.6 V. Forwarded pn-junction current is negligible because it flows in the enhancement mode. The high-speed mode can attain high on-current in the enhancement mode when γ is high and applied $|\Delta V_{bs}|$ is larger than V_o, which is about 0.2 V in the present case. Although the off-current is also enhanced in the enhancement mode as shown in Fig. 6(b), the off-current can be reduced in the normal mode by switching V_{th}.

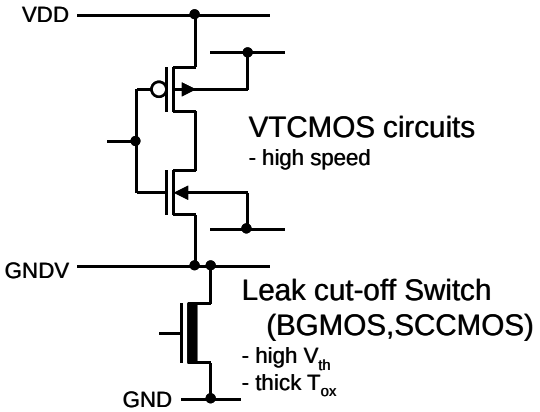

Fig. 7. A device/circuit scheme in the future, where the high-speed VTCMOS and a leak cut-off switch such as BGMOS[10] or SCCMOS[11] are combined. VTCMOS enhances I_{on} and leak cut-off switch reduces I_{off}.

However, in the high-speed mode (Scenario C), the stand-by power will be huge even in the normal mode. We certainly need another method to suppress the stand-by current. Figure 7 shows a schematic of the device/circuit scheme where high-speed mode VTCMOS is combined with a leak cut-off switch such as boosted gate MOS (BGMOS)[10] and super cut-off CMOS (SCCMOS).[11] The high-speed VTCMOS in combination with a low stand-by scheme would be one of the most promising device/circuit schemes that can attain high-speed and low stand-by power at the same time in the future.

5. Conclusions

The optimum device parameters and scalability of VTCMOS are discussed. The optimum body effect factor depends on the relationship between the substrate bias and the supply voltage. Although the scaling scenario of low stand-by power VTCMOS will fail, high-speed VTCMOS will take advantage in the combination with another low stand-by scheme.

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