High Drive-Current Electrically Induced Body Dynamic Threshold SOI MOSFET (EIB-DTMOS) with Large Body Effect and Low Threshold Voltage

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***Abstract*—A novel electrically induced body dynamic threshold metal oxide semiconductor (EIB-DTMOS) is proposed where the body is electrically induced by substrate bias and its high performance is demonstrated by experiments and simulations. EIB-DTMOS achieves a large body effect and a low V_{th} at the same time. The upper limit of the supply voltage of the EIB-DTMOS is higher than that of a conventional DTMOS, because the forward biased p–n junction leakage current of the EIB-DTMOS is lower. Among several DTMOSs, the accumulation mode EIB-DTMOS shows the highest drive-current at fixed off-current due to a large V_{th} shift (or large back gate capacitance) and a suppressed short channel effect.**

***Index Terms*—Body effect, DTMOS, low power, low voltage, SOI MOSFET.**

I. INTRODUCTION

THE REDUCTION of the supply voltage of a MOSFET is essential to decrease CMOS power consumption. However, as the supply voltage is reduced, it becomes very difficult to realize both a high drive-current and a low off-current. Therefore, the top priority in a low power device design is high drive-current at low off-current and low supply voltage. The dynamic threshold MOSFET (DTMOS) [1]–[8], where the gate is connected to the body, can realize both high drive-current and low off-current at very low supply voltage below 0.6 V, because it has an ideal subthreshold slope and a high drive-current. DTMOS circuit operation at 0.5 V supply voltage is also demonstrated [9]–[11].

In [1], [2], [4], [7]–[10], the higher drive-current of the DTMOS than that of the conventional MOSFET is explained by its "dynamic threshold voltage," where the threshold voltage (V_{th}) is dynamically changed by a positive body to source bias ($V_{bs}(=V_{gs})$). To enhance the drive-current of the DTMOS, a large body effect is essential [3], because the gate drive of the DTMOS is increased by $\Delta V_{th}(=V_{th(Vbs=0\text{ V})}-V_{th(Vbs=Vdd)})$ compared with a conventional MOSFET. It is interesting that the requirements for the body effect in a DTMOS and a normal MOSFET are opposite [12]. In a normal MOSFET, a small body effect is desirable to avoid a high electric field perpendicular to the channel and a reverse body effect in stacked circuits.

Manuscript received July 27, 2000; revised March 2, 2001. This work was supported in part by the Japan Society for the Promotion of Science (JSPS) Research for the Future Program and by the Grant-in-Aid for Scientific Research on Priority Areas, "Ultimate Integration of Intelligence on Silicon Electronic Systems" from the Ministry of Education, Science, Sports, and Culture. The review of this paper was arranged by Editor M. Hirose.

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Publisher Item Identifier S 0018-9383(01)05746-X.

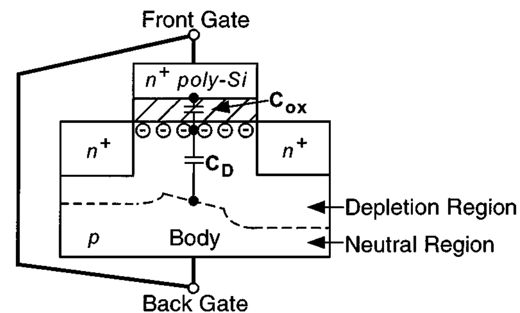

Fig. 1. Interpretation of the DTMOS as a kind of "double gate MOSFET." In DTMOSs, a single channel is induced not only by an n$^+$ poly-Si gate but by a neutral region (body), because the gate is connected to the body.

Another interpretation of the higher drive-current of a DTMOS compared with that of a conventional MOSFET is to consider the DTMOS as a kind of "double gate MOSFET" as shown in Fig. 1. A single channel is induced by both the front gate and the back gate. The front gate capacitance (C_{ox}) is a normal gate oxide capacitance, and the back gate capacitance (C_D) is a forward biased p–n junction capacitance between the channel and the neutral body region. The total gate capacitance of DTMOS is $C_{ox}+C_D$, and $(1+\gamma)$ times as large as that of a conventional MOSFET [2], when the body effect factor (γ) is defined as

$$\gamma \equiv \left|\frac{\Delta V_{th}}{\Delta V_{bs}}\right| = \frac{C_d}{C_{ox}} \propto \frac{t_{ox}}{l_d} \tag{1}$$

where l_d is the channel depletion layer width and t_{ox} is the gate oxide thickness. Therefore, a large γ leads to a large drive-current of the DTMOS.

However, it is very difficult to attain a large γ at a low V_{th}, because γ is determined primarily by the ratio of gate oxide thickness (t_{ox}) to channel depletion layer width (l_d) which is reduced by a high channel doping concentration. Previously reported DTMOSs [1], [2], [4], [8] have small values of $\gamma(0.2-0.3)$ due to the low V_{th} (0.3 V) for a low supply voltage and do not take full advantage of the high drive-current inherent to the DTMOS.

In this study, we propose a novel Electrically Induced Body DTMOS (EIB-DTMOS) which achieves a large γ and a low V_{th} at the same time. A thin SOI layer thickness provides a very

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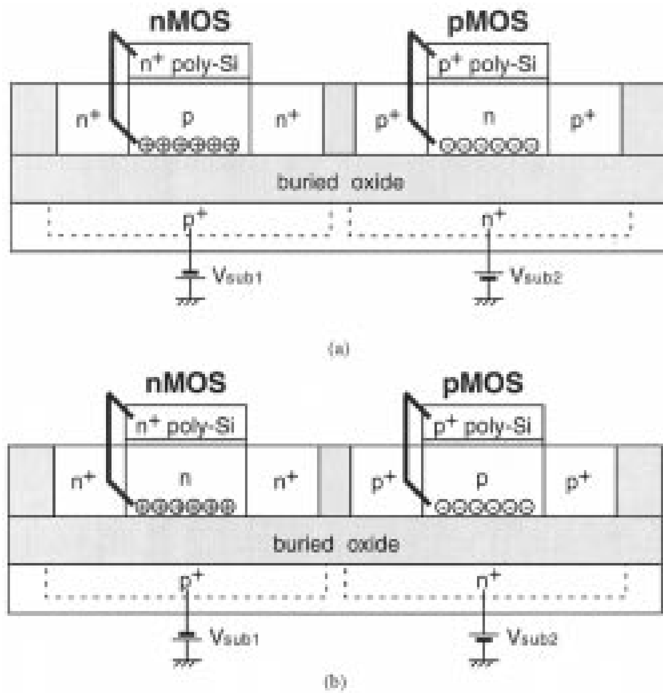


Fig. 2. Schematic cross sections of the proposed EIB-DTMOSs. The gate electrode is connected to the body. (a) Inversion mode. (b) Accumulation mode.

large γ, while V_{th} is determined by impurity concentration in the SOI layer. Experimental and simulation results demonstrate the superiority of the EIB-DTMOS to the conventional DTMOS and the normal SOI MOSFET. γ is as high as 0.8–1 and V_{th} can be set to around 0.1 V.

II. Proposed EIB-DTMOS

A. Device Structure of EIB-DTMOS

Fig. 2 shows a schematic cross-section of the proposed EIB-DTMOS in the inversion mode and in the accumulation mode. They have different types of dopant in the SOI layer. The body region is electrically induced (accumulated in the inversion mode and inverted in the accumulation mode) by a large static substrate bias at the back-interface in the SOI layer. In EIB-DTMOSs the gate is tied to this electrically induced body (EIB) via a body contact terminal. In the case of the inversion mode EIB-DTMOS the conducting channel is induced by inversion, and in the case of the accumulation mode EIB-DTMOS the conducting channel is induced by accumulation. If a large substrate voltage is not applied, the inversion mode EIB-DTMOS operates as the fully depleted SOI MOSFET shown in Section III, and the accumulation mode EIB-DTMOS operates as a MOSFET with punch-through. Both the inversion mode and the accumulation mode EIB-DTMOSs are enhancement mode devices. In the accumulation mode EIB-DTnMOS, holes which form the EIB are supplied from the p^+ body contact region. We show in Section IV that the accumulation mode EIB-DTMOS is the best type of DTMOS.

B. Possible Implementations of EIB-DTMOS

The layout of masks for p^+/n^+ doped substrates below the buried oxide in an EIB-DTMOS is the same as that for p/n doped wells in a normal bulk MOSFET. However, the distance between p^+ and n^+ doped substrates needs to be increased to avoid reverse bias p–n junction breakdown. Another measure is deep trench isolation between p^+ and n^+ doped substrates. Complementary doping of substrates can be done by ion implantation through the buried oxide [13], [14]. Contacts to the p^+/n^+ doped substrates are fabricated through STI (or LOCOS) and the buried oxide [13], [14]. Complementary large static substrate biases are supplied externally or generated within the chip.

TABLE I
Measurement Method of SOI nMOSFETs for Three Operation Modes

Operation Mode	V_{bs}	V_{sub}
FD SOI MOSFET	0V	0V
PD SOI MOSFET	0V	-20V
Inversion mode EIB-DTMOS	$=V_{gs}$	-20V

C. Large Body Effect Factor in EIB-DTMOS

As shown in (1), a large body effect factor (γ) can be obtained by the reduction of channel depletion layer width (l_d) at fixed gate oxide thickness. In a conventional DTMOS, l_d is determined both by the channel profile and by the channel doping concentration. In an EIB-DTMOS, however, l_d is determined only by the SOI thickness. Therefore, by thinning the SOI thickness, the EIB-DTMOS can reduce l_d and realize a larger γ and thus, a higher drive-current, than the conventional DTMOS. Reduced l_d also leads to a suppressed short channel effect.

For low voltage DTMOS design, not only large γ but also low V_{th} are important. In a uniformly doped channel MOSFET, γ and V_{th} are closely related and large γ leads to high V_{th}. In order to determine γ and V_{th} independently, the channel profile must be optimized. Large γ at low V_{th} can be obtained by counter doping and an abrupt low-high step channel profile for the body [3]. In the conventional DTMOSs, the channel profile is determined by impurity doping and subsequent impurity diffusion, and it is difficult to obtain a steep low-high step channel profile. Larger γ at lower V_{th} in an indium channel DTMOS compared with a BF_2 channel DTMOS has been experimentally demonstrated [8]. In an EIB-DTMOS, however, channel profile is determined electrically and ideal abrupt low-ultra-high step channel profile is realized, which is steeper than in any other conventional DTMOS. Therefore, the EIB-DTMOS can realize the largest γ at the lowest V_{th}.

III. Experimental

The inversion mode EIB-DTMOS is compared with conventional fully depleted (FD) and partially depleted (PD) SOI MOSFETs by experiment. The devices measured are fully depleted SOI nMOSFETs with body contacts fabricated on a SIMOX wafer [15]. The thicknesses of the gate oxide, the SOI, and the buried oxide are 10 nm, 40 nm, and 100 nm, respectively. An n^+ poly Si gate is used and the SOI layer is p-type with a concentration of the order of 10^{16} cm^{-3}.

A MOSFET is measured in three different modes (FD, PD, and EIB-DTMOS) by changing the bias conditions shown in Table I. When $V_{bs} = 0$ V and $V_{sub} = 0$ V, the entire SOI layer

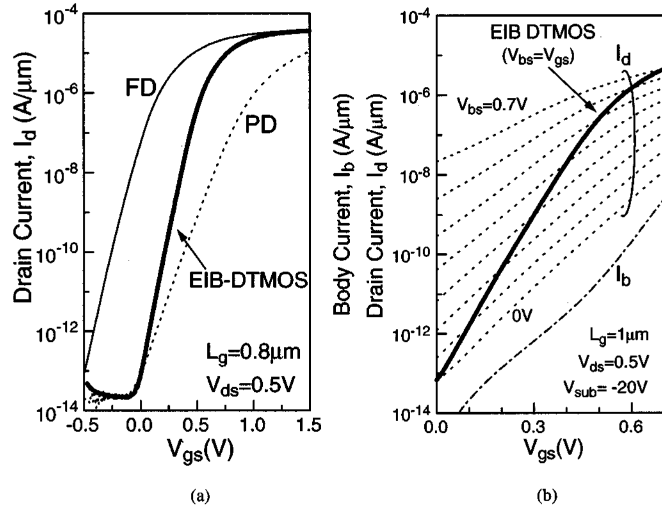


Fig. 3. (a) Measured subthreshold characteristics of a FD SOI MOSFET, a PD SOI MOSFET, and an inversion mode EIB-DTMOS. A SOI nMOSFET with gate length of 0.8 μm is measured by changing bias conditions as shown in Table I. (b) The measured subthreshold characteristics of an EIB-DTMOS (solid line) and a PD SOI MOSFET (dotted lines). In the PD, V_{bs} is varied from 0 V to 0.7 V in 0.1 V steps. The body current (=gate current) of the EIB-DTMOS is also shown.

is depleted and the devices operate in the FD SOI MOSFET mode. When $V_{bs} = 0$ V and $V_{sub} = -20$ V, holes are accumulated at the back-interface and the devices operate in the PD SOI MOSFET mode. When the gate is tied to the body ($V_{bs} = V_{gs}$) and $V_{sub} = -20$ V, they operate in the inversion mode EIB-DTMOS mode.

Fig. 3(a) shows subthreshold characteristics in the three modes. The EIB-DTMOS has a steep subthreshold slope. Fig. 3(b) shows the subthreshold characteristics of the EIB-DTMOS and the PD SOI MOSFET where V_{bs} is varied from 0 V to 0.7 V by 0.1 V steps. In a PD SOI MOSFET, V_{th} is lowered with increased V_{bs} due to the body effect. The EIB-DTMOS has the same γ as a PD SOI MOSFET, because they have identical device structures. Therefore γ for an EIB-DTMOS is derived experimentally from the V_{bs} dependence of V_{th} in the PD SOI MOSFET. The derived γ from Fig. 3(b) is as high as 0.8, because the ratio of the gate oxide thickness to the SOI thickness is high. The body current (=gate current) of the EIB-DTMOS is also shown. Band-to-band tunneling current between the EIB and the drain is not observed.

Fig. 4 shows V_{th} rolloff and subthreshold slope degradation by the short channel effect. The EIB-DTMOS suppresses the short channel effect very well, because the potential of the back interface is fixed and the source/drain depletion layer width is reduced by a forward body bias in the DTMOS. The subthreshold slope of a PD SOI MOSFET is much worse compared with a FD SOI MOSFET even for long channel devices because of the different effective channel depletion layer widths (l_D). In FD SOI MOSFET, the effective l_D that determines the subthreshold slope is more than 140 nm, because the effective l_D is the sum of the SOI thickness (40 nm), the buried oxide thickness (100 nm), and the depletion layer width below the buried oxide. On the other hand, in a PD SOI MOSFET, l_D is 40 nm, because l_D is determined by the SOI thickness. In a DTMOS, the subthreshold slope is steep irrespective of l_D. In Fig. 5, drive-current versus off-current characteristics are compared. In each device, the gate length is changed. In this figure, the supply voltage is not 0.5 V but 1.5 V just for comparison, because V_{th} of PD SOI MOSFET is 0.9 V. Under supply voltage of 1.5 V, large body current was actually observed in EIB-DTMOS. Nevertheless its value was measured to be only 7.1% and 0.79% of the corresponding drive-current values in our 1 μm and 0.15 μm EIB-DTMOS devices, respectively. Moreover, practical body current value is considered to be by orders of magnitude smaller than its drive-current because the normal supply voltage for the DTMOS operation should be 0.5–0.6 V. The EIB-DTMOS shows a high drive-current and a low off-current due to a high γ and a steep subthreshold slope. These experimental results show that the EIB-DTMOS is superior to conventional FD and PD SOI MOSFETs.

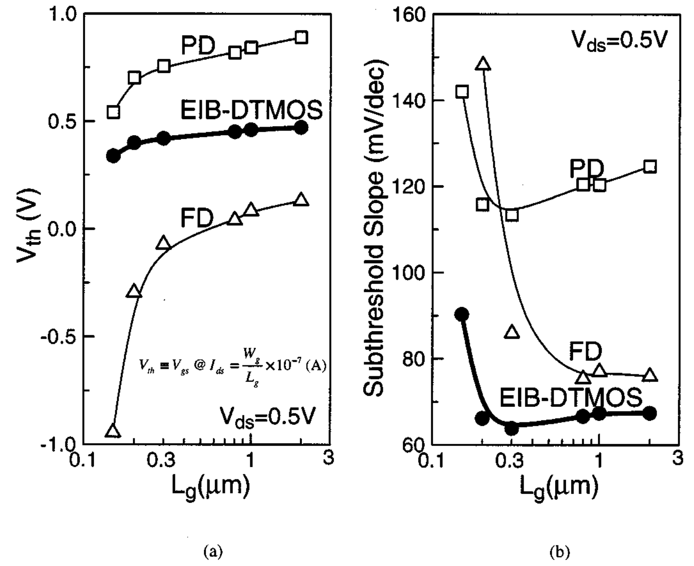


Fig. 4. Gate length dependence of V_{th} and the subthreshold slope in a FD SOI MOSFET, a PD SOI MOSFET, and an EIB-DTMOS (measured). The definition of V_{th} is shown in the inset.

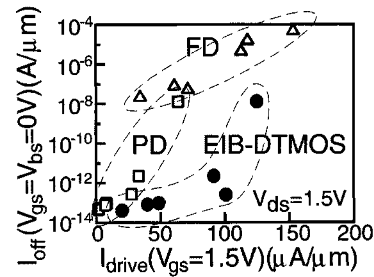


Fig. 5. Drive-current versus off-current characteristics in a FD SOI MOSFET, a PD SOI MOSFET, and an EIB-DTMOS (measured). In each device, the gate length is changed.

IV. Comparison with Conventional DTMOSs by Simulation

In order to demonstrate advantages of the EIB-DTMOS, four types of DTMOS shown in Fig. 6 are compared by device simulation [16]. Fig. 6(a) is a conventional DTMOS (Conv) [1]–[11],

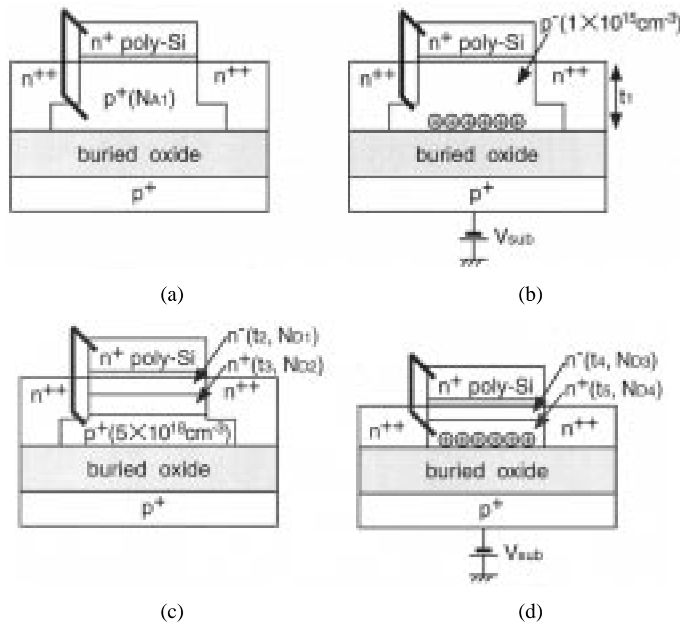


Fig. 6. Four types of DTMOS compared by device simulation: (a) conventional DTMOS (Conv), (b) inversion mode EIB-DTMOS (Inv EIB), (c) counter doped DTMOS (Count), and (d) accumulation mode EIB-DTMOS (Acc EIB). (a)–(b) inversion mode devices; (c)–(d) accumulation mode devices. (b), (d) proposed in this study. $t_2 = t_4 = 5$ nm, $t_5 = 10$ nm, $N_{D1} = N_{D3} = 1 \times 10^{17}$ cm^{-3}, $N_{D2} = 5 \times 10^{18}$ cm^{-3}. N_{A1}, t_1, t_3, N_{D4} are varied.

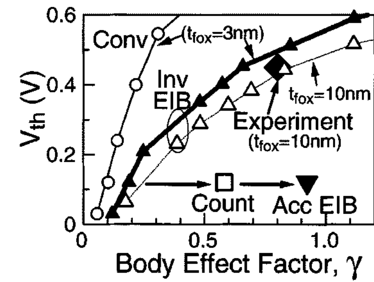


Fig. 7. Body effect factor (γ) dependence of V_{th} determined by the simulations for four types of DTMOS at long channel length as shown in Fig. 6. In the conventional DTMOS and the inversion mode EIB-DTMOS, both γ and V_{th} are varied by changing the channel doping concentration (N_{A1}) and the SOI thickness (t_1), respectively. The gate oxide thickness is 3 nm. The experimental result for the inversion mode EIB-DTMOS with a gate oxide thickness of 10 nm is also plotted. In the inversion mode EIB-DTMOS, the simulation results with a gate oxide thickness of 10 nm are also shown to compare with the experimental result.

Fig. 6(b) is the inversion mode EIB-DTMOS (Inv EIB), Fig. 6(c) is a counter doped DTMOS (Count) [3], and Fig. 6(d) is the accumulation mode EIB-DTMOS (Acc EIB). The conventional DTMOS and the inversion mode EIB-DTMOS are inversion mode devices, and the counter doped DTMOS and the accumulation mode EIB-DTMOS are accumulation mode devices. The gate oxide thickness is 3 nm, the buried oxide thickness is 20 nm, the supply voltage is 0.5 V, and the extension junction depth is 15 nm in all cases. A static substrate bias for the EIB-DTMOS is -12 V.

A. Inversion Mode DTMOSs

Two inversion mode devices are discussed here. In the conventional DTMOS shown in Fig. 6(a), a uniformly doped p type channel is assumed and the SOI layer is partially depleted. In the inversion mode EIB-DTMOS shown in Fig. 6(b), a very lightly doped p type channel is assumed. Fig. 7 shows the dependence of V_{th} on γ for the conventional DTMOS and the inversion mode EIB-DTMOS at long channel length. The channel doping concentration (N_{A1}) is varied in the conventional DTMOS, and the SOI thickness (t_1) is varied in the inversion mode EIB- DTMOS. High N_{A1} and small t_1 result in high V_{th} and large γ due to the reduced channel depletion layer width at fixed gate oxide thickness. γ for the inversion mode EIB-DTMOS is two times as large as that for the conventional DTMOS at fixed V_{th}, because l_D of the inversion mode EIB-DTMOS is half that of the conventional DTMOS [17]. This is due to the same theory as that where a uniformly doped channel MOSFET and an ideal step channel MOSFET are compared [18], [19]. The experimental result for the inversion mode EIB-DTMOS ($V_{th} = 0.45$ V, $\gamma = 0.8$) in Section III is also plotted, and it fits the simulation results very well. However, V_{th} of the experimental result is too high for supply voltages below 0.5 V. If V_{th} is decreased, γ is also decreased as shown in Fig. 7. Even in the inversion mode EIB-DTMOS, therefore, a large γ can not be attained at low V_{th}.

B. Accumulation Mode DTMOSs

To realize both large γ and low V_{th}, the accumulation mode DTMOSs shown in Fig. 6(c) and (d) are required. In the accumulation mode EIB-DTMOS, a whole SOI layer is doped by n-type dopants for low V_{th} and the body is composed of holes generated by inversion at the back interface. The conventional counterpart of the accumulation mode EIB-DTMOS is the counter doped DTMOS [3]. The counter doped DTMOS has a shallow n-type doped channel region for low V_{th} and a deep p-type doped channel region for the body. In both devices, the surface regions in the SOI layer are lightly doped to avoid mobility degradation by impurity scattering.

The difference between the counter doped DTMOS and the accumulation mode EIB-DTMOS is discussed in the following. In the accumulation mode EIB-DTMOS, the body region is formed by electrically inverted carriers and l_D is limited by a thin SOI thickness. The carrier concentration of the body (holes for nMOS) could be very high and a very steep low-high step carrier profile is achieved. On the other hand, in the counter doped DTMOS, not only the counter doped region but also the body region are formed by the doping. The body concentration is limited and it is very difficult to obtain a steep low-high carrier profile. Therefore, the accumulation mode EIB-DTMOS can realize larger γ at lower V_{th} than the counter doped DTMOS. These are the same discussions as those in Section II-C.

The channel donor concentration (N_{D4}) in the accumulation mode EIB-DTMOS is an important device parameter and needs to be optimized. Fig. 8 shows N_{D4} dependence of V_{th} and γ. By increasing N_{D4}, V_{th} is lowered and γ is increased because the operation mode is changed from surface channel to buried channel. Low V_{th} and large γ result in a higher drive-current. However, too high N_{D4} results in punch-through, which is not shown in Fig. 8. Therefore, N_{D4} of 1×10^{19} cm^{-3} is used in the following.

γ value for the counter doped DTMOS and the accumulation mode EIB-DTMOS are also plotted in Fig. 7. At V_{th} of 0.12 V,

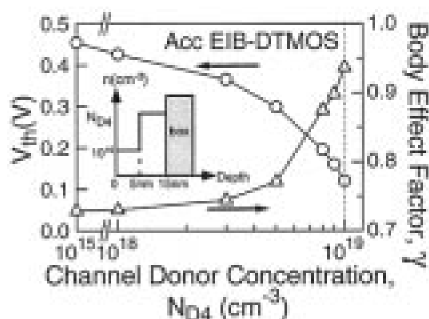


Fig. 8. Channel donor concentration (N_{D4}) dependence of V_{th} and γ in the accumulation mode EIB-DTMOS (simulated). The inset shows the channel concentration profile. N_{D4} is also shown.

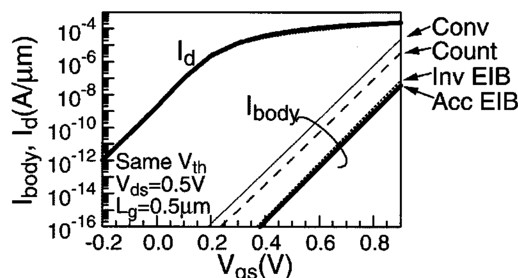


Fig. 9. Gate voltage dependence of drain current and body current in four types of DTMOS with the same V_{th} at a gate length of 0.5 μm by changing device parameters (simulated). $N_{A1} = 3.1 \times 10^{16}$ cm^{-3}, $t_1 = 89$ nm, $t_3 = 8.7$ nm, $N_{D4} = 1 \times 10^{19}$ cm^{-3}. Other device parameters are shown in the caption of Fig. 6. Subthreshold current characteristics of the four DTMOSs are completely the same.

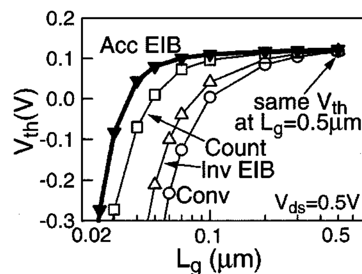
γ of the inversion MOSFETs is as low as 0.1–0.2. However, γ of the counter doped DTMOS is 0.58, and γ as high as 0.92 is achieved in the accumulation mode EIB-DTMOS.

C. Junction Leakage Current

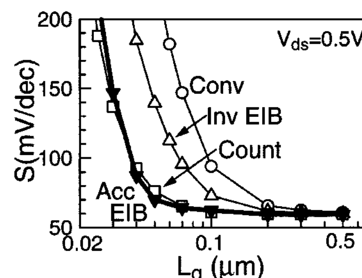
One of the most serious problems in DTMOSs is an upper limit of supply voltage due to a forward biased p–n junction leakage current. Fig. 9 shows forward biased p–n junction current in four types of DTMOS. The devices have the same V_{th} by changing N_{A1}, t_1, t_3, and N_{D4} in Fig. 6. The inversion mode and the accumulation mode EIB-DTMOSs show the smallest leakage current due to a very small junction area and a high hole concentration. Therefore, the upper limit of supply voltage of EIB-DTMOSs is higher than that of conventional DTMOS. For example, the upper limit of supply voltage ($V_{dd(\max)}$) is defined as $V_{gs}(=V_{bs})$ when the body current is equals to drain current at $V_{gs} = 0$ V. In Fig. 9, while $V_{dd(\max)}$ of the conventional DTMOS is 0.65 V, $V_{dd(\max)}$ of the EIB-DTMOS is increased to 0.82 V. When the SOI thickness is thinned below 10 nm in EIB-DTnMOSs to scale down the gate length, the leakage current may increase due to direct tunneling between electrons at the front interface and holes at the back interface [20].

D. Short Channel Effect

Fig. 10 shows V_{th} rolloff and subthreshold slope degradation for four types of DTMOS with a V_{th} of 0.12 V at a gate length of 0.5 μm. The device structures and the device parameters except for the gate length are the same as in Fig. 9. The gate length of



(a)



(b)

Fig. 10. Dependence of V_{th} on L_g, and the subthreshold slope in four types of DTMOS with the same V_{th} at a gate length of 0.5 μm (simulated). Device parameters are the same as for Fig. 9.

each DTMOS is varied. The short channel effect of the accumulation mode EIB-DTMOS is the smallest, because the channel depletion layer width (=SOI thickness) is the smallest.

E. Drive-Current Versus Off-Current

Fig. 11(a) shows drive-current versus off-current characteristics of the devices shown in Fig. 10, where they have the same V_{th} at a gate length of 0.5 μm. Although the drive-current for the four types of DTMOS is almost the same at fixed gate length, the accumulation mode EIB-DTMOS shows three decades less off-current than the conventional DTMOS at a gate length of 0.07 μm due to the suppressed short channel effect. Fig. 11(b) shows drive-current versus off-current characteristics of the conventional DTMOS, the inversion mode EIB-DTMOS, and the accumulation mode EIB-DTMOS, where the device parameters are changed to have the same off-current at a gate length of 0.07 μm. At a gate length of 0.07 μm, the accumulation mode EIB-DTMOS shows one and a half times as high drive-current as the conventional DTMOS due to a large γ and much less drain-induced-barrier-lowering (DIBL) as shown in the inset of Fig. 11(b). These results indicate that the accumulation mode EIB-DTMOS has a better performance than any of the other DTMOSs under any conditions.

F. Gate Delay

Finally, we compare the AC characteristics of the three types of DTMOS shown in Fig. 11(b) by two-dimensional (2-D) mixed-mode simulations of a three-stage inverter chain [16]. Fig. 12 shows the wire capacitance dependence of the gate delay. The supply voltage is 0.5 V, the gate length is 0.07 μm, and the gate width is 0.5/1 μm for nMOS/pMOS. The accumulation mode EIB-DTMOS is the fastest due to a higher drive-current and a lower junction capacitance.

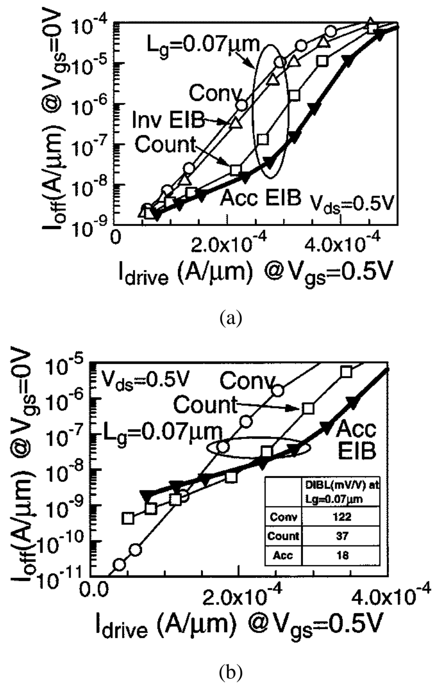


Fig. 11. (a) Drive-current versus off-current characteristics of the devices shown in Fig. 10, where they have the same V_{th} at a gate length of 0.5 μm (simulated). (b) Drive-current versus off-current characteristics of the conventional DTMOS, the counter doped DTMOS, and the accumulation mode EIB-DTMOS, where device parameters are changed to have the same off-current at a gate length of 0.07 μm (simulated). $N_{A1} = 2 \times 10^{17}$ cm^{-3}, $t_3 = 8$ nm, $N_{D4} = 1 \times 10^{19}$ cm^{-3}. The inset shows the DIBL at a gate length of 0.07 μm.

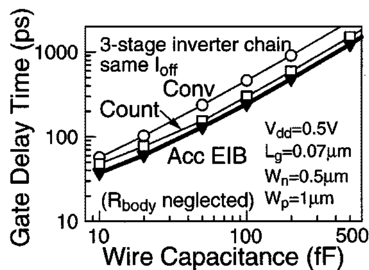


Fig. 12. Wire capacitance dependence of the inverter delay in the conventional DTMOS, the counter doped DTMOS, and the accumulation mode EIB-DTMOS (simulated). Device parameters are the same as for Fig. 11(b). The effect of the body RC delay is not included.

V. Body Resistance Problem in DTMOSs

DTMOSs have a distributed body resistance in the gate width direction, because the body contact is located at the sides of the body. Body RC delay is a serious problem in a DTMOS with wide gate width (W_g), because the body potential does not follow the gate voltage and differs in the gate width direction for ac operation [2]–[4], [6], [7], [21]. Although the body RC delay problem is similar to the gate RC delay problem, the body RC delay is much larger than the gate RC delay, because the body sheet resistance is 1 k–100 kΩ/sq. compared with 1–10 Ω/sq. in gate sheet resistance. In Fig. 12, the effect of the body resistance is negligible because W_g is narrow. When W_g is wider, the body RC delay becomes comparable to the gate delay and the body potential does not follow the gate voltage, resulting in a slower propagation delay. When W_g is much wider and the body RC delay is much longer, the body potential will depend strongly on the history of the input and output voltages and will vary between 0 V and V_{dd}. In such a case, a history dependent propagation delay and a large power consumption due to low V_{th} would be expected [21].

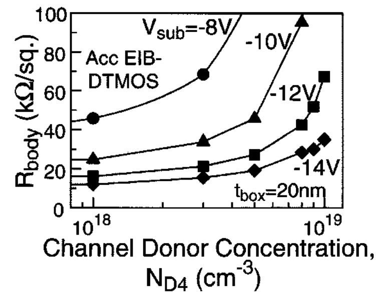


Fig. 13. Channel donor concentration (N_{D4}) dependence of the body sheet resistance in the accumulation mode EIB-DTMOS with several substrate biases (simulated).

The EIB-DTMOS also has a serious body RC delay. The body capacitance of EIB-DTMOSs is much lower than that of a conventional DTMOSs, because the p-n junction area is very small. However, the EIB-DTMOS has a higher body resistance (10 k–100 kΩ/sq.) than the conventional DTMOS (5 k–50 kΩ/sq.) or bulk DTMOS (1 k–10 kΩ/sq.) [6], because the body is electrically induced only at the SOI/buried oxide interface. Fig. 13 shows the channel donor concentration (N_{D4}) dependence of the body sheet resistance in the accumulation mode EIB-DTMOS with several substrate biases. As shown in Fig. 8, a high N_{D4} is desirable for a large γ and a low V_{th}. However, a high N_{D4} also leads to an increased body resistance, because the back-interface is not sufficiently inverted at a given negative substrate bias. To decrease the body resistance, a higher substrate bias is needed but causes a reliability problem in the buried oxide. For example, when N_{D4} is 1×10^{19} cm^{-3} and required body sheet resistance is the same as the worst case of the conventional DTMOS (50 kΩ/sq.), a substrate bias of -12 V is needed, which results in a buried oxide electric field of 6 MV/cm. Therefore, in the accumulation mode EIB-DTMOS, there is a trade-off between the reduction of the body resistance and the reliability of the buried oxide. A low/high/low channel profile in the SOI layer alleviates the problem.

In order to solve the body RC problem, an upper limit on the W_g/L_g ratio must be set. A DTMOS with a large W_g should have multiple-finger gate layouts with each body contact, and interdigitated source and drain regions. When a DTMOS is divided into n narrow DTMOSs with respective body contacts, the body RC delay is decreased at the rate of $1/n^2$. Fig. 14 shows the dependence on the number of divided DTMOSs of the gate delay including the body RC delay by 3-dimensional device and circuit mixed-mode simulations [22]. The devices used are almost the same as the accumulation mode EIB-DTMOS in Fig. 12 except for W_g. The total W_g is 5 (10) μm for nMOS (pMOS). Devices with both a one side body contact and both sides body contact are shown. The supply voltage is 0.5 V, the gate length is 0.07 μm, the load capacitance is 100 fF, and the interconnect resistance is 50 Ω. By increasing the finger length, the gate delay also increases due to an increased body RC delay. The gate delay without the body RC delay is 40 ps, determined by 2-D device and circuit mixed-mode simulations [16]. Fig. 14

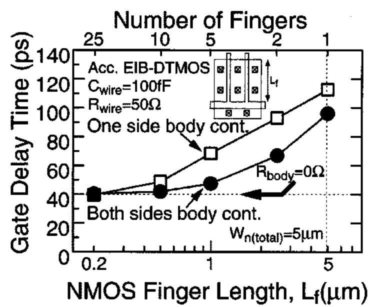


Fig. 14. NMOS finger length dependence of gate delay including the body RC delay, deduced by three-dimensional (3-D) device and circuit mixed-mode simulations (simulated). Upper axis shows the number of fingers corresponding to the finger length. The inset shows an example of a two-finger gate layout and the definition of the finger length.

shows that the influence of the body RC delay is observed only when $W_g/L_g > 10$ in the accumulation mode EIB-DTMOS with a both sides body contact, which is not a serious issue in logic circuits. The critical W_g/L_g ratio is determined by a relative relation between the circuit delay and the body RC delay.

Finally, a change of the influence of the body RC delay on the gate delay is considered in EIB-DTMOSs with scaling-down. The major part of the body capacitance is the lateral abrupt p–n junction capacitance between the EIB and the source/drain, because the upper capacitance between the EIB and the gate is negligible in a DTMOS and the lower capacitance between the EIB and the substrate is small when the buried oxide is thick. In EIB-DTMOSs, the body resistance is proportional to W_g/L_g because of the constant sheet resistance of the EIB, and the lateral abrupt p–n junction capacitance between the EIB and the source/drain is proportional to W_g because of the constant thickness of the EIB. Therefore, the body RC delay in EIB- DTMOSs is proportional to W_g^2/L_g. The gate delay is proportional to L_g. It is assumed that W_g is scaled-down at the same rate as L_g. Once a critical W_g/L_g ratio which does not suffer from the body RC delay is found, the gate delay of a future scaled-down EIB-DTMOS with the same W_g/L_g ratio will not be degraded by the body RC delay.

VI. Conclusion

We have proposed a low power high drive-current EIB-DTMOS with a large body effect and a low V_{th}, and its high performance has been demonstrated by experiments and simulations. An ideal low-ultra-high step channel profile made by an electrically induced body (EIB) with a high carrier concentration at the back interface and a thin SOI layer reduce the channel depletion layer width and achieve the maximum body effect at low V_{th}. The upper limit of supply voltage for EIB-DTMOSs is higher than that of the conventional DTMOS due to a reduced p-n junction leakage current. Among several DTMOSs, the accumulation mode EIB-DTMOS shows the highest drive-current at fixed off-current due to a large body effect factor and a suppressed short channel effect.

Acknowledgment

The authors would like to thank T. Saraya and T. N. Duyet for their great contribution to the fabrication of the devices used in this work.

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