A 6.7-fF/μm^2 Bias-Independent Gate Capacitor (BIGCAP) with Standard CMOS Process and its Application to the Loop Filter of a Differential PLL

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Abstract

A linear bias-independent gate capacitor (BIGCAP) with large intrinsic capacitance and low parasitic capacitance, which needs no additional fabrication process steps, is proposed. Measured results with 0.13-μm standard CMOS technology show that the intrinsic capacitance is 6.7 fF/μm^2 (6.7 times bigger than that of typical MIM capacitors) and the parasitic capacitance is 1.9% of the intrinsic capacitance (one-fifth that of typical MIM capacitors). The linearity is ±2.9% and capacitance variation across a wafer is as small as σ = 0.096%.

Applying BIGCAP to the loop filter of a differential PLL reduces the gate area of the MOS capacitor for the loop filter to only 35% of that of the conventional design without degrading the performance of the PLL. The measured jitter at 840 MHz was 7.0 ps (rms) and 74.4 ps (p-p) for 1.5-V supply.

1. Introduction

Bias-independent (i.e., linear) capacitors are needed for many applications such as the loop filter of a PLL, level-shift in I/O buffers, switched-capacitor circuits, phase-compensation in operational amplifiers, data converters, and mixers. Most of these applications employ MIM or poly-to-poly capacitors to retain high linearity at the cost of additional process steps and a large area due to the low capacitance-per-unit area (~ 1 fF/μm^2). Various MIM capacitors [1-2] that require no additional process steps show very low capacitance (0.2 ~ 0.3 fF/μm^2). Though the capacitance-per-unit area of the conventional MOS gate capacitors is one or two orders of magnitude higher, MOS gate capacitors cannot be applied to these applications because of their large nonlinearity.

This paper presents a linear area-efficient MOS gate capacitor with low parasitic capacitance that can be fabricated using a standard digital CMOS fabrication process. The bias-independent gate capacitor (BIGCAP) is applied to the loop filter of a differential PLL.

2. BIGCAP concepts and configurations

Figure 1 shows the configuration of BIGCAP, which is composed of a pair of accumulation-mode n-poly gate capacitors in an n-well and a pair of pMOS gate capacitors. The n-poly gate capacitors can be fabricated by replacing the p-well for nMOS by an n-well for pMOS in the standard CMOS process. In order to obtain symmetrical bias-dependence, i.e., bipolarity, both the n-poly gate capacitors have the same layout and only the connections are reversed. The same is true of the pMOS gate capacitors. As shown in Fig. 2(a), the pair of n-poly gate capacitors shows its maximum capacitance at 0 V, while the pair of pMOS gate capacitors (Fig. 2(b)) shows its minimum capacitance at 0 V. Therefore, by appropriately adjusting the area ratio between the n-poly and pMOS gate capacitors, we can achieve a very low dependence of capacitance on bias.

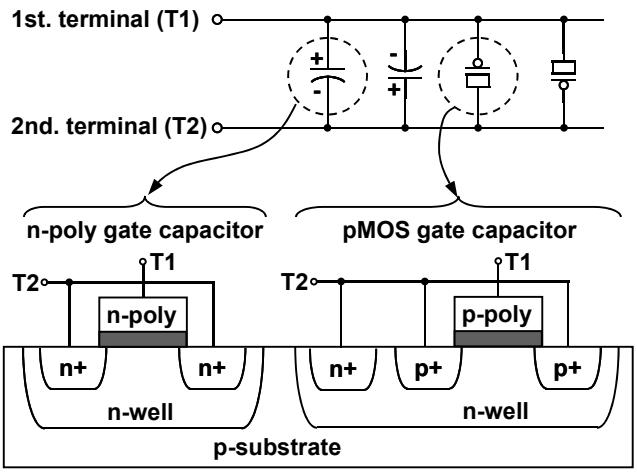

Figure 1. Configuration of BIGCAP. The bias dependence of the capacitance of the n-poly and pMOS gate capacitors cancel each other out.

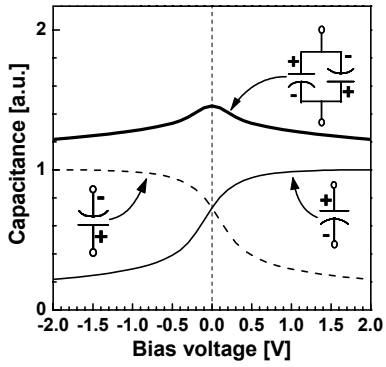

Figure 2. C-V characteristics. (a) The pair of n-poly gate capacitors. (b) The pair of pMOS gate capacitors.

3. Experimental results of BIGCAP

Figure 3 shows the dependence of the capacitance of BIGCAP on bias as measured at 100 kHz. The ratio (x) of the n-poly gate capacitors' area to that of the pMOS gate capacitors was varied by changing the area of the latter. Figure 4 shows the linearity extracted from Fig. 3. The smallest dependence of capacitance on bias appeared with $\pm$2.9% linearity from -2 V to 2 V, when the ratio (x) was 15%. This optimum ratio depends on each CMOS process. The intrinsic capacitance of BIGCAP was 6.7 fF/μm^2, which is 70% of the gate capacitance of 9.6 fF/μm^2 at inversion and 6.7 times as large as the typical MIM capacitor's value of 1.0 fF/μm^2.

Figure 5 shows an equivalent circuit of BIGCAP. The measured parasitic capacitance between the n-well and p-substrate of BIGMOS is as small as 1.9% of the intrinsic gate capacitance, which is smaller than the 11% reported in [1] and 6% reported in [2]. Figure 6 shows the calculated dependence of the relative parasitic capacitance (C_{para}) on the intrinsic capacitance (C_{int}) for various gate lengths (L_{gate}). Here, C_{para} is the parasitic capacitance over the intrinsic capacitance in percentage. Measured data is also plotted, and it fits the calculated results very well. A long L_{gate} achieves the smallest C_{para} for a large C_{int}, while a short L_{gate} achieves the smallest C_{para} for a small C_{int}, because, in the long-and-narrow layout, the area of the n-well is much larger than the gate area. These results indicate that there is an optimum L_{gate} to achieve the smallest C_{para} for a given C_{int} When C_{int} is larger than 100 fF, C_{para} is less than 4%.

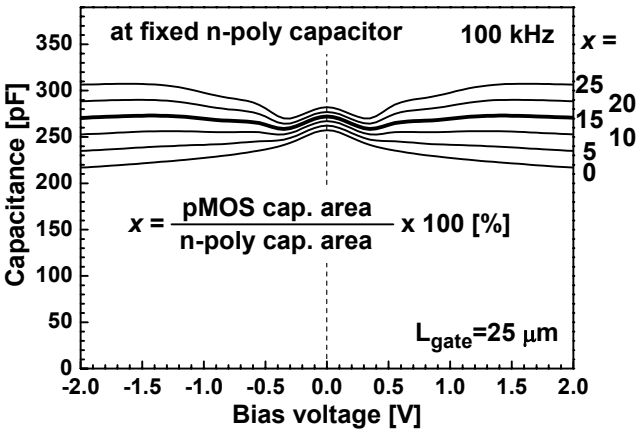

Figure 3. Measured C-V characteristics of BIGCAP for various values of x at a fixed area of the n-poly gate capacitors.

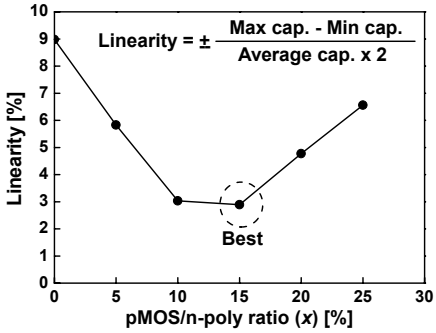

Figure 4. Dependence of the linearity on x extracted from Fig. 3.

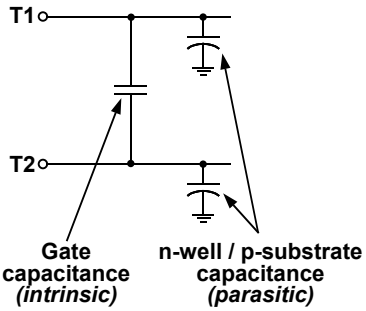

Figure 5. Equivalent circuit of BIGCAP.

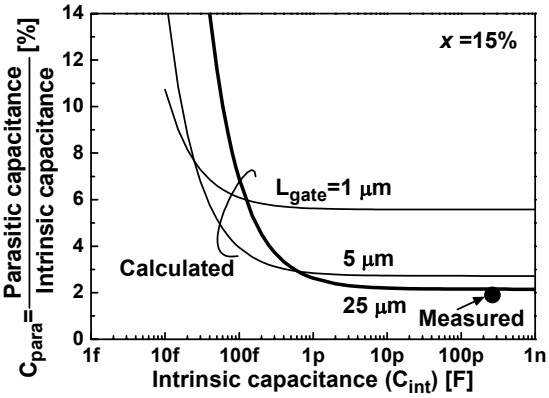

Figure 6. Calculated dependence of the relative parasitic capacitance on the intrinsic capacitance.

Fig. 7 shows the dependence of the Q-value of BIGCAP on frequency as measured with a network analyzer. The Q-value was 4 at 50 MHz and 217 pF. The Q-value normalized by frequency and capacitance was 43 / (f (GHz) C (pF)), which is sufficient for most applications.

The measured capacitance variation across the wafer was $\sigma = 0.096\%$, which is much smaller than the 1.5% reported in [1], because the capacitance of BIGMOS is determined by the gate oxide thickness, unlike the MIM capacitors. Figure 8 shows the measured bias dependence of the BIGCAP capacitance for different pMOS threshold voltages as the n-well doping concentration was changed. The capacitance variation was only $\sigma = 0.69\%$ for a 0.1 V threshold voltage variation.

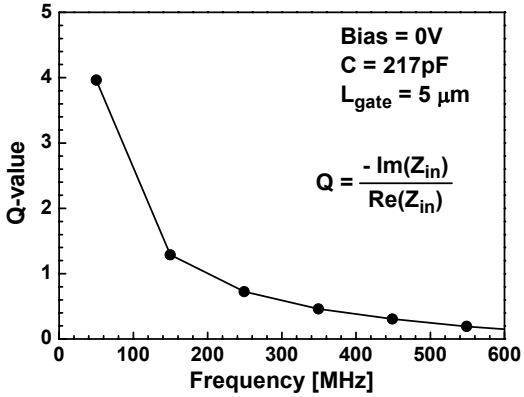

Figure 7. Measured Q-values of BIGCAP as a function of frequency.

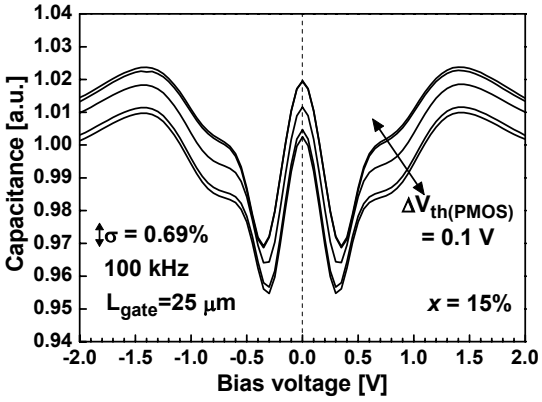

Figure 8. Measured C-V characteristics of BIGCAP for various pMOS threshold voltages.

4. Application of BIGCAP to the loop filter of a differential PLL

Recently, the differential PLLs are often used to avoid an increase in jitter due to the supply-noise. Figure 9 shows a block diagram of a differential PLL. Two outputs (V_{cnt}, V_{cntb}) of the two charge pump circuits are differential control voltages of VCO. The loop filter (LF) is connected between V_{cnt} and V_{cntb}. When one of the differential control voltages goes high, the other goes low. The common-mode feedback circuit keeps the common-mode of the differential control voltages.

Here, we discuss the capacitance of the LF in a differential PLL. Figure 10(a) shows the conventional configuration of the LF of a differential PLL, and Fig. 10(b) shows the proposed configuration. The conventional LF in Fig. 10(a) requires twice as much capacitance as the LF of a single-ended PLL. Therefore, the PLL area is nearly twice as large, because it is generally determined by the large capacitance of LF which is shown as C_Y in Fig. 10. If the capacitor used in the LF is bias-independent, C_Y can be inserted between V_{cnt} and V_{cntb} as shown in Fig. 10(b). In this case, the capacitance needed to achieve the same transfer function as in Fig. 10(a) is only $C_Y/2$ by the mirror effect, which is one-fourth the size of that in Fig. 10(a) and half the size of that of the single-ended PLL. However, the n-poly gate capacitor, which is widely used in LF, cannot be inserted between V_{cnt} and V_{cntb}, because the capacitance of the n-poly gate capacitor changes dramatically depending on whether the bias voltage is positive or negative. It has been reported that the proposed LF in Fig. 10(b) can be made by using a bias-independent poly-to-poly capacitor [3]. However, the area of the PLL is very large, because the capacitance-per-unit-area of the poly-to-poly capacitor is about one-tenth that of the n-poly gate capacitor. To solve this problem, BIGCAP is applied to the proposed LF in Fig. 10(b).

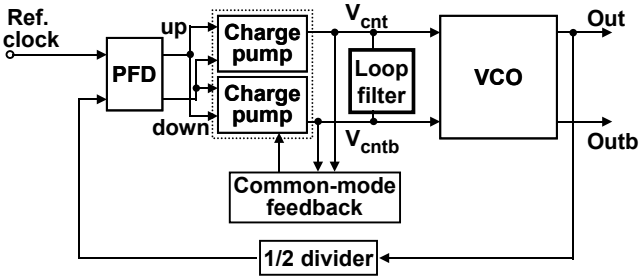

Figure 9. Block diagram of the differential PLL.

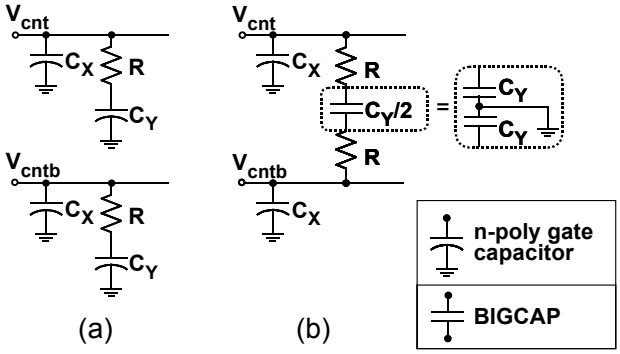

Figure 10. Configuration of the loop filter of the differential PLL. (a) Conventional configuration. (b) Proposed configuration. BIGCAP was used for C_Y in (b), and n-poly gate capacitors were used for the other capacitances.

A PLL with the proposed LF in Fig. 10(b) was fabricated by 1.5-V 0.13-μm CMOS. Figure 11 shows a micrograph of the fabricated PLL. BIGCAP was used for C_Y, and the n-poly gate capacitor was used for C_X in Fig. 10(b). Parameters of the fabricated LF were C_X = 5 pF, R = 0.5 kΩ, and $C_Y/2$ = 250 pF. As shown in Fig. 12, the measured jitter of the PLL with the proposed LF at 840 MHz was 7.0 ps (rms) and 74.4 ps (peak-to-peak) for a 1.5-V supply. Table 1 summarizes the gate area of the MOS capacitor for the LF for different LFs shown in Fig. 10. The area of the proposed LF is only 35% (= 0.5 × 0.70) of that of the conventional LF. It is 70% of that of a single-ended PLL. Therefore, by applying the BIGCAP to the LF, we can avoid an increase in PLL area when changing from the single-ended design to the differential design.

5. Conclusions

The proposed BIGCAP showed good linearity of ± 2.9%, large capacitance of 6.7 fF/μm^2, and as low as 1.9% relative parasitic capacitance without any additional fabrication processes on 0.13-μm standard CMOS technology. The Q-value was 43 / (f (GHz) C (pF)) and capacitance variation across a wafer was as small as σ = 0.096%.

By applying BIGCAP to the loop filter of a differential PLL, we reduced the gate area of MOS capacitor for the loop filter to only 35% of that of the conventional design without changing the transfer function of the PLL. BIGCAP is widely applicable to many other circuits such as I/O buffers, switched-capacitor circuits, operational amplifiers, data converters, and mixers.

6. Acknowledgements

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7. References

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[3] H. Djahanshahi and C. A. T. Salama, "Differential CMOS circuits for 622-MHz/933-MHz clock and data recovery applications," *IEEE J. of Solid-State Circuits*, vol. 35, pp. 847-855, June 2000.

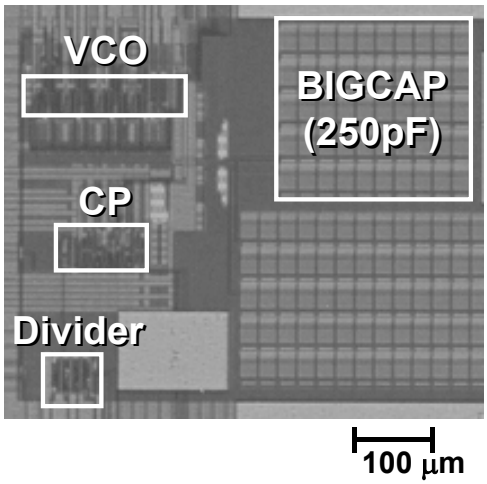

Figure 11. Micrograph of the fabricated PLL with the proposed loop filter shown in Fig. 10(b).

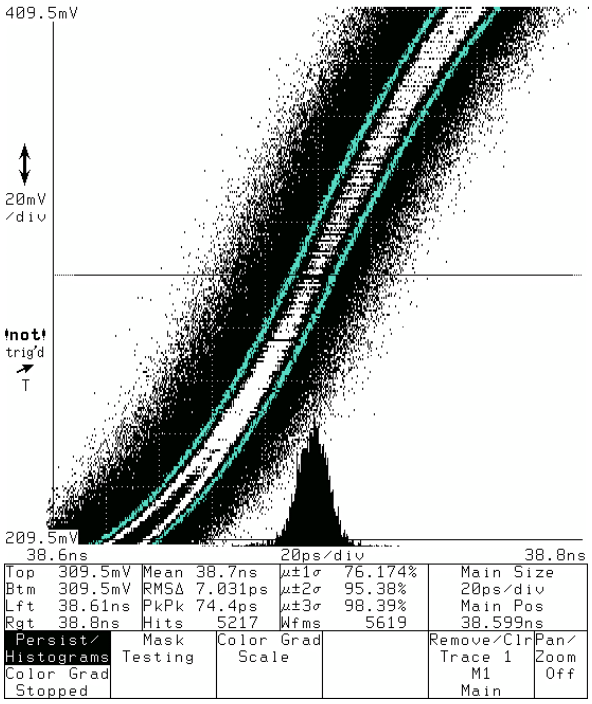

Figure 12. Measured jitter of the PLL with the proposed loop filter. The jitter at 840 MHz was 7.0 ps (rms) and 74.4 ps (p-p) for a 1.5-V supply.

Table 1. Summary of the gate area of MOS capacitor for the loop filter for the different loop filters shown in Fig. 10.

	Conventional LF w/o BIGCAP	Proposed LF with BIGCAP
Gate area of MOS capacitor for LF	0.104 mm^2 (100%)	0.0373 mm^2 (35%)