A Package-process-oriented Multilevel 5-μm-thick Cu Wiring Technology with Pulse Periodic Reverse Electroplating and Photosensitive Resin

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Abstract

A package-process-oriented multilevel 5-μm-thick Cu wiring technology has been developed for low resistance power supply wirings in high-speed ULSIs. A thick Cu wiring fabricated by pulse periodic reverse electroplating achieves the good thickness uniformity without CMP process. A photosensitive resin as interlayer dielectric eliminates dry etching steps. Three layers of thick Cu wirings have been successfully fabricated on the top of a 0.13-μm CMOS ULSI with three layers of 0.5μm-thick Al wiring. The total thick Cu wiring resistance is confirmed to be five times as small as that of the conventional two layers of 0.5-μm-thick Al wirings. This simple technology is suitable for future low-cost ULSI global wirings.

I. Introduction

It is generally expected to achieve smaller wiring pitch, higher operating speed (>3.1 GHz), larger chip area (>310 mm^2), larger number of flip-chip pads (>4000), and smaller area array flip-chip pad pitch (<0.15 mm) in future advanced ULSIs [1]. In contrast, the wiring pitch dimensions in ULSI packages are not scaled down so much, mostly because of the cost and registration accuracy issues. Therefore, as this trend proceeds, the following subjects should be taken into account: 1) the design rule mismatch between ULSIs and packaging substrates [2], and 2) the power supply voltage drop (IR-drop) in ULSI chips at high speed operation.

The design rule mismatch between ULSIs and packages makes it very difficult to produce high-density and fine-pitch advanced packaging substrates. The stable fabrication of the packaging substrate wirings smaller than 20 μm in width is especially difficult. Because of this mismatch, the flip-chip pad pitch on the surface of ULSIs should be expanded to fit the design rule of packaging substrates. Consequently, the number of wiring layers inside ULSIs increases unnecessarily, resulting in high chip fabrication cost.

The IR-drop in ULSI chips becomes larger for smaller pitch wiring, higher operating speed, and larger chip area. Power supply wiring and global interconnect resistance especially influence the IR-drop and signal delay [1]. Lower resistance wirings with larger width and thickness are needed for these wirings. Although present ULSIs have several layers of power supply wiring for the reduction of circuit resistance [3], the improvement in IR-drop is not sufficient.

To solve these problems, we have developed a package-process-oriented multilevel thick Cu wiring technology with electroplated Cu of the thickness of 5 μm and photosensitive resin without using CMP process, to replace conventional power supply wiring in high-speed ULSIs. Figure 1 shows the concept of our multilevel thick Cu technology. Since this technology has 20-μm-pitch Cu wiring with 5-μm thickness, it is expected to reduce the number of power or ground pads of ULSIs by connecting common circuits, in order to solve the design rule mismatch. Also, the IR-drop in ULSI chips is expected to be improved.

In this paper, we describe our thick Cu wiring process technology and discuss the IR-drop evaluation results.

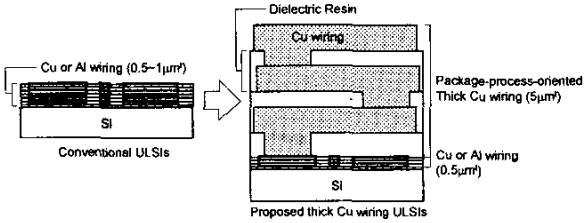

Fig. 1 Concept of thick Cu wiring technology

II. Multilevel thick Cu wiring technology

A. Multilevel wiring process

The thick Cu wiring technology is based on our packaging substrate technology, reported as deposited substrate on laminate (DSOL) previously [4]. The main features are pulse periodic reverse (PPR) Cu electroplating process and high-resolution photosensitive epoxy resin for interlayer dielectric. The former makes it possible to eliminate barrier metal layer used in conventional Cu interconnect, and to control Cu thickness on the wafer without CMP process. The latter contributes to develop low-cost process without using dry etching step.

Figure 2 shows our thick Cu wiring process for one layer. The photosensitive resin is coated on the wafer with CMOS transistors and several Cu or Al wiring layers. After photolithography for via-hole fabrication and curing, a seed layer is sputtered. Then, thick photoresist are patterned and Cu is plated by PPR Cu electroplating. Since the Cu thickness is fairly large, the photoresist thickness should be 10 μm. After stripping photoresist, the seed layer is removed by wet etching, and no CMP process is needed. An aligner-type exposure system is used to expose an entire 8-inch wafer

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simultaneously, so that the throughput and process cost are much better, compared to using an ordinary stepper system. Three layers of wiring are fabricated by repeating this flow three times.

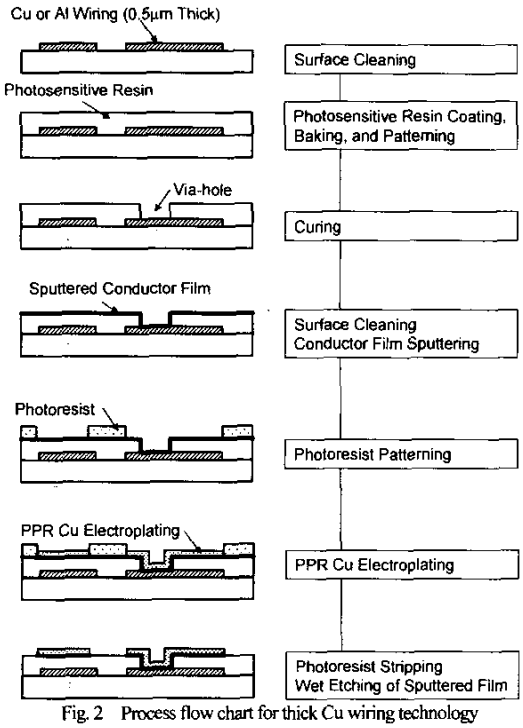


Fig. 2 Process flow chart for thick Cu wiring technology

B. PPR Cu electroplating

When the thick Cu wiring is electroplated only at the designated area, opening pattern regulated by photoresist and its density affect the uniformity of Cu thickness. Moreover, an electric charge concentration generally occurs at the top edge of the via-holes, and this uneven electric field is not suitable for stable via-hole electroplating smaller than 20 μm in diameter. In the PPR Cu electroplating process, the input current waveform is controlled during plating, as shown in Fig. 3. Cu ions and additives move to the anode side during minus current step, and the electric charge concentration during plus current step is suppressed. The thickness uniformity is better than the conventional direct current (DC) Cu electroplating used in the packaging process. When the target thickness is 5 μm on an 8-inch wafer, the thickness variation by PPR Cu electroplating is less than 2 μm, compared to that of 5 μm or more by conventional DC Cu electroplating.

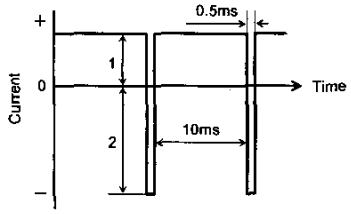


Fig. 3 Schematic diagram of PPR electroplating current

C. Interlayer dielectric material

Via-hole resolution, in other words, the aspect ratio is an important characteristic regarding the connectivity of the thick Cu wiring to the ULSI inner wiring. Several kinds of resin have been evaluated, in terms of internal stress, endurance for plasma treatment, and organic solution resistance. Finally, a negative-type epoxy resin is selected. Table 1 shows the epoxy resin characteristics.

Table 1 Typical properties of the epoxy resin

Dielectric constant (1MHz)	3.2
Dissipation factor (1MHz)	0.002
Insulation breakdown	230 kV/mm
Insulation resistance	> 10^{15} Ωcm
Coefficient of thermal expansion	40 ppm/°C
Glass transition temperature (at TMA)	230 °C
Curing temperature	160 °C
Elongation	7 %
Water absorption	0.7 wt%
Via-hole resolution (aspect ratio)	1.2 - 1.4

This epoxy resin has the advantages of low dielectric constant of 3.2, low dissipation factor of 0.002, and high Glass transition temperature of 230 °C. In particular, a remarkable property is excellent via-hole resolution, so that 10-μm diameter via-holes are fabricated for the connection to the ULSI inner wiring. Since the curing temperature of epoxy resin is as low as 160 °C, ULSIs are not thermally influenced.

High temperature and humidity bias tests (HHBTs) are performed to estimate the insulation reliability of the resin, using line-and-space patterns. The test patterns are 20-μm-pitch Cu wiring with 5-μm thickness covered with 8-μm-thick resin. The applied voltage, temperature, and relative humidity are 10 V, 85 °C, and 85 %, respectively. Figure 4 shows the insulation resistance for ten samples as a function of time. The resistance of the insulation remains excellent value, approximately $1x10^{13}$ Ω, over a period of 1000 hours. There is little variation in resistance among the samples. From this result, this resin prevents Cu migration under an ULSI operating condition.

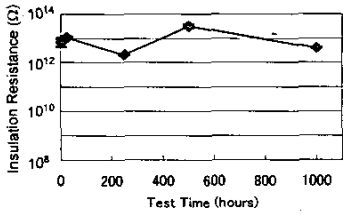


Fig. 4 HHBT results (line pitch = 20 μm)

III. Thick Cu wiring ULSI and electrical properties

A. Test structures

Four types of test structure were prepared for the IR-drop evaluation. The basic structure, named as M3 shown in Fig. 5(a), consists of 0.13-μm CMOS transistors and conventional three layers of 0.5-μm-thick Al wiring. On this M3 structure, additional wiring of two layers of 0.5-μm-thick Al, one layer of 5-μm-thick Cu, and three layers of 5-μm-thick Cu were

fabricated for M5, TEG-1, and TEG-2, respectively. Table 2 shows the design rule for thick Cu wiring.

Chip and IR-drop evaluation circuit photographs for TEG-2 are shown in Fig. 6(a). Cross-sectional SEM images of Cu and Al wirings are shown in Fig. 6(b). The thick Cu wiring dimensions are larger than that of Al wiring. The epoxy resin surface is approximately flat without polishing, because it has excellent surface planarization characteristics.

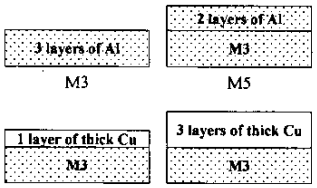
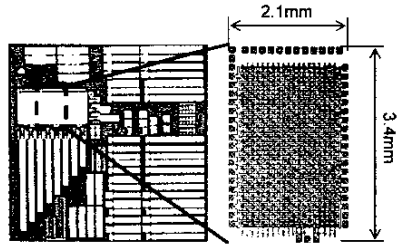


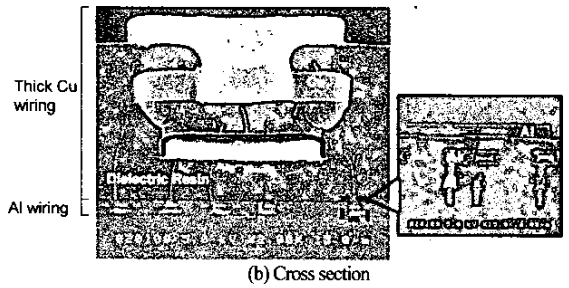
Fig. 5 Test structures

Table 2 TEG-2 specification

Design rule for thick Cu wiring	
Line width / space (minimum)	10μm / 10μm
Via-holes diameter (minimum)	10μm
Line thickness	5μm
Dielectric layer thickness	8μm
Number of thick Cu layers	3
Chip size	17.96mm□
Dielectric resin	Photosensitive epoxy
Basic ULSI (M3)	
Gate length	130nm
Al wiring thickness	0.5μm
Number of conductor layers	3



(a) Chip (17.96mm□) and evaluation circuit outline



(b) Cross section

Fig. 6 TEG-2 patterns

B. IR-drop evaluation

The resistance of power supply wirings, R, is evaluated by measuring the circuit current, I_{dd}, for each test structure, in order to investigate the IR-drop, as shown in Fig. 7. The resistance reduction, ΔR, is defined as follows:

$$\Delta R = R_X - R_{M3} \quad (X = \text{M5, TEG-1, TEG-2})$$

, where R_{M3}, R_{M5}, $R_{TEG\text{-}1}$, and $R_{TEG\text{-}2}$ denote the resistances of power supply wiring for M3, M5, TEG-1, and TEG-2, respectively.

The clock frequency, f_{clock}, and power supply voltage, V_{dd}, are 1 GHz and 1.5 V, respectively, and a switching capacitance, C_{switch}, is estimated to be 1 nF. The ΔR values are relatively plotted in Fig. 8, with regarding M5 as standard. The proposed Cu wirings of TEG-2 successfully demonstrate the reduction of power supply resistance five times as large as that of the conventional two layers of Al wirings of M5. Even the TEG-1 with one thick Cu wiring layer shows the resistance reduction two times as large as that of M5.

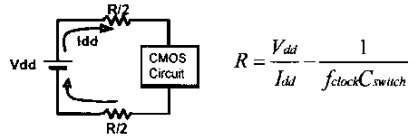


Fig. 7 IR-drop evaluation

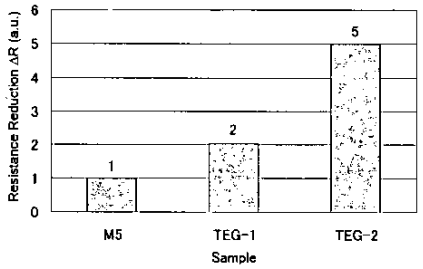


Fig. 8 IR-drop evaluation results (f_{clock}=1GHz, V_{dd}=1.5V)

IV. Conclusion

A multilevel 5-μm-thick Cu wiring technology was successfully developed and the improvement in the resistance of ULSIs power supply wirings was demonstrated. The PPR Cu electroplating and photosensitive resin made a simple process flow and low cost fabrication possible.

This technology is believed to provide not only advanced ULSIs with stable power supply wirings and higher speed operation, but also connectivity between ULSIs and packaging substrates and possible wiring in System-in-Package.

Acknowledgements

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