44th meeting of IFIP Working Group 10.4
on Dependable Computing and Fault Tolerance,
Workshop on "Hardware Design and Dependability"

June 28, 2003

Challenges to Dependable VLSIs

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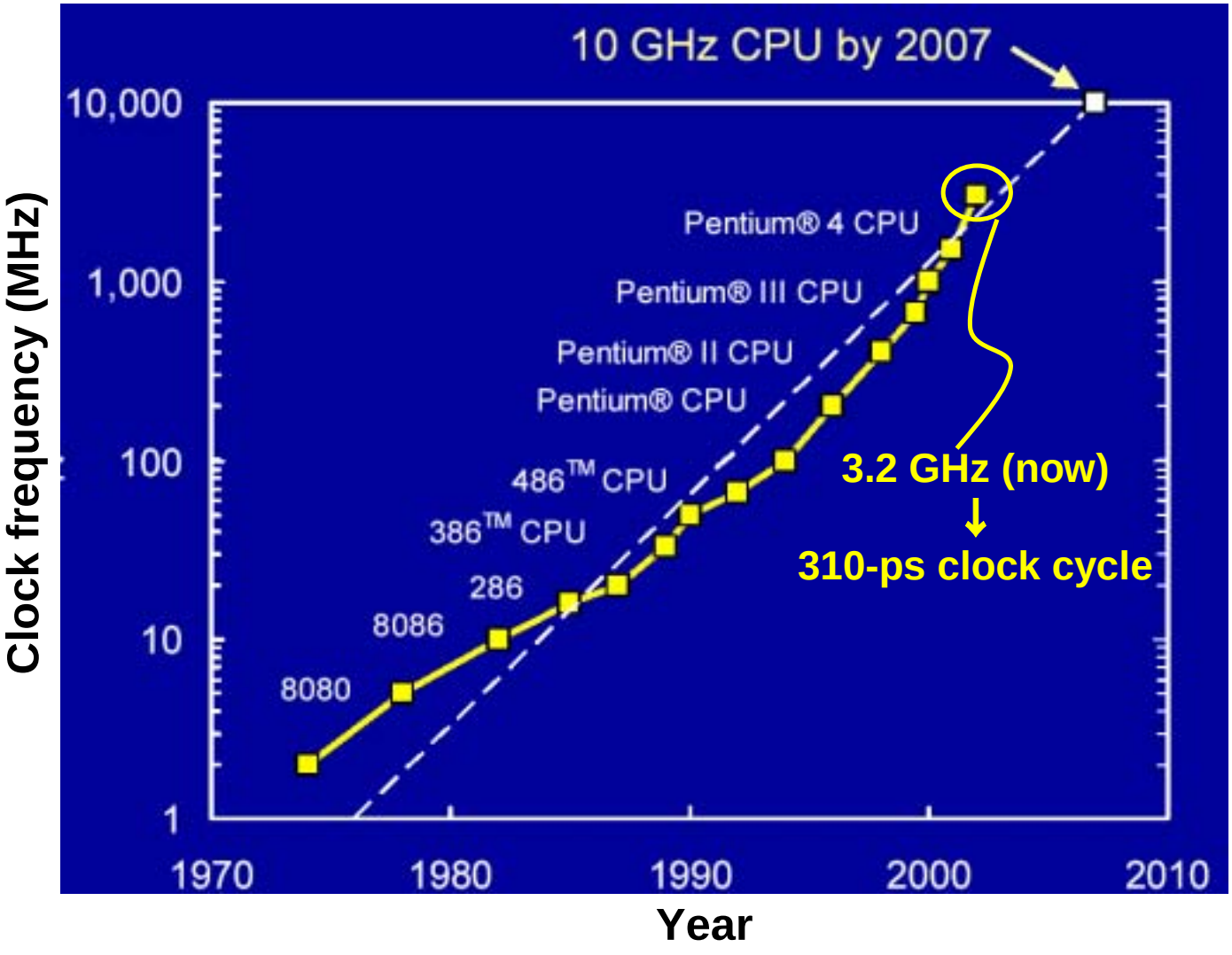
Outline

- Technology trend of VLSIs
- Dependability issues
  - Power / signal integrity problems at design-phase
  - Device variation problems at manufacturing-phase
  - Degradation problems after shipping
- Future Dependable VLSIs
  - Autonomous Reconfigurable Cell Array (ARCA)
- Summary

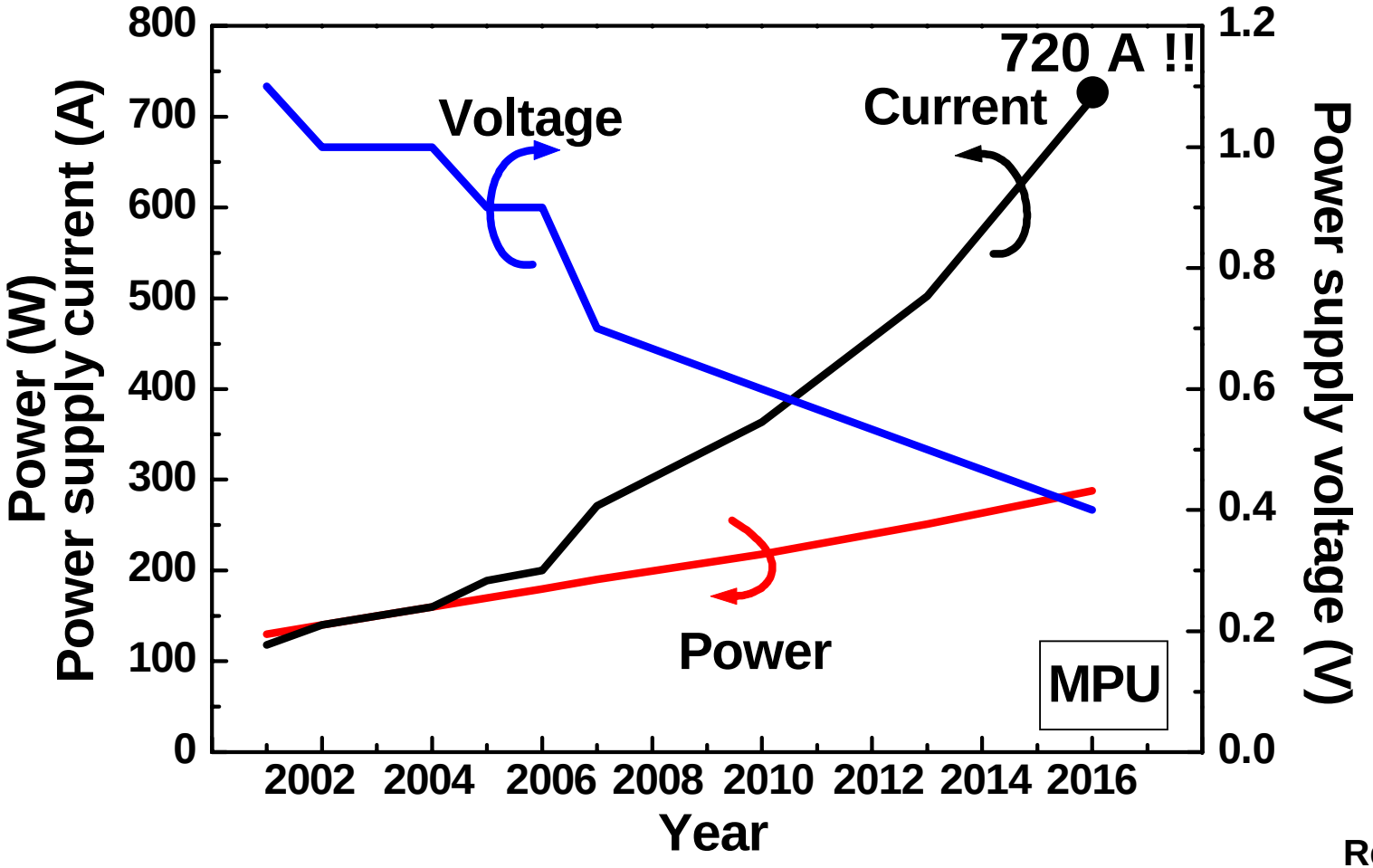
MPU Clock Frequency Trend



Ref [1]

- **Pico-second timing-design is required.**

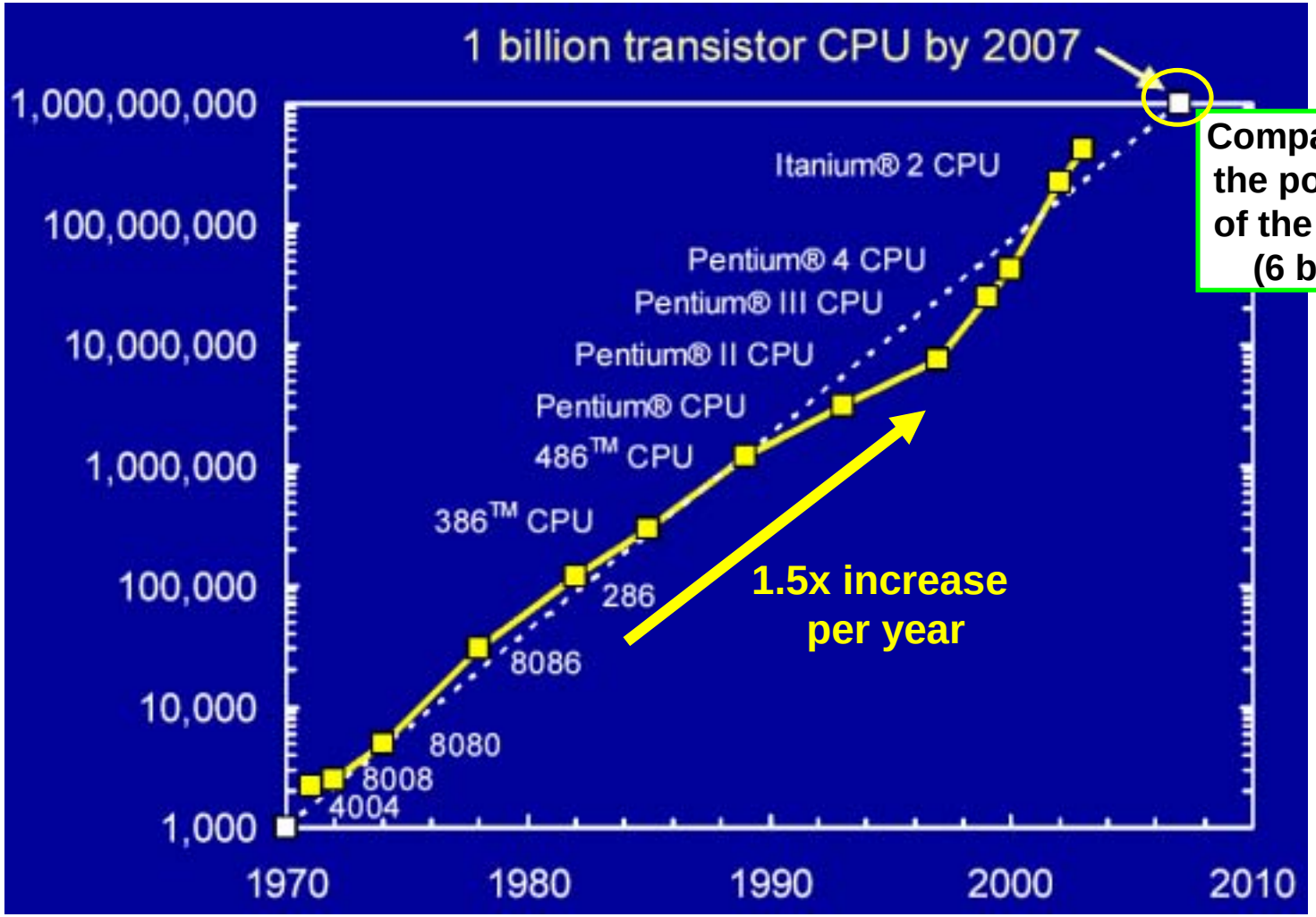
MPU Power-Supply Trend



Ref [2]

- Power-supply-current increases rapidly, even though the supply-voltage decreases.
- Large current causes power-integrity and electro-migration problems.

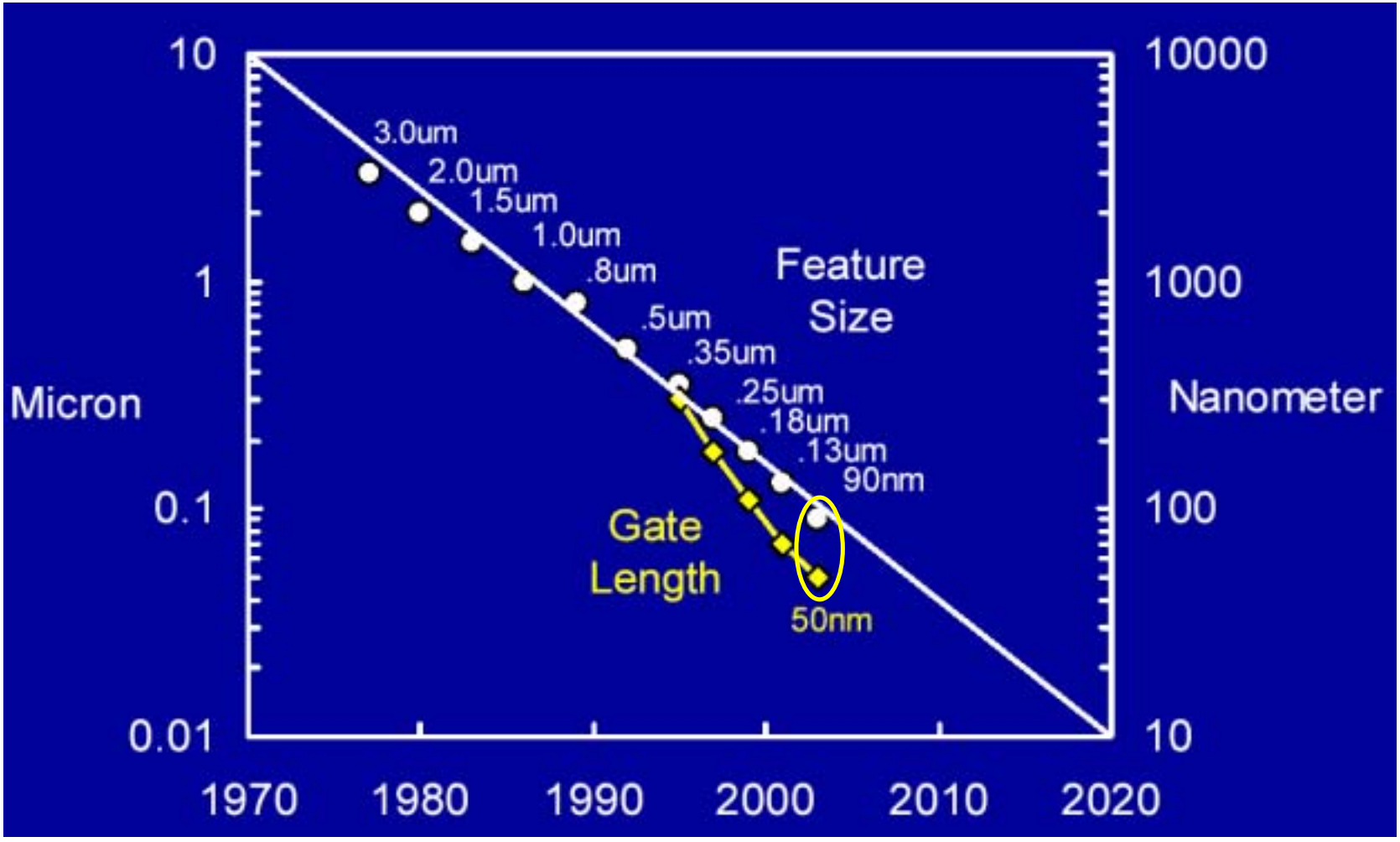
MPU Transistor Count Trend



Ref [1]

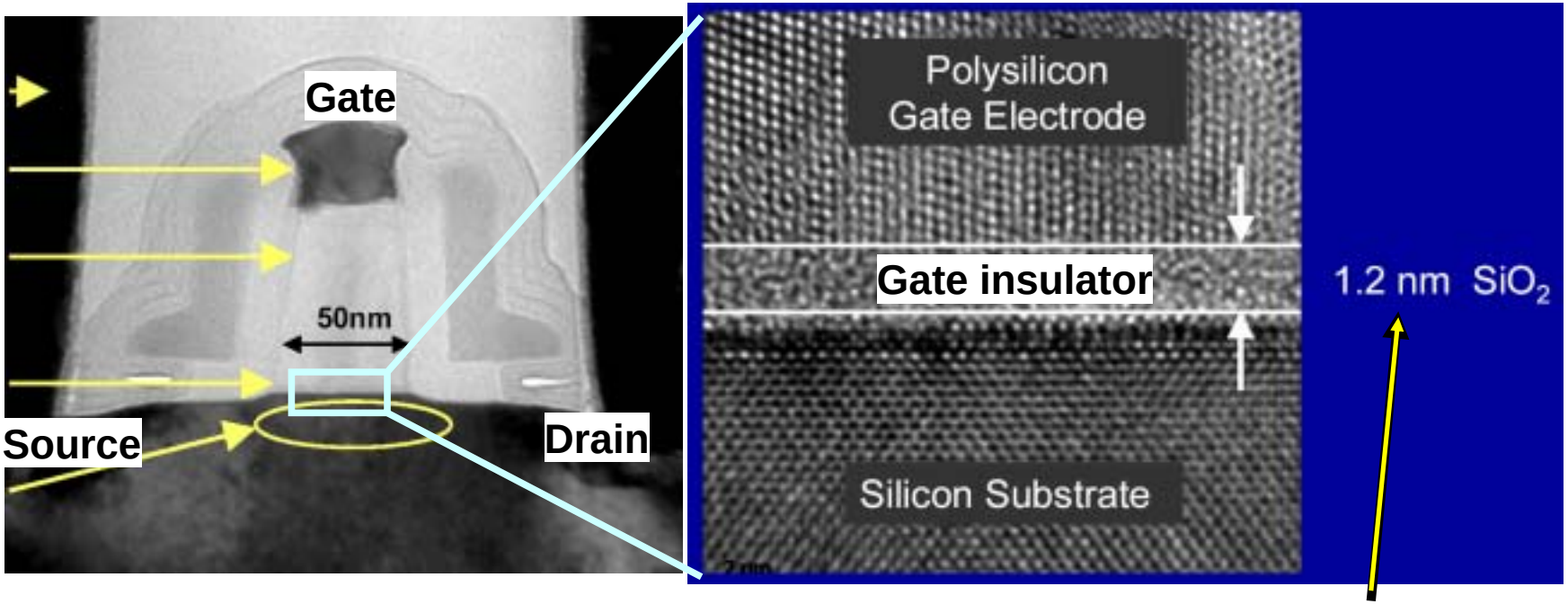
- A lot of functions are integrated on a chip.
- Design complexity increases.
- 7σ-control of device variations is required for 1 billion transistors.

MPU Feature Size Trend



- **Transistor size is aggressively scaled into nanometer region.**

MOS Transistor



Comparable to the lattice constant of silicon (0.54 nm)

Ref [1]

- **50-nm gate length transistor with the atomic-level gate insulator**

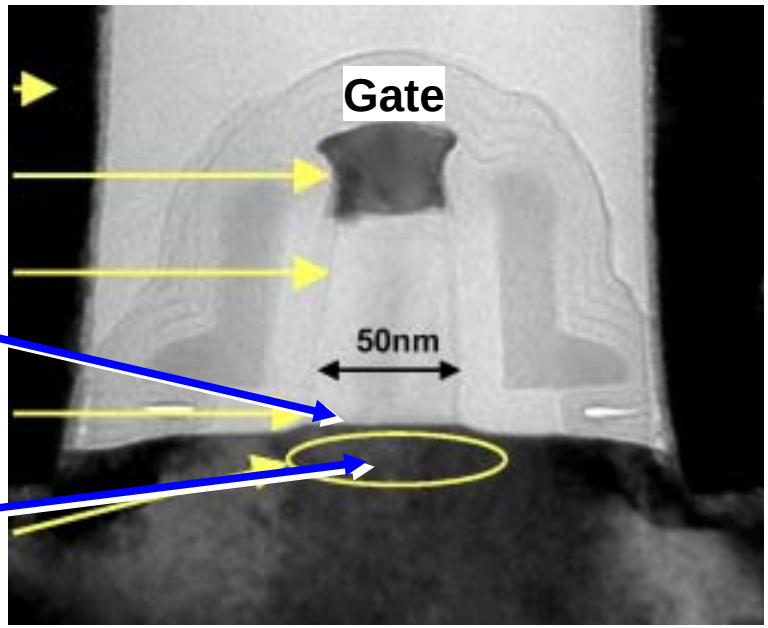
Introduction of New Materials

From Al to Cu Interconnect for low resistance

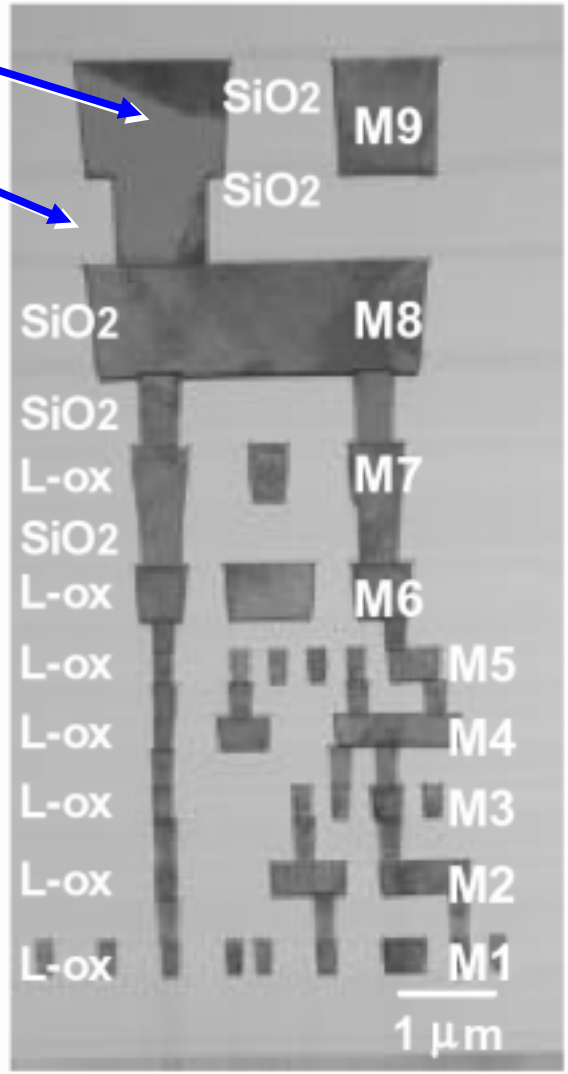
From SiO_2 to low-k dielectric for low capacitance

From SiO_2 to high-k gate dielectric for low leakage

From Si to SiGe channel for large current

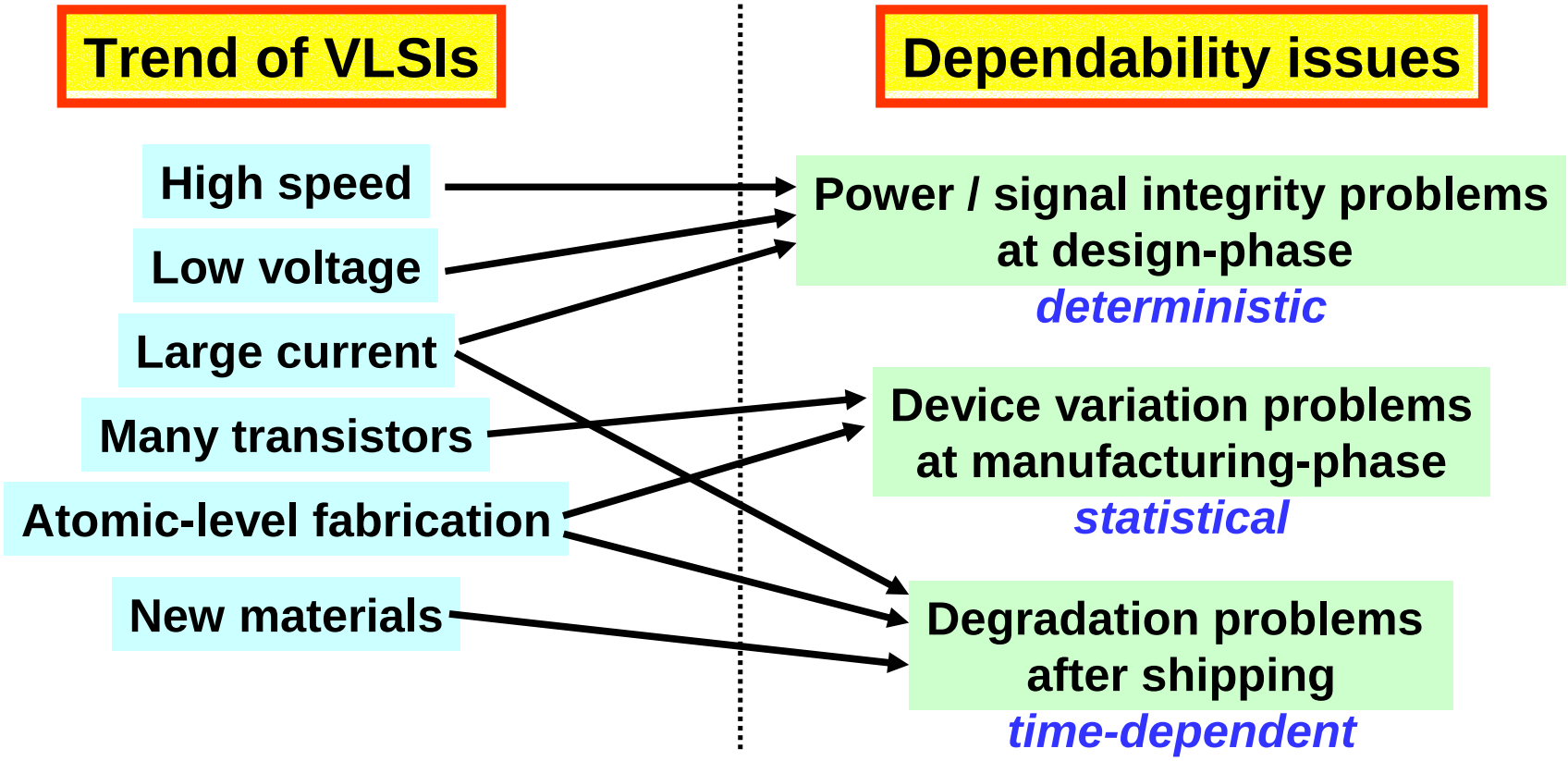


Ref [1,3]



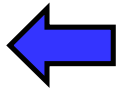
- New materials are introduced to break through the scaling limit.
- New materials cause novel reliability problems.

What Threatens the Dependability of VLSI?



- The dependability of VLSI is threatened by a lot of problems at 3-phases.
- All these problems are difficult to predict accurately.
- The prompt solutions to these problems are essential to keep the continuous evolution of VLSIs.

Outline

- Technology trend of VLSIs
- Dependability issues
  - Power / signal integrity problems at design-phase 
  - Device variation problems at manufacturing-phase
  - Degradation problems after shipping
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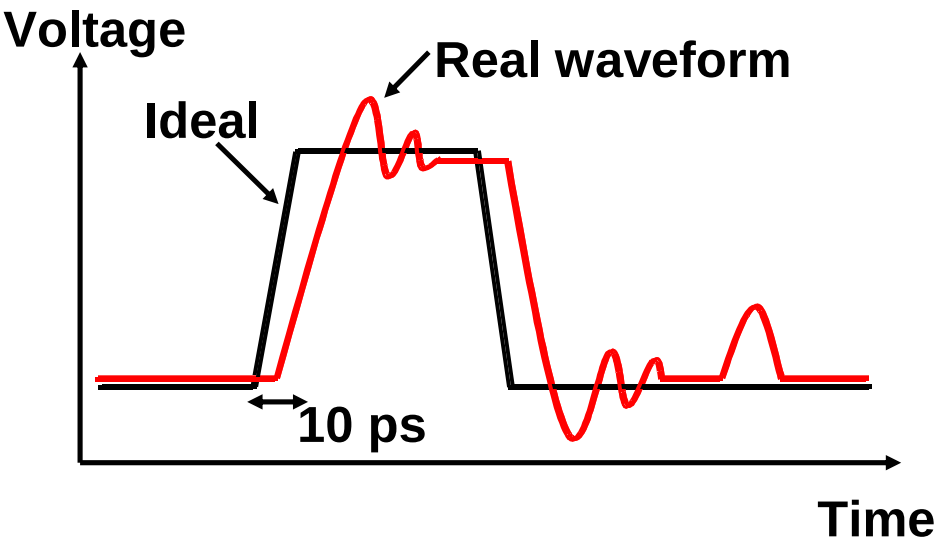
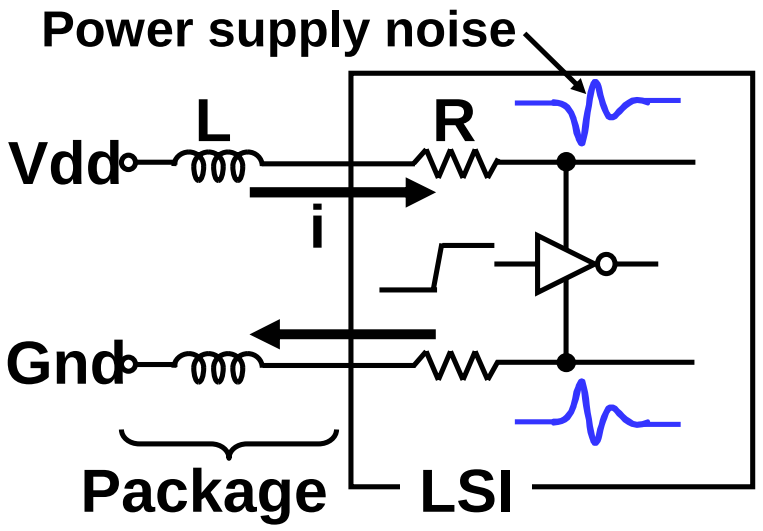
Power / Signal Integrity Problems at Design-Phase

Signal Integrity Problems

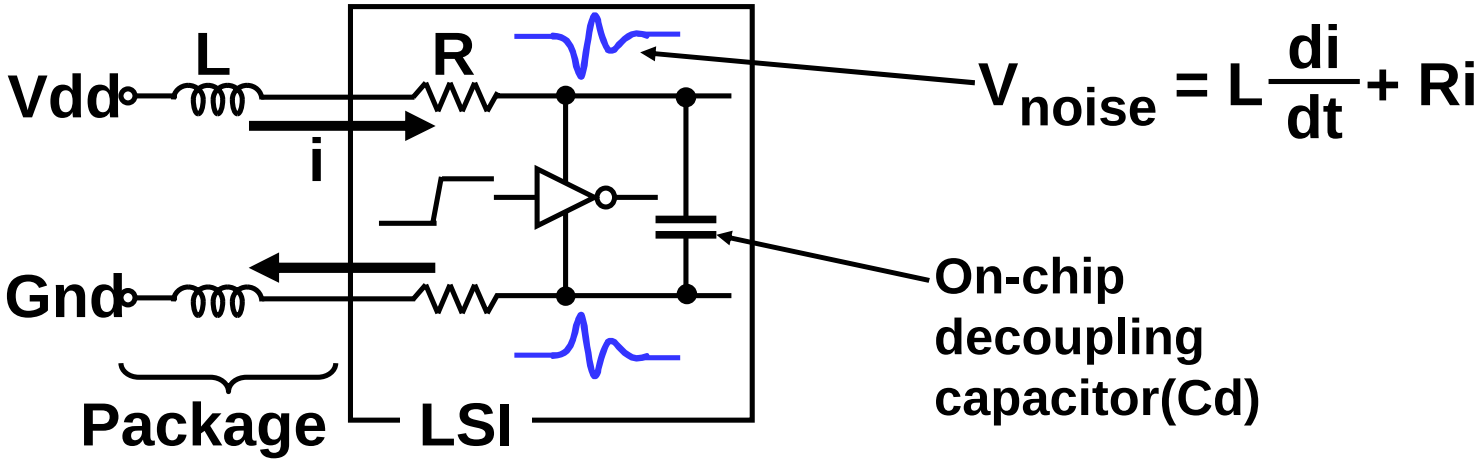


Power Integrity Problems



- These problems could be ignored in the past, however, they increase the influence on the circuits performance with the high-speed, low-voltage, and large-current trend.
- Now, they are the main cause of the failure of LSI design.

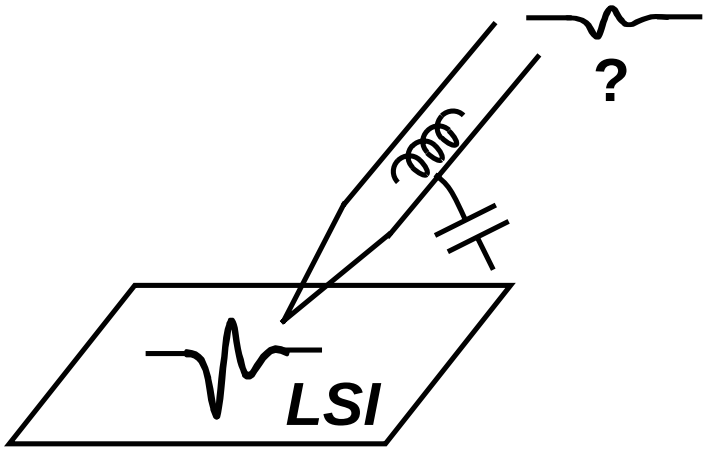
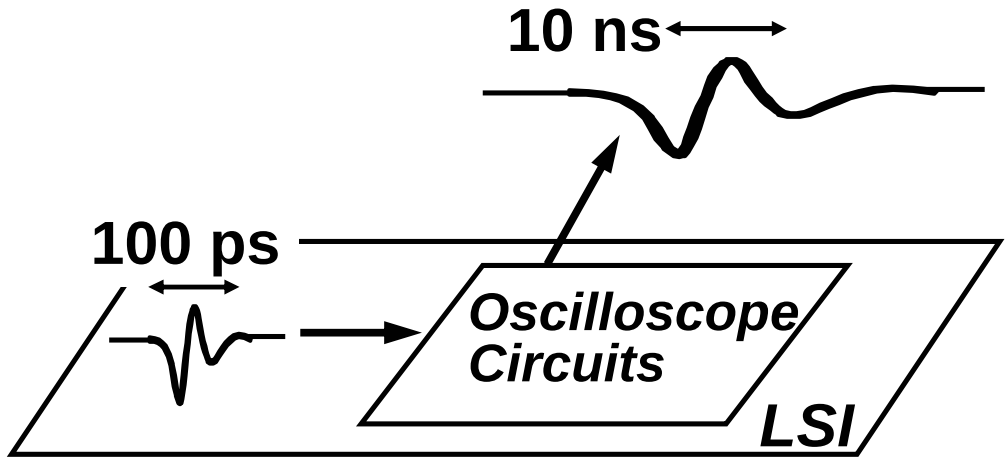
Power Integrity Problems



- Modeling of the power-supply-noise is difficult, because;
  (1) The power-supply-network is large-scale.
  Ex.) 5000 pads for Vdd/Gnd,
  Total length of Vdd/Gnd wires on 20 mm-square-chip is 1.1 km!!
  (2) The supply-current changes with the operation of LSI.
- Typical measures against the noise is Cd, however, Cd occupies 20 % of a chip. → Increased chip area
- Verification of the model is also difficult, because the measurement of the on-chip noise waveform is hard.

→ On-chip oscilloscope circuits is developed.

Off-Chip vs. On-chip Measurement Techniques

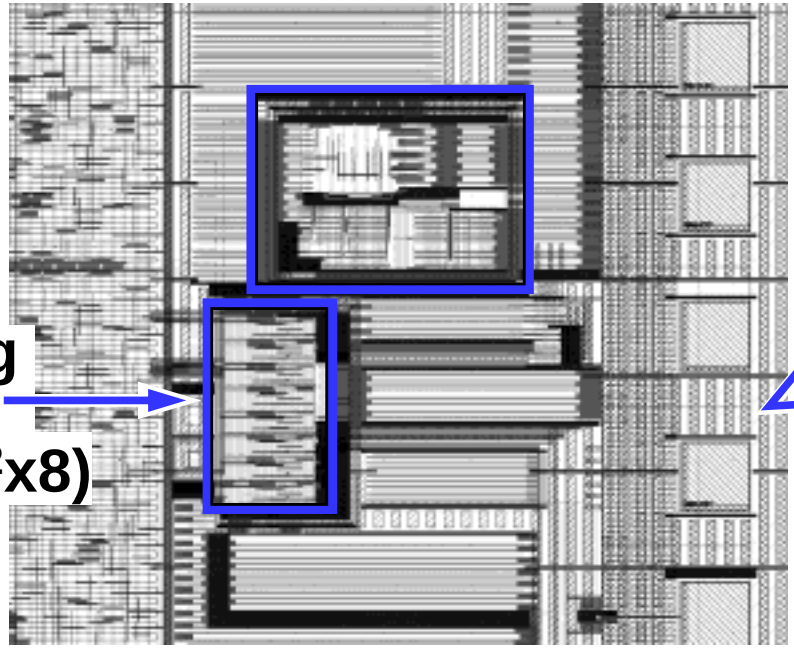
Off-chip Measurement	On-chip Measurement
	
Large Parasitic L, C ⬇ **Low Bandwidth**	**Time scale of outputs is expanded by sampling** ⬇ **High Bandwidth**

- **On-chip very fast waveforms can be measured by the on-chip measurement using the oscilloscope circuits.**

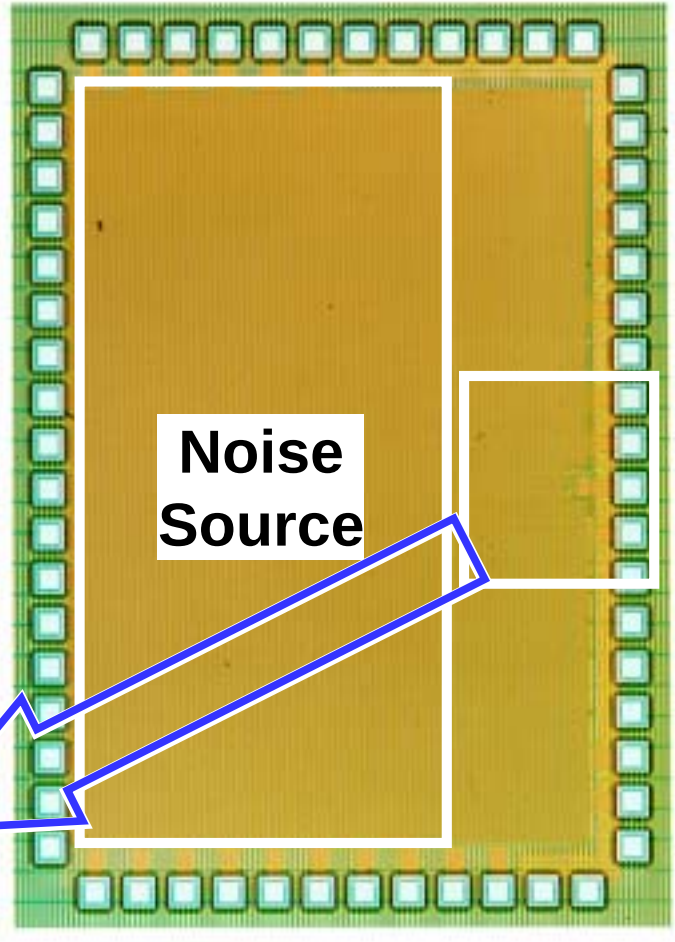
On-Chip Oscilloscope Circuits

1.2V, 0.13μm CMOS

Oscilloscope circuits

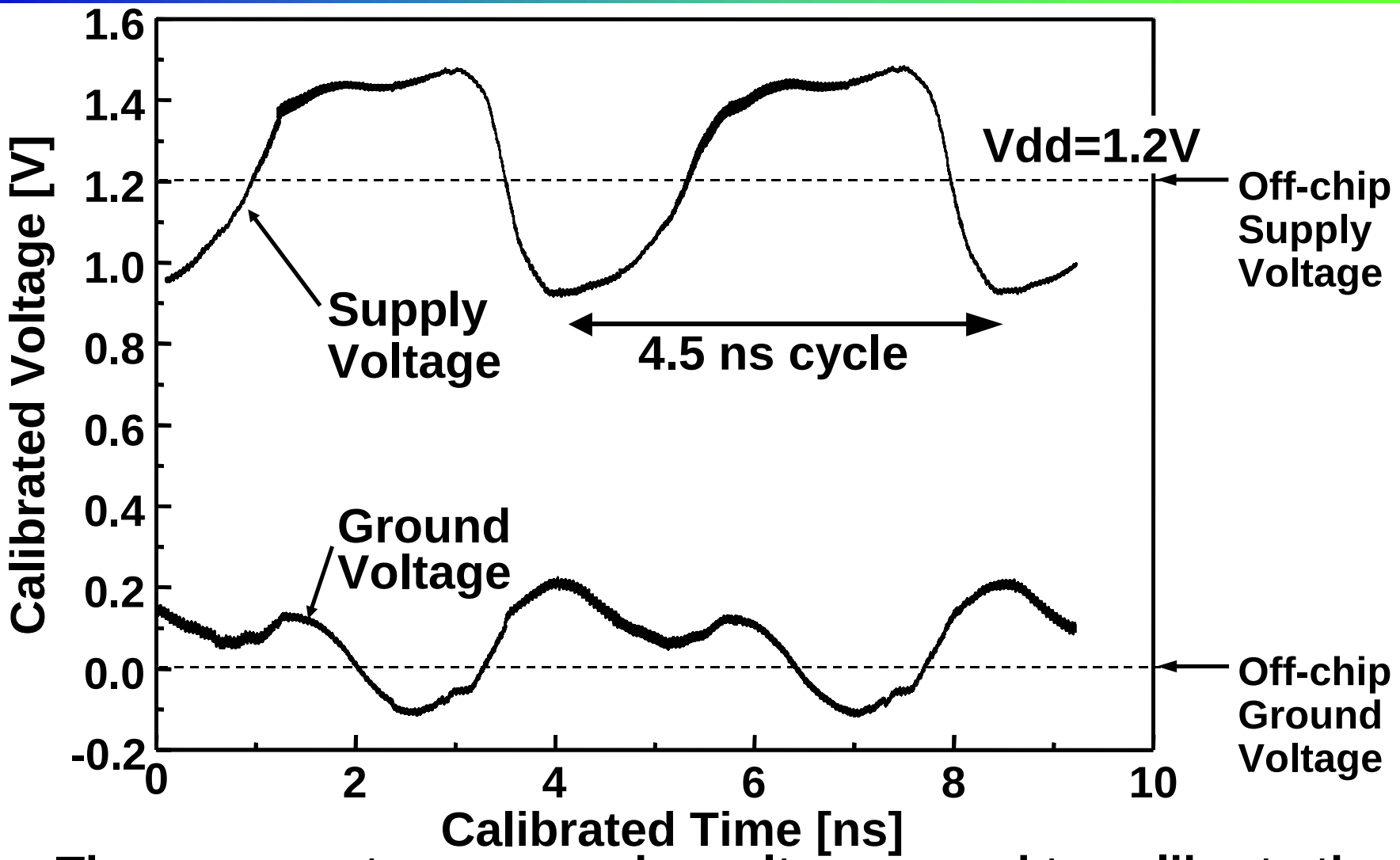


Sampling heads (1550μm²x8)



Ref [4]

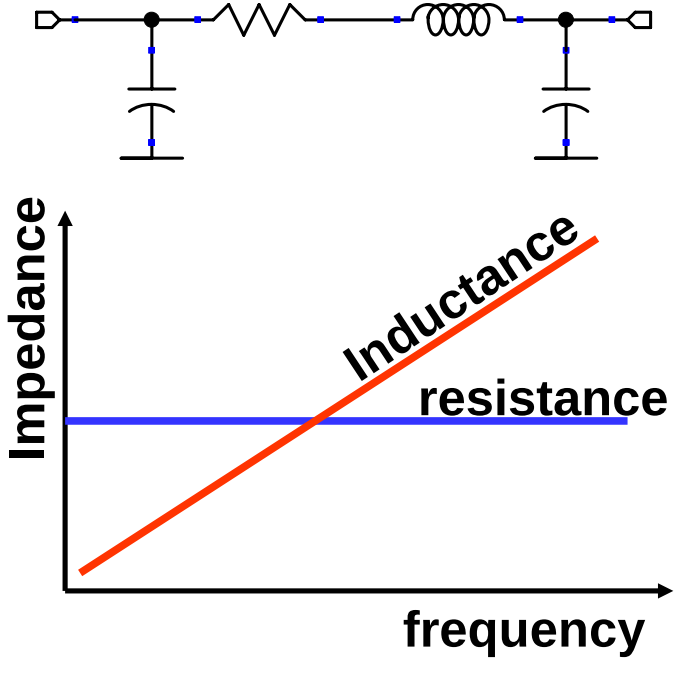
Measured Power-Supply-Noise by Oscilloscope Circuits

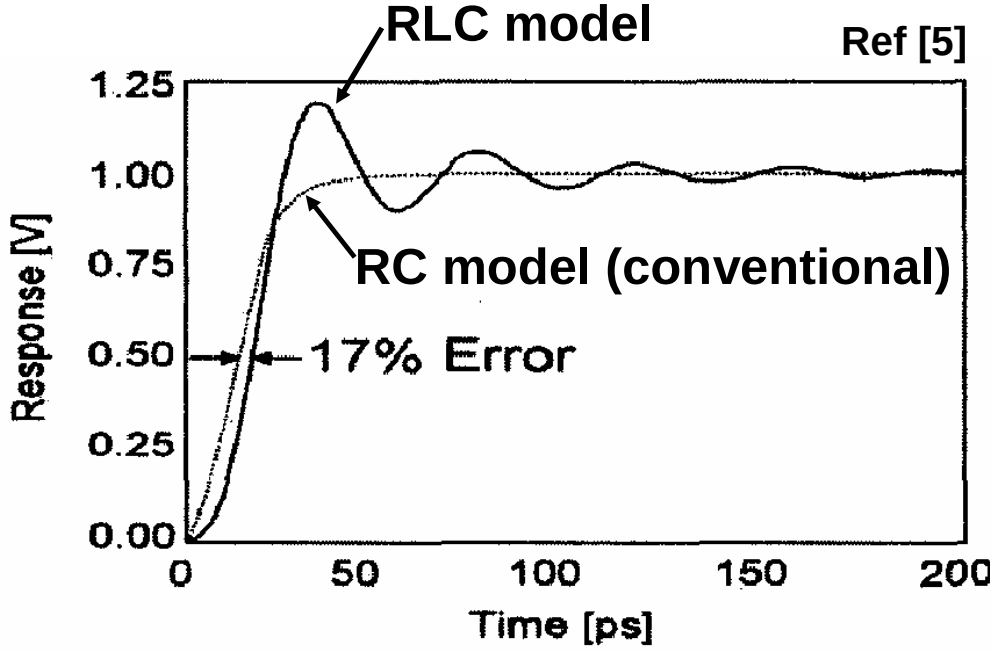


- These accurate measured results are used to calibrate the power-supply-noise model.

Signal Integrity Problems

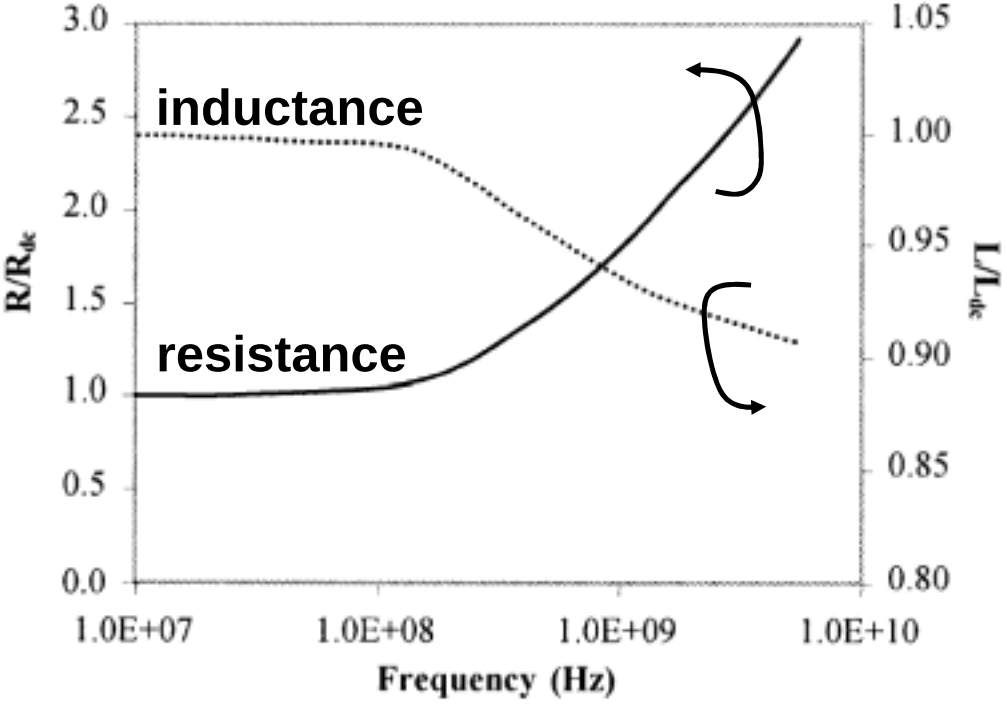
- Signal integrity problems contain;
  - Crosstalk between the interconnects (←not discussed here)
  - Inductive component of the interconnects
- Inductive effect is especially-pronounced in the low-resistance interconnects for global clock distribution.
- Delay error due the inductive effect results in clock skew.

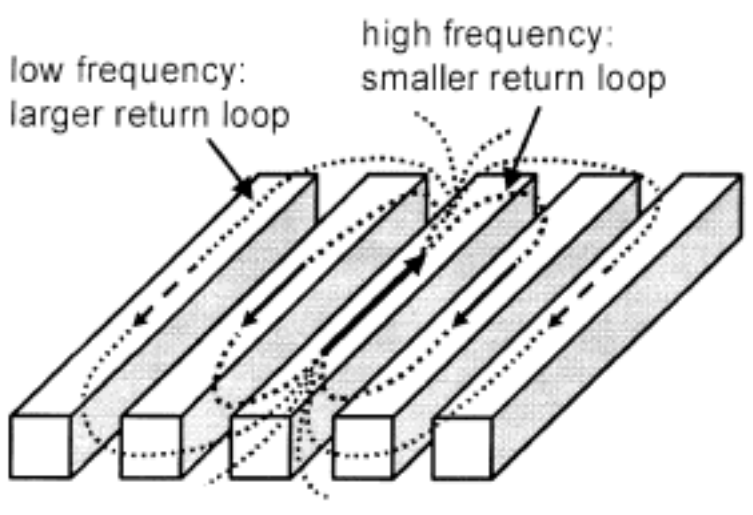




Modeling of On-Chip Inductance

- **Inductance is determined by the current-loop.**
- **Modeling of the on-chip inductance is difficult, because;**
  (1) A on-chip signal line has no ground plane, and it has many current-return-loops.
  (2) Inductance and resistance depend on the frequency because of the skin effect and the proximity effect.





Proximity effect

Ref [6,7]

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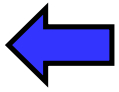
  - Device variation problems at manufacturing-phase 
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Device Variation Problems at Manufacturing-Phase

- **Atomic-level control of the fabrication of billons of transistors is a challenging task.**

- **The relative variation of the gate length (Lg) increases with technology scaling due to the fabrication difficulty.**

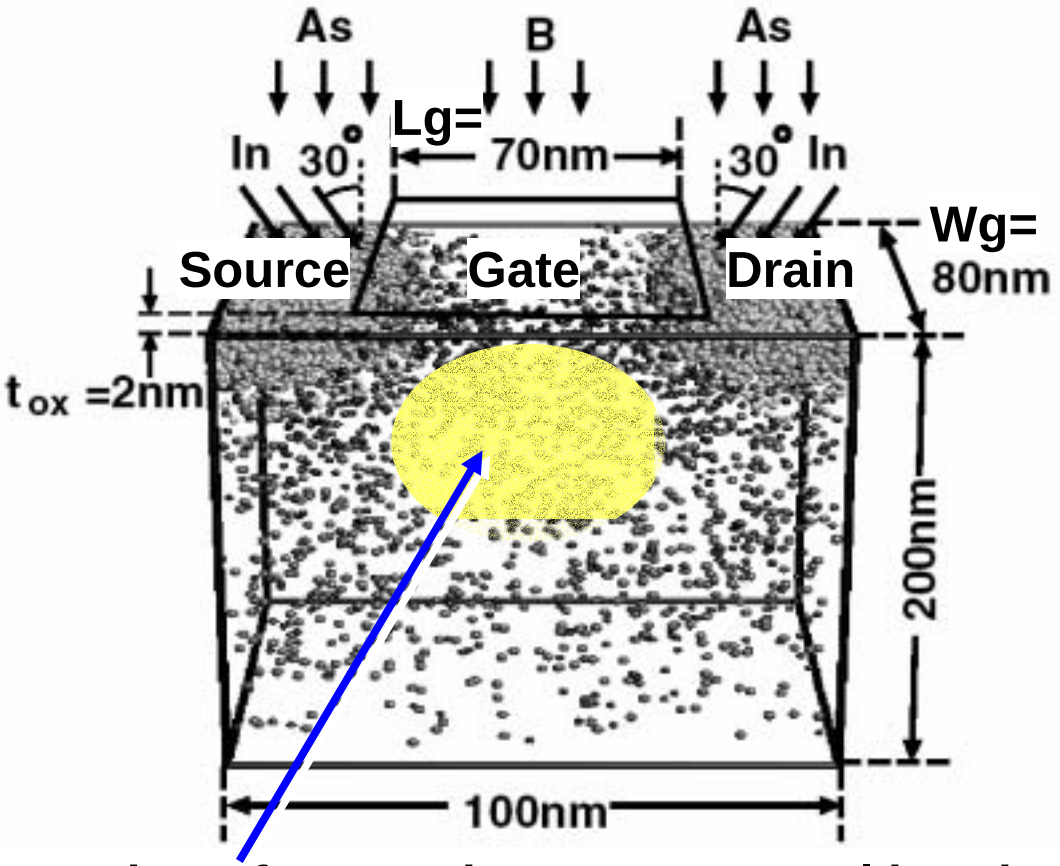
  Ex.) Lg = 350 nm±10% (past) → Lg = 50 nm±20% (now)

→Large variations of the device characteristics

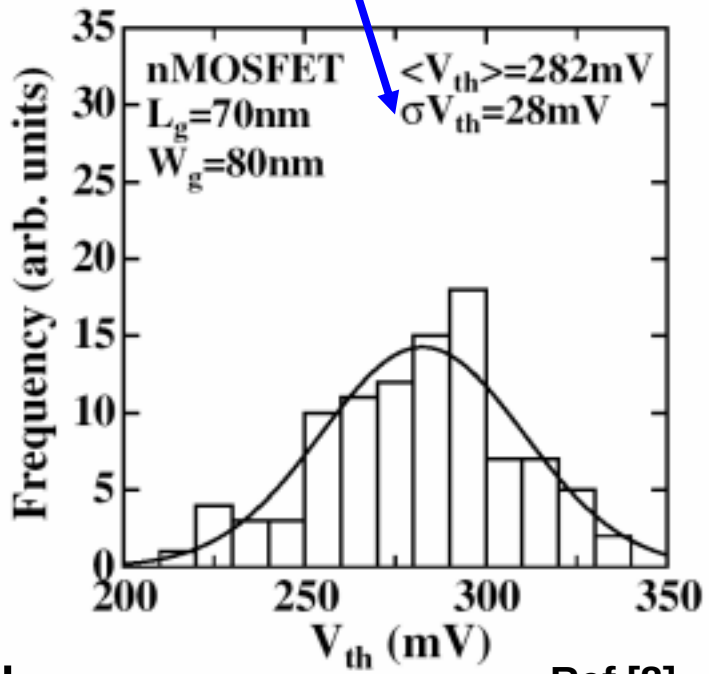
- **Intrinsic fluctuation in device characteristics due to discrete dopant atoms is an essential problem.**

V_{th} Fluctuation due to Discrete Dopant Atoms

Atomic 3-D process/device simulation



$$\sigma V_{th} \propto \frac{t_{ox}}{\sqrt{L_g W_g}}$$

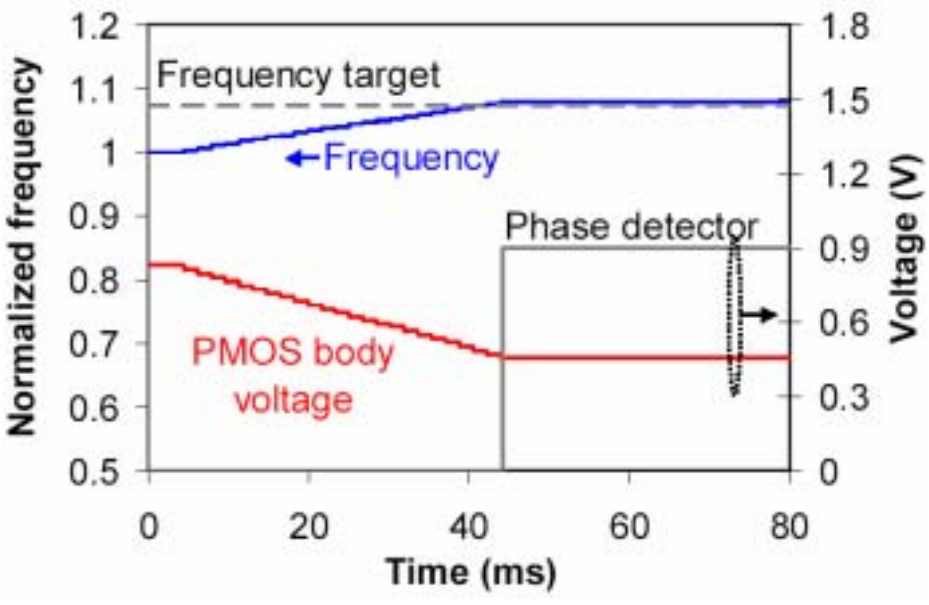


Number of Boron dopants = several hundreds

Ref [8]

- Threshold voltage (V_{th}) fluctuation induced by the statistical nature of the number and position of discrete dopant atoms.
- The only solution is the non-doped SOI devices.

Circuit Techniques to Compensate for Device Variations



	Frequency variation (σ)
w/o V_{sub} control	4.1 %
Same V_{sub} for a chip	0.69 %
Each V_{sub} for each region (chip is divided into 21 regions)	0.21 %

Ref [9]

- The substrate bias (V_{sub}) is controlled adaptively by using the replica of the critical path to meet the frequency target.
- Intra-chip variations, as well as inter-chip variations, are corrected, and the frequency variations are reduced.

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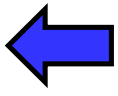
  - Degradation problems after shipping 
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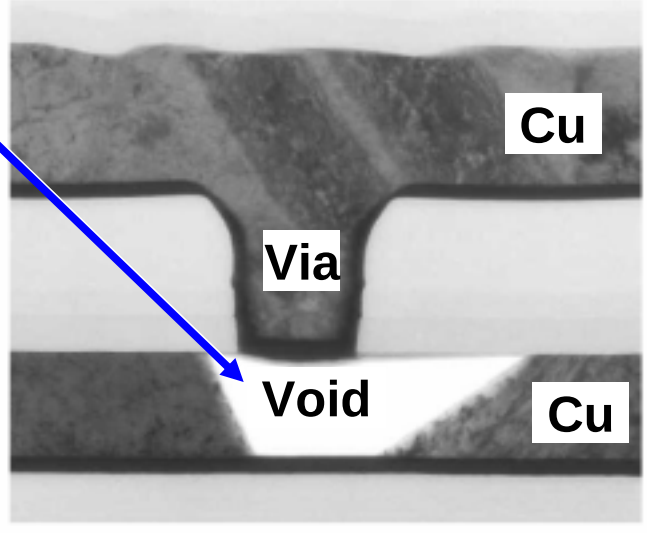
Degradation Problems after Shipping

- Introduction of new materials to VLSI causes novel reliability issues.
- Reliability of the high-k gate dielectric is not clearly understood.
- Electromigration is mitigated by changing from Al to Cu interconnects. However, it will be a serious problem, because the current density increases rapidly.
- Stress-induced voiding is the most serious problem in Cu interconnects.



Ref [10]

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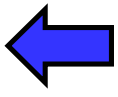
- Future Dependable VLSIs 
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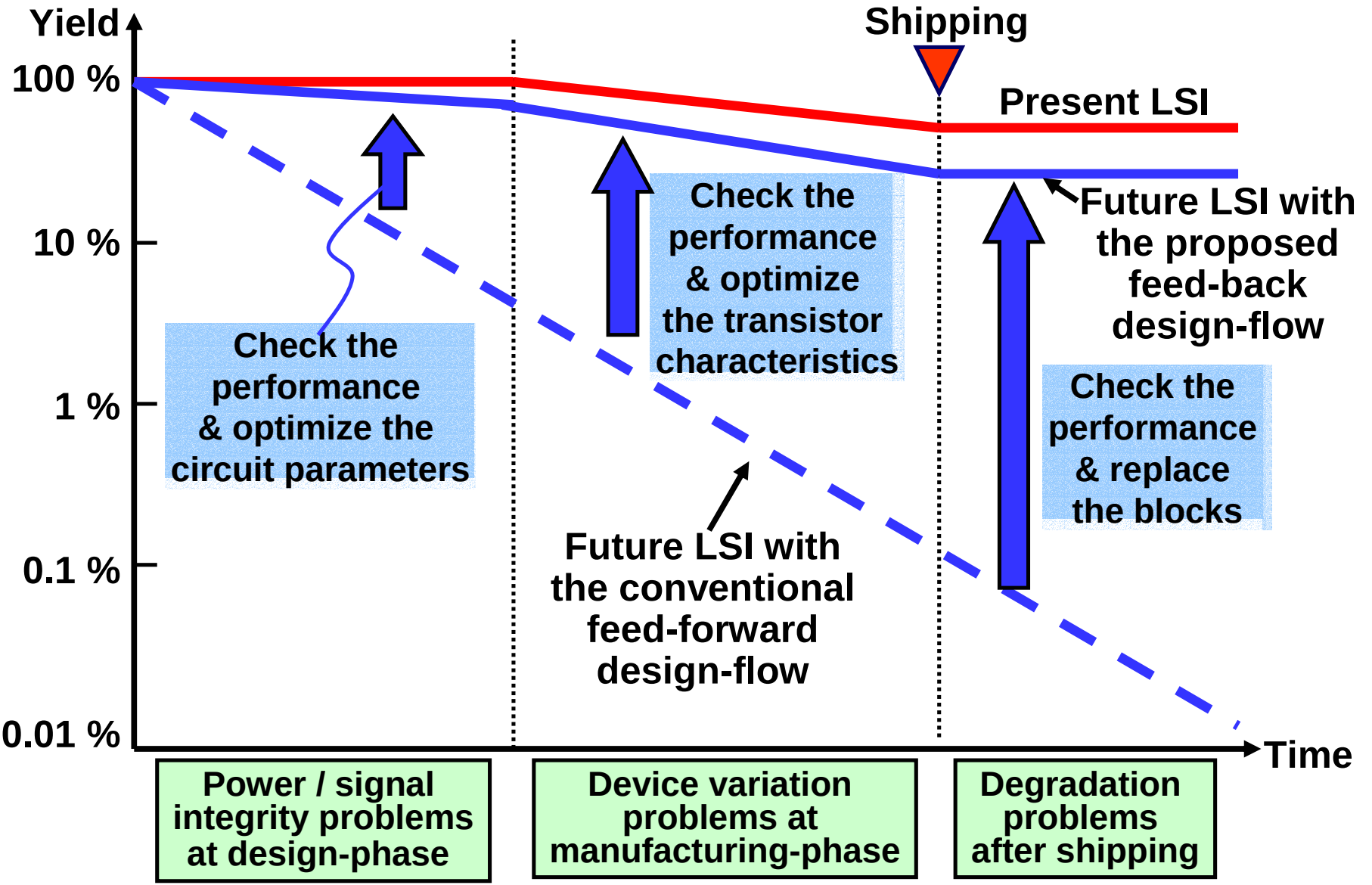
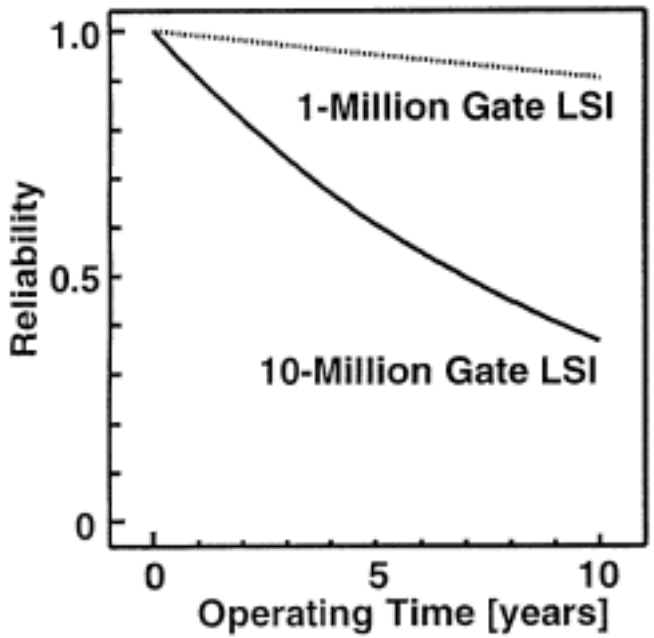
Future Dependable VLSIs with Feed-Back Design-Flow



Dependable VLSIs Design

Reliability Degradation in 10-Million Gate LSIs



Reliability $R = e^{-\lambda Ht}$

Error Rate $\lambda = 10^{-12}$/hour · gate

H : Number of Gates

t : Hours

- **Memory LSI has the simple function and the regular structure.**

→ **Redundancy and the error correcting code (ECC) are the mature technologies.**

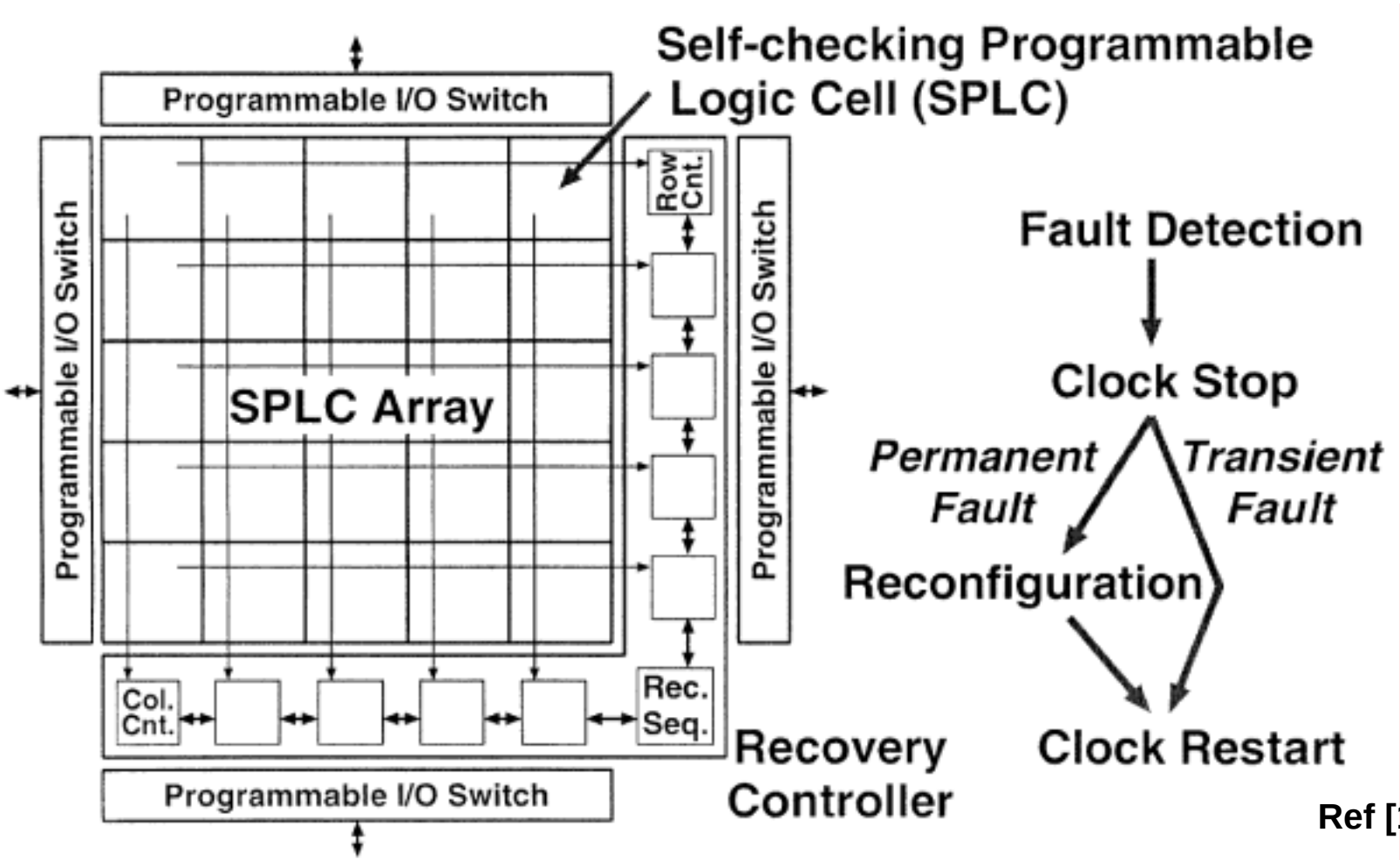
- **Logic LSI has the various functions and the complicated structure.**

→ **Random logic LSI with the redundancy is hard to realize.**

- **FPGA has the regular structure.**

→ **FPGA is suitable for the logic LSI with the redundancy.**

Autonomous Reconfigurable Cell Array (ARCA) for Dependable Logic VLSIs



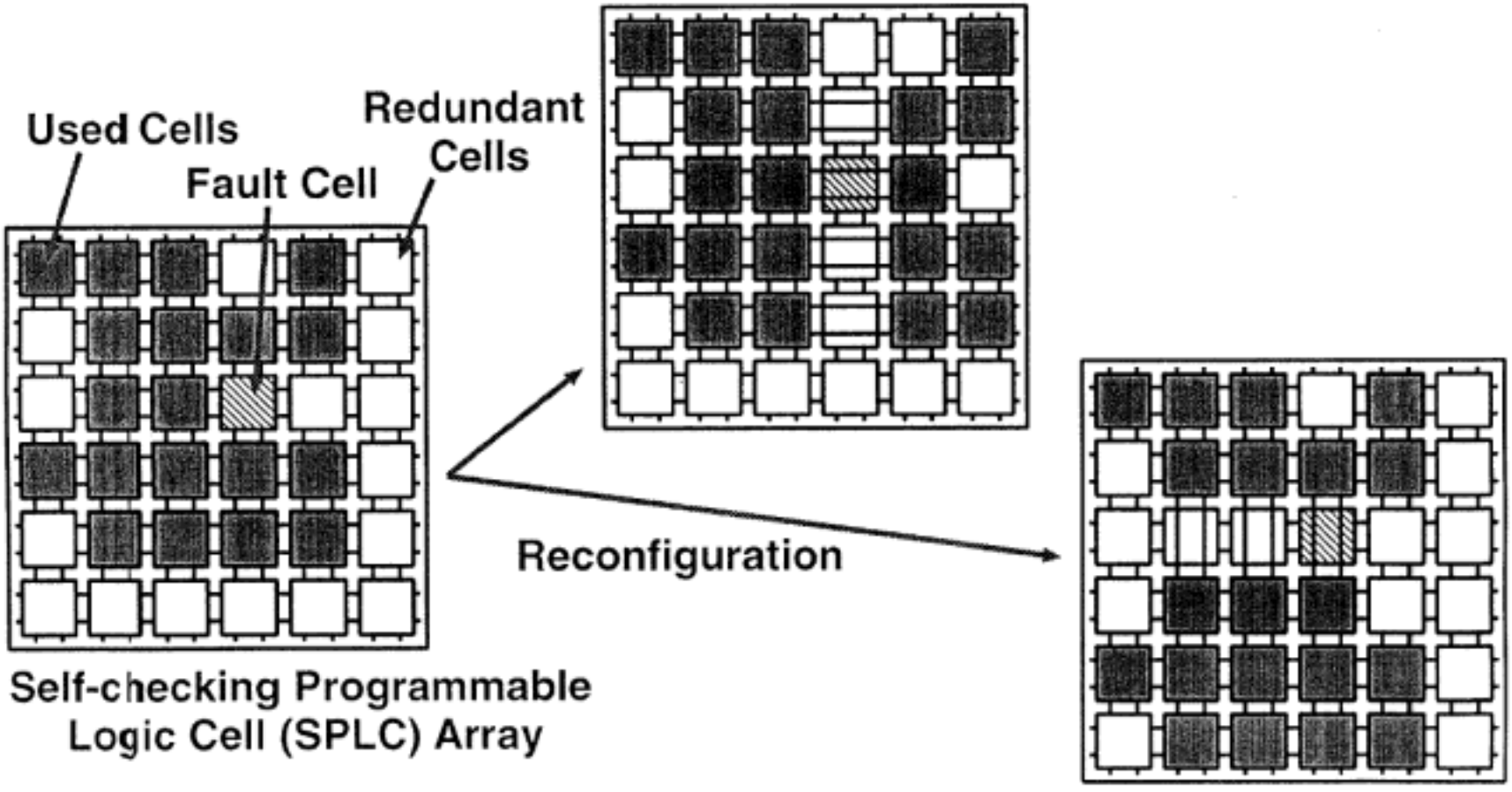
Ref [11]

- SPLC is composed of the two-rail logic.

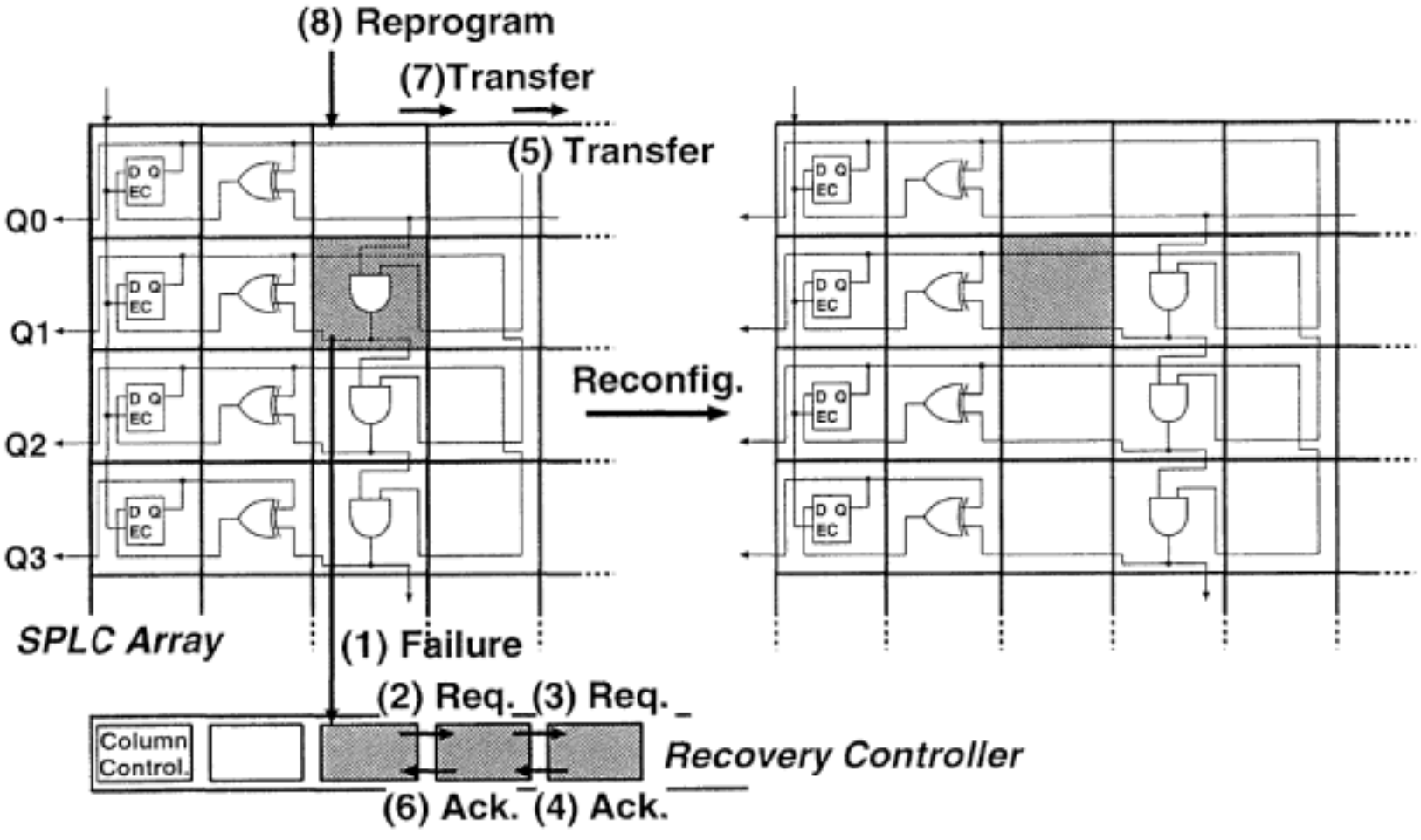
→ A fault is detected, when the signals of the two-rail logic are the same.

- Real-time online fault recovery is performed by the self-checking.

Autonomous Reconfiguration

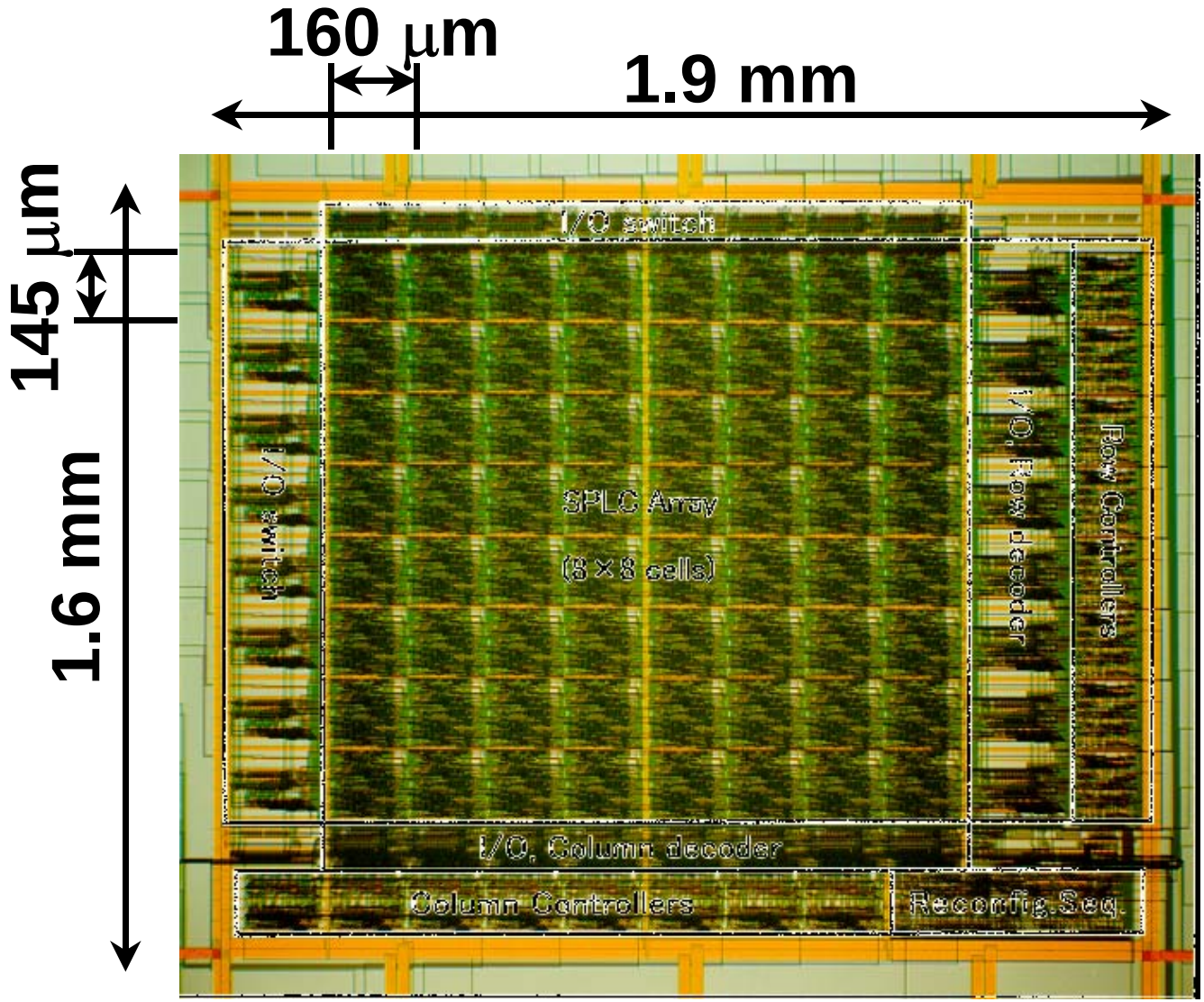


Reconfiguration Sequence



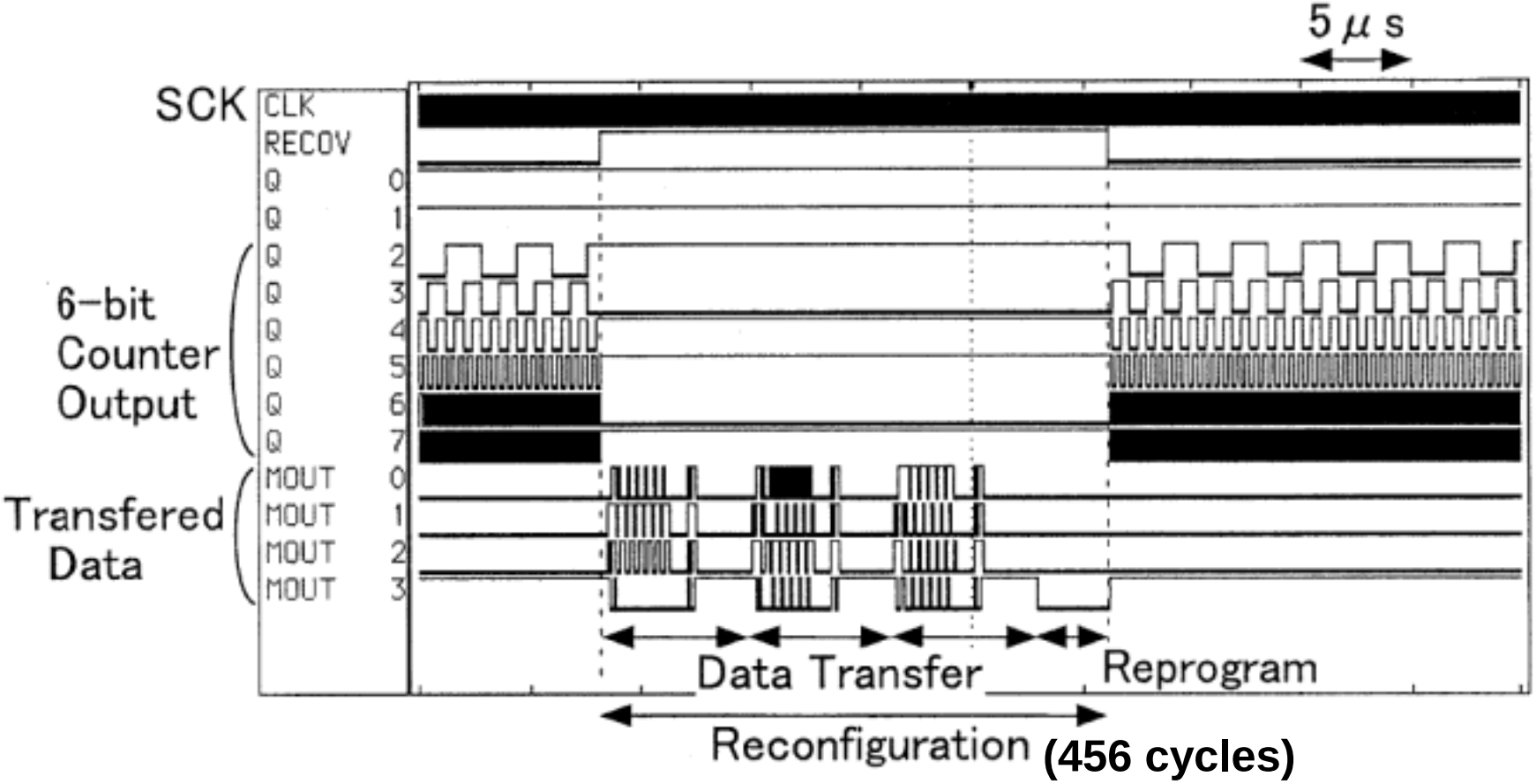
Reconfiguration of 4-bit Counter

Chip Micrograph of ARCA



8 x 8 ARCA LSI with 0.35-μm CMOS

Measured Reconfiguration



Reconfiguration for 6-bit Counter at 20 MHz Operation

Overhead of ARCA

- Time Overhead for Reconfiguration

  (8S+2)D+(4S+2) clock cycles

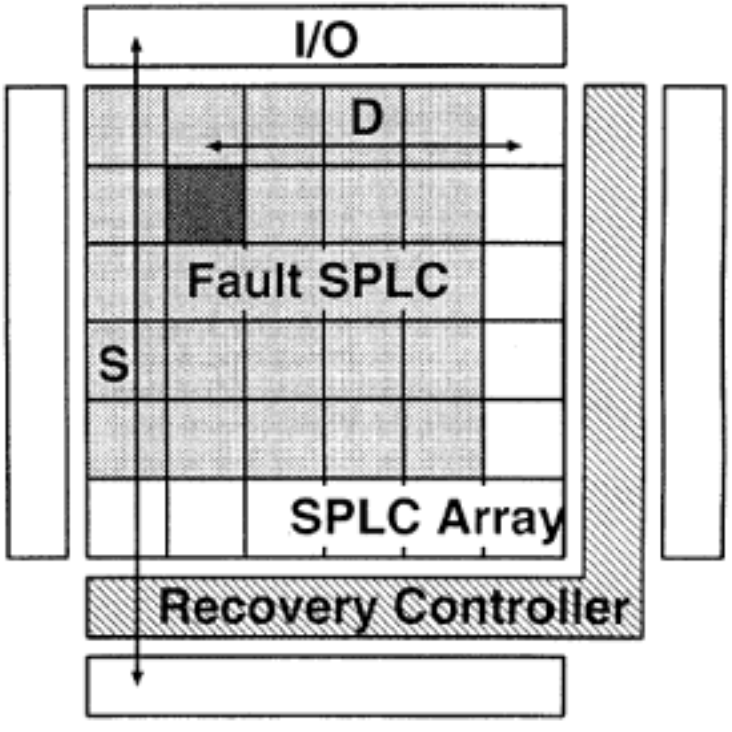
  S: SPLC array size *+2*

  D: Distance from fault line to redundant line

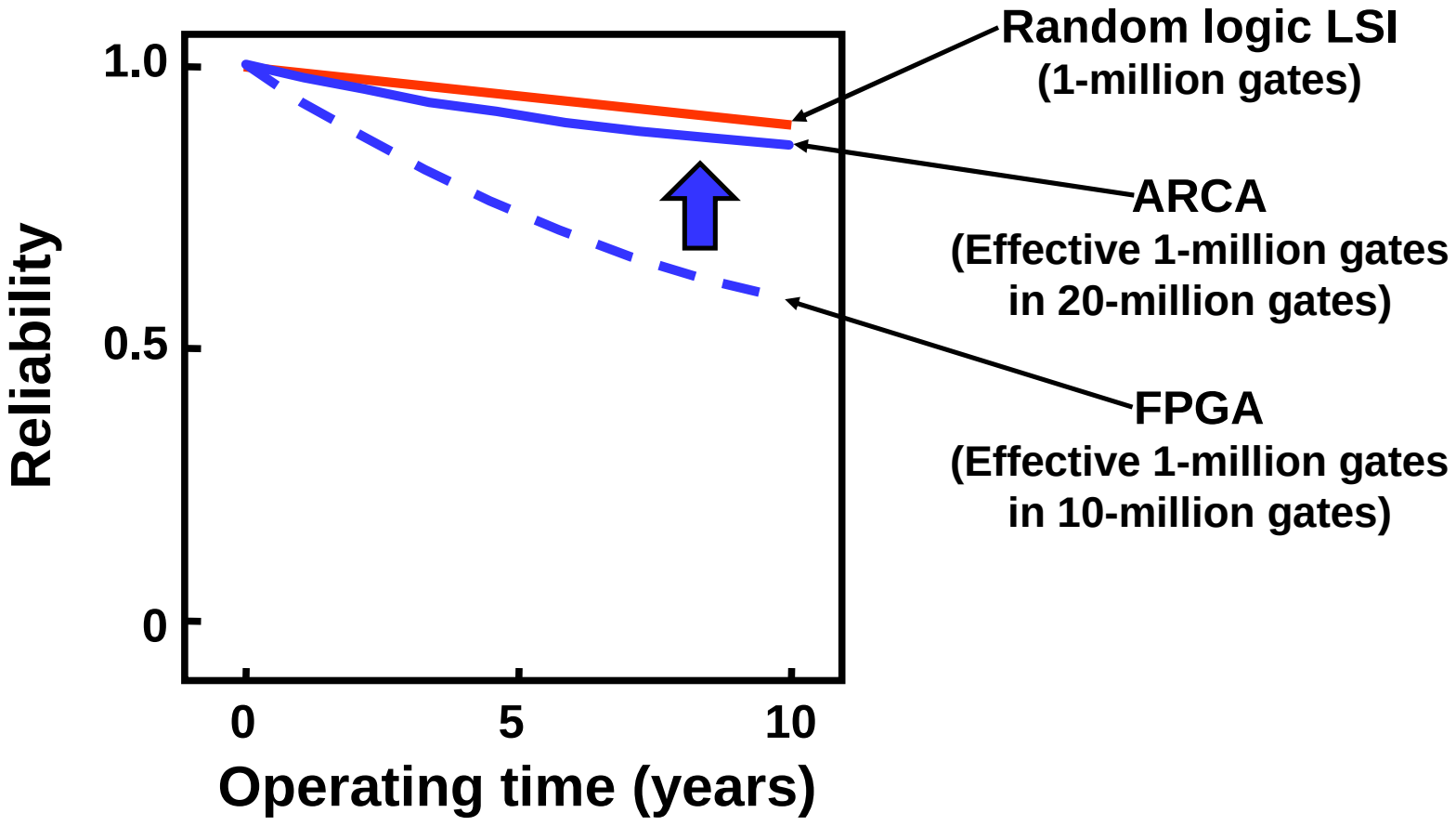
- Area Overhead
  - Two-rail logic implementation

    ⇒ x2
  - Recovery controller

    ⇒ 2% @ 100x100 ARCA



Improved Reliability by ARCA



- Reliability of FPGA is improved by ARCA.

Summary

- **The dependability of VLSI is threatened by;**
  (1) The deterministic power / signal integrity problems at design-phase
  (2) The statistical device variation problems at manufacturing-phase
  (3) The time-dependent degradation problems after shipping

- **The prompt solutions to these problems are essential to keep the continuous evolution of VLSIs.**

- **Future dependable VLSIs should introduce the fault-tolerant systems by the feed-back design-flow.**

References

[1] M. Bohr, “High-performance logic technology and reliability challenges”, IEEE International Reliability Physics Symposium, 2003.

[2] International Technology Roadmap for Semiconductors, 2002 Update. http://public.itrs.net/

[3] N. Oda et al., “A robust embedded ladder-oxide/Cu multilevel interconnect technology for 0.13 μm CMOS generation”, IEEE Symposium on VLSI Technology, pp. 34 – 35, 2002.

[4] M. Takamiya et al., "An on-chip, 100-GHz sampling rate, 8-channel sampling oscilloscope macro with embedded sampling clock generator", IEEE International Solid-State Circuits Conference, pp. 182 – 183, 2002.

[5] M. Beattie et al., “Inductance 101: modeling and extraction”, Design Automation Conference, pp. 323 – 328, 2001.

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[7] X. Huang et al., “Loop-based interconnect modeling and optimization approach for multigigahertz clock network design”, IEEE Journal of Solid-State Circuits, pp. 457 – 463, 2003.

[8] T. Ezaki et al., “Investigation of realistic dopant fluctuation induced device characteristics variation for sub-100 nm CMOS by using atomistic 3D process/device simulator”, IEEE International Electron Devices Meeting, pp. 311 – 314, 2002.

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[10] K. Yoshida et al., “Stress-induced voiding phenomena for an actual CMOS LSI interconnects”, IEEE International Electron Devices Meeting, pp. 753 – 756, 2002.

[11] A. Shibayama et al., "An autonomous reconfigurable cell array for fault-tolerant LSIs", IEEE International Solid-State Circuits Conference, pp. 230 – 231, 1997.