19.5 On-Chip Jitter-Spectrum-Analyzer for High-Speed Digital Designs

Makoto Takamiya, Hiroki Inohara[1], Masayuki Mizuno

NEC, Kanagawa, Japan
[1]NEC, Tokyo, Japan

The inability to predict accurately the degree to which such performance-degradation factors as jitter induced by power supply noise are likely to occur is an increasingly serious issue [1]. This inability tends to slow the rate of advance in high-speed digital LSI performance. This suggests that it may be useful to replace traditional digital LSI feedforward design-flow for high-speed LSIs by a feedback design-flow based on previously obtained experimental data. As a first step, an on-chip jitter-spectrum analyzer (JSA) is developed which locates and analyzes trouble-spots in off- and on-chip power-and-clock-distribution-networks during actual field operation. An on-chip frequency-domain measurement is demonstrated for the first time. Data thus obtained is used to support a feedback design-flow approach which contributes significantly in advancing the performance of high-speed digital LSIs.

As shown in Fig. 19.5.1, the degree of jitter is determined by the degree to which power supply noise affects the circuits for clock generation and distribution. Power supply noise itself is determined by the power supply current (I_p) and the impedance (Z_p) of the hierarchical power supply networks (PSN) contained in the LSI, its package, and its PCB. In-field measurements of the jitter are essential because I_p fluctuates greatly with changes in LSI operations, and Z_p depends not only on on-chip PSN parameters but also on off-chip PSN parameters. Since each of the factors that determine jitter has its own unique frequency band, on the basis of jitter spectrum data obtained with the JSA, critical spots in both the power supply networks and the clock circuits are clearly identified in the frequency domain. This information is crucial to the work of reducing both power supply noise and clock jitter. By way of contrast, because on-chip conventional time-domain measurement circuits used to obtain power supply noise amplitudes [2] and jitter histograms [3] are unable to determine specific trouble-spot locations, they do not offer the same prospect of reducing either power supply noise or clock jitter.

Figure 19.5.2 is a block diagram of the JSA. One or more jitter measurement macros are first embedded in an LSI to be tested. These macros perform real-time successive in-field measurements of timing jitter, i.e. the discrepancy between the rising edge of a on-chip reference clock and the rising edge of a measured clock. This avoids the difficulty in off-chip probing of on-chip high-speed clock signals. Timing jitter is measured rather than the conventionally measured period jitter [3] in order to be able to obtain a wide range of spectra, from kHz to GHz. Jitter in on-chip reference clocks is not fatal because the timing-jitter to be measured is not an absolute value but a relative value based on the on-chip reference clock. Time-domain data is fed into a PC via a logic analyzer; the PC converts this data into frequency-domain data and then reports any trouble-spots.

Figure 19.5.3 shows two circuits for jitter measurement macros. The digital type in Fig. 19.5.3a is suitable for the measurement of high-speed clocks. Flip-flops are used to compare the respective phases of n reference signals and those of measured clocks, and the results are encoded by a priority encoder. The n reference signals have ΔT timing differences with each other and are generated from the phase interpolation of the delay in the delay lines. Careful design of the phase interpolator and the delay lines is required because jitter generated by them is added to the jitter of measured clocks. Furthermore, measured results are successively fed into a logic analyzer in order to obtain jitter spectra. This requires high-bandwidth outputs, thus increasing costs, a critical issue for in-field measurements. This problem is avoided, however, by using a decimation filter to reduce output bandwidths.

Figure 19.5.3b shows an analog-type. Unlike the digital-type, it has the advantage of directly measuring the jitter between two inputs, but its speed is limited by the sampling speed of its A/D converter. A sample-and-hold low-pass-filter may be added, obviating the need for a high sampling speed. Whether the rising edge of the measured clock is faster or slower than that of the reference clock, timing differences between them are successfully converted to analog voltages (V_x) by a phase-frequency-detector and a reset-charge-pump. The timing diagram is displayed in Fig. 19.5.4. By way of contrast, when the rising edge of a measured clock is ahead of a reference clock by ΔT, the ON-period of NMOS (N1) of the reset-charge-pump is longer than that of PMOS (P1) by ΔT, and V_x changes from $V_{dd}/2$ to $V_{dd}/2 - I_{cp}\Delta T/C$, where I_{cp} is the current of the current source and C is the capacitance. At T_1, which occurs just before the falling edge of the reference clock, V_x is sampled by the A/D converter. Then, at the falling edge of the reference clock, switch (SW) turns on, and V_x is reset to $V_{dd}/2$. When the rising edge of the measured clock is slower than that of the reference clock by ΔT, V_x changes from $V_{dd}/2$ to $V_{dd}/2 + I_{cp}\Delta T/C$. In actual measurements, the relationship between ΔT and V_x is calibrated to remove any effects of PVT variations or circuit non-linearity. The obtained V_x values are digitized by the A/D converter.

A micrograph of an analog-type jitter measurement macro, fabricated in a 1.8V 0.18μm CMOS process, is shown in Fig. 19.5.5. To evaluate the front-end performance of the macro, the test chip does not contain a low-pass-filter or an A/D converter. The area of the macro is 137μm by 95μm. V_x is measured by high-frequency probes via an open-drain buffer.

Figure 19.5.6 shows a measurement-based calibration function between V_x and ΔT. Jitter is measured over a range of ± 200ps, and the sensitivity is 3.2mV/ps. Figure 19.5.7 shows a jitter spectrum and lists peak-to-peak (p-p) jitter. Results are obtained from JSA measurements of jitter in a 1ns-inverter-chain operating at a 1GHz clock. To modulate the jitter, power supply noise is applied to the chain by an on-chip noise generator. When the power supply noise is off and off-chip decoupling capacitors are removed, p-p jitter was 78.7ps. High peaks in the spectrum indicate trouble-spots in the power supply networks and appear to result from resonance. To confirm this, power supply noise at a peak frequency of 120MHz and non-peak frequency of 150MHz are experimentally applied. With 120MHz noise, p-p jitter was 281.1ps, while it was 99.7ps for 150MHz noise. These results clearly support the assumption that resonance generates the large power supply noise which results in high peaks. To eliminate this resonance, off-chip decoupling capacitors are added. As a result, p-p jitter decreased to 23.3ps, 35.7ps, and 26.1ps at quiet supply, 120MHz noise, and 150MHz noise, respectively, and indicates a successful power-supply-design.

References:

[1] T. Rahal-Arabi et al., "Design and Validation of the Pentium III and Pentium 4 Processors Power Delivery," *Dig. Symp. VLSI Circuits*, pp. 220–223, June 2002.
[2] A. Muhtaroglu et al., "On-Die Droop Detector for Analog Sensing of Power Supply Noise," *Dig. Symp. VLSI Circuits*, pp. 193–196, June 2003.
[3] R. Kuppuswamy et al., "On-Die Clock Jitter Detector for High Speed Microprocessors," *Dig. Symp. VLSI Circuits*, pp. 187–191, June 2001.

 0-7803-8267-6/04

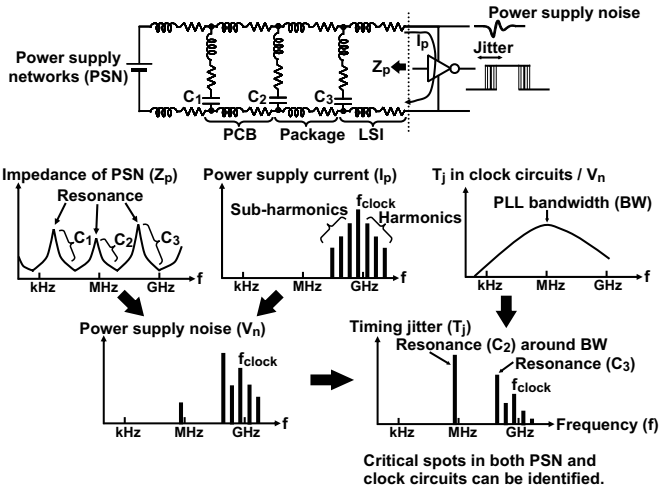


Figure 19.5.1: Principle of jitter generation in frequency-domain.

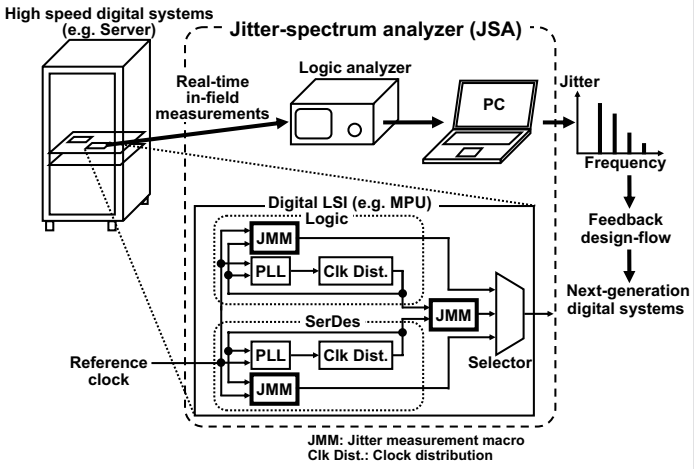


Figure 19.5.2: Jitter-spectrum analyzer and its implementation.

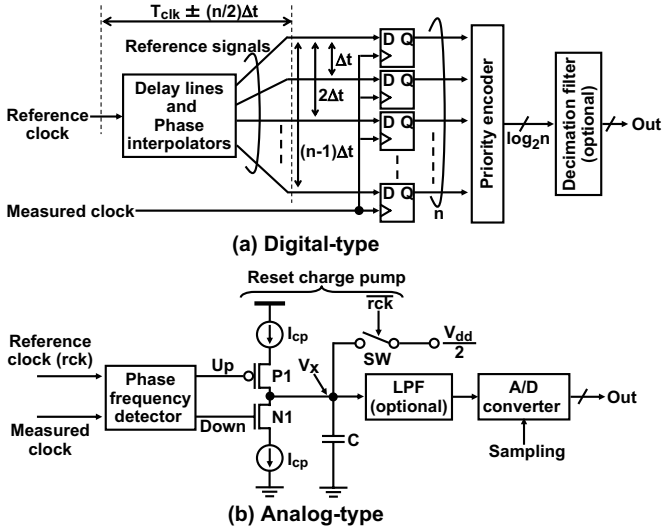


Figure 19.5.3: Digital- and analog-type jitter measurement macros.

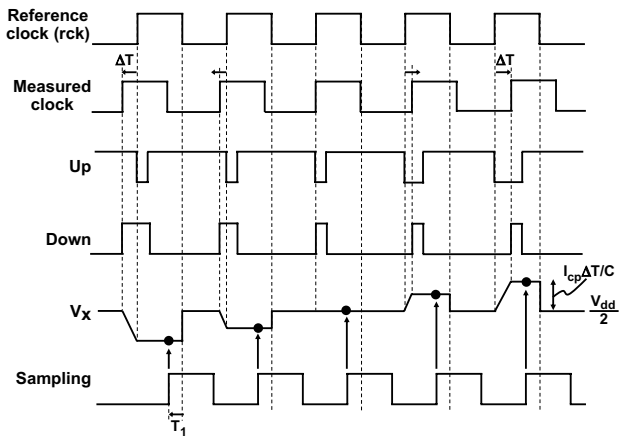


Figure 19.5.4: Timing diagram for analog-type jitter measurement macro.

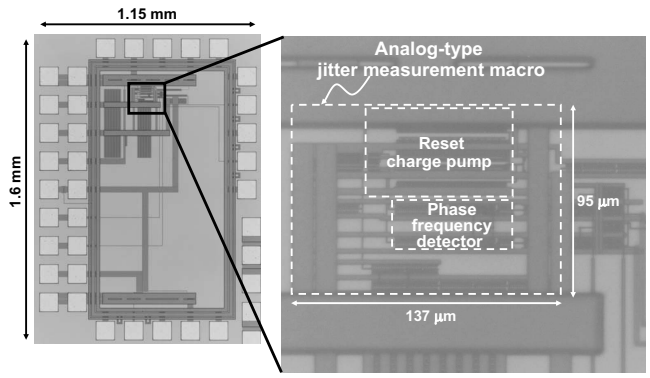


Figure 19.5.5: Chip microphotograph.

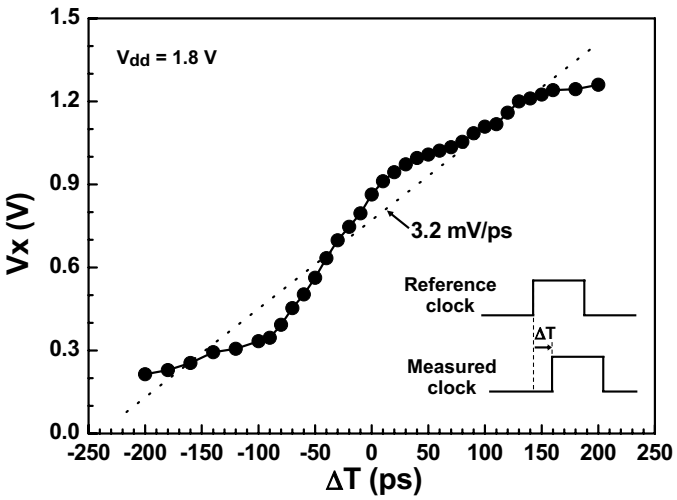
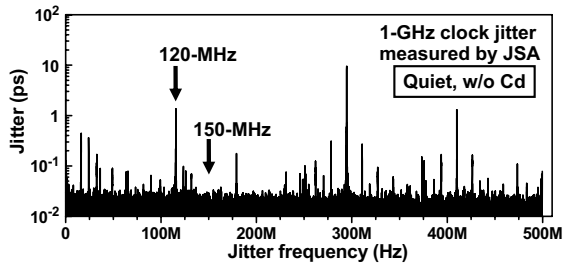


Figure 19.5.6: Measured V_x vs. ΔT, used for calibration.

0-7803-8267-6/04



Power supply	Peak-to-peak jitter	
	Without decoupling capacitors (C_d)	With C_d
Quiet	78.7 ps (Upper spectrum)	23.3 ps
120-MHz noise (*On* the resonant frequency)	281.1 ps	35.7 ps
150-MHz noise (*Off* the resonant frequency)	99.7 ps	26.1 ps

Figure 19.5.7: Jitter spectrum and peak-to-peak jitter measured by JSA.

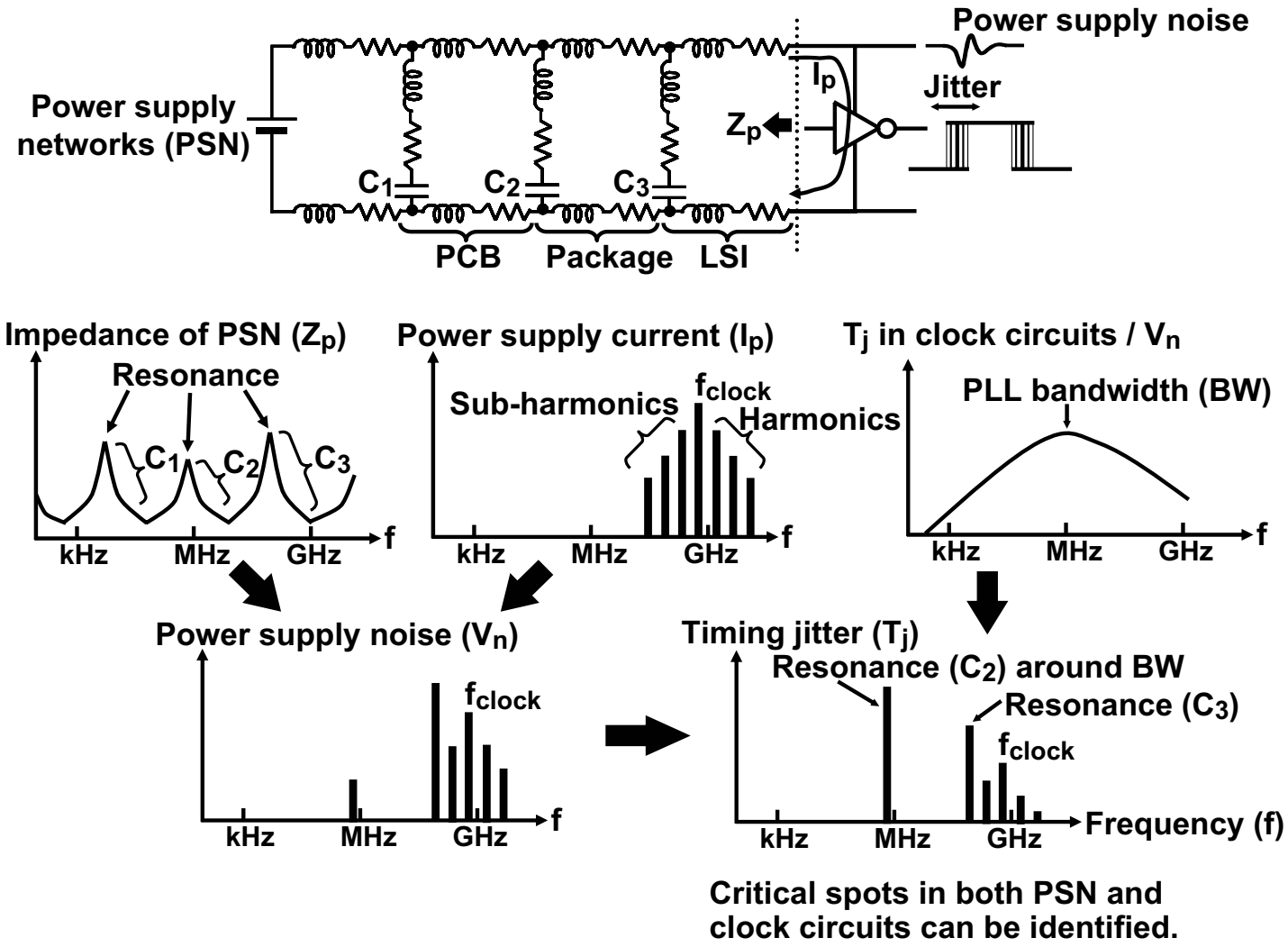


Figure 19.5.1: Principle of jitter generation in frequency-domain.

0-7803-8267-6/04

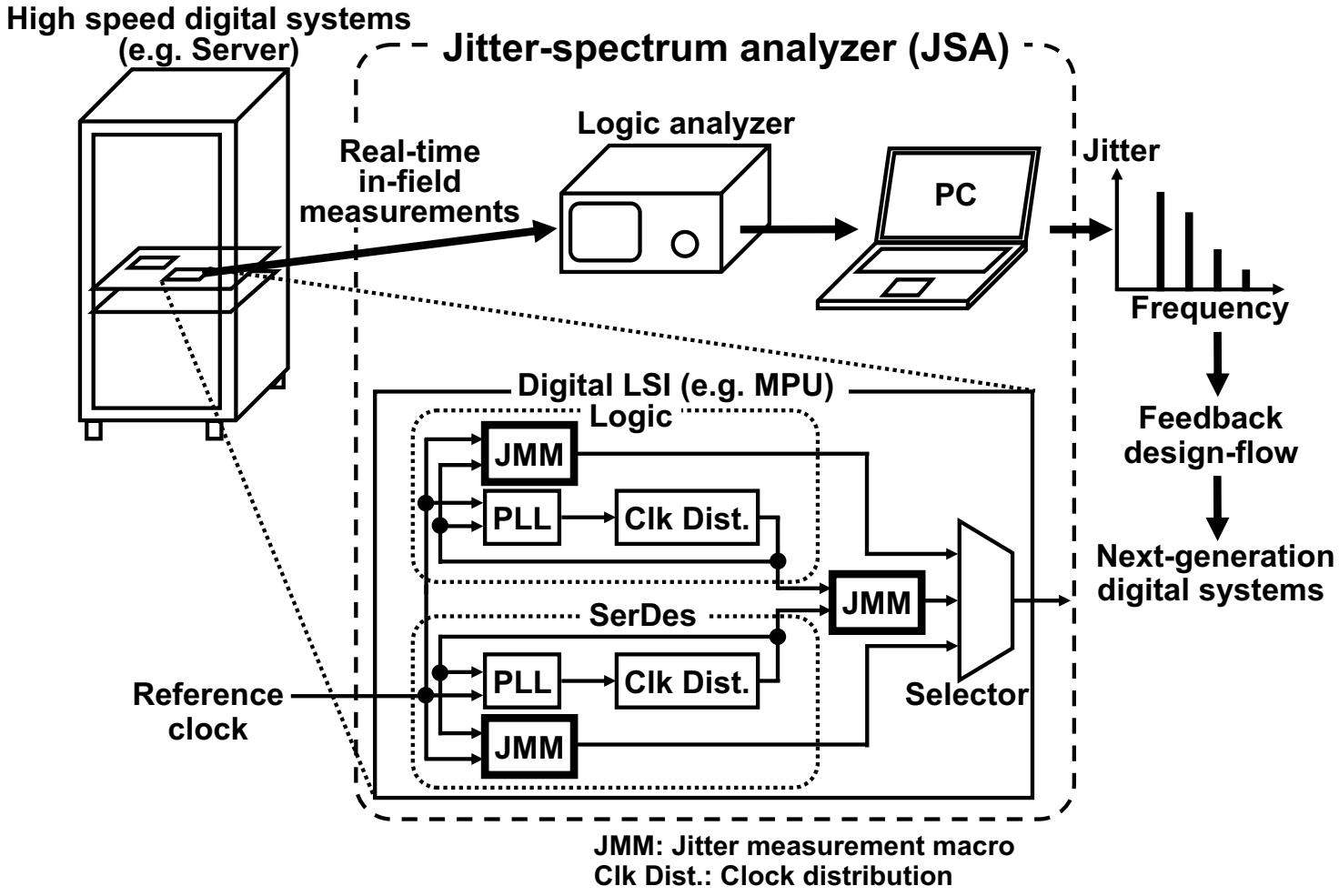


Figure 19.5.2: Jitter-spectrum analyzer and its implementation.

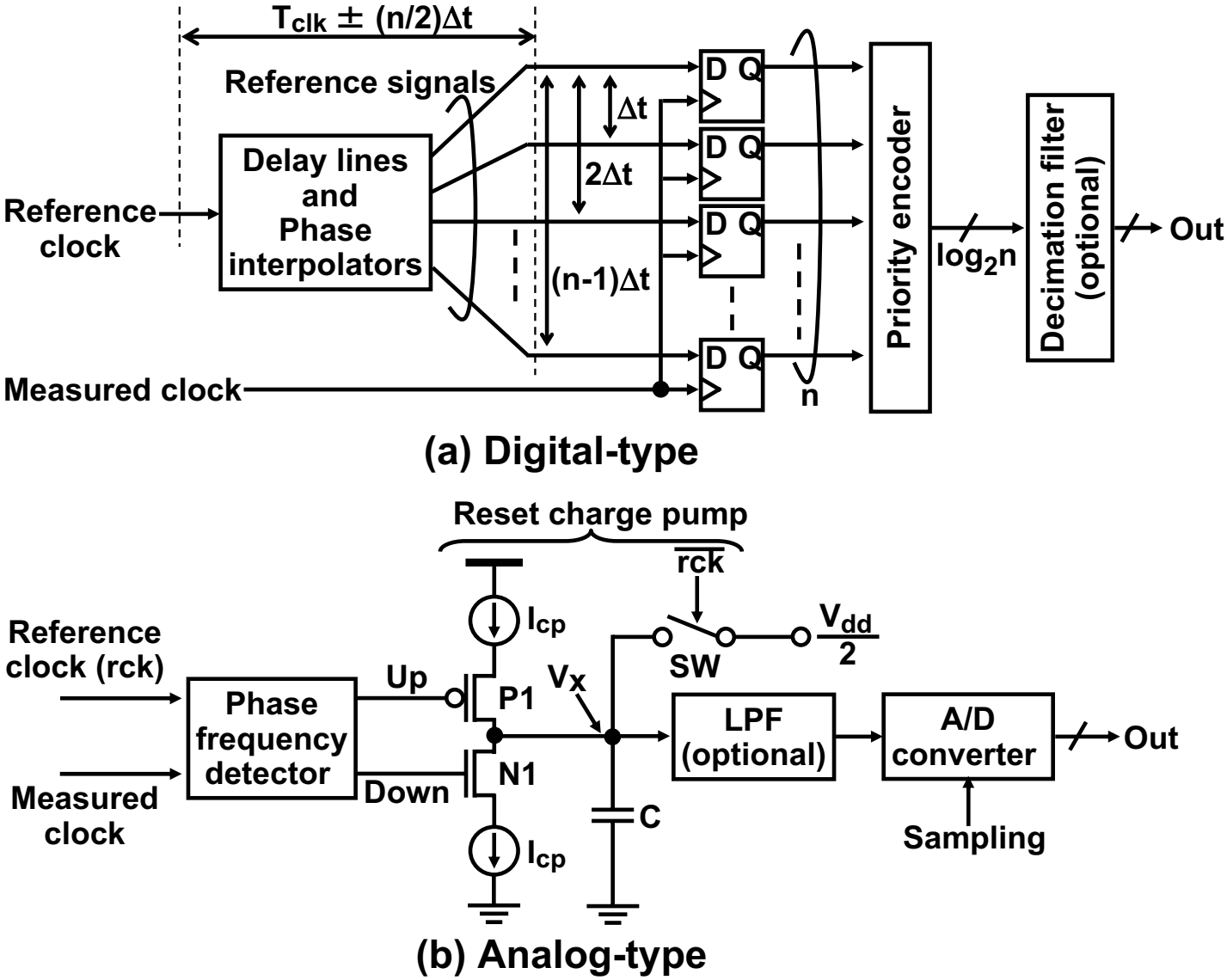


Figure 19.5.3: Digital- and analog-type jitter measurement macros.

0-7803-8267-6/04

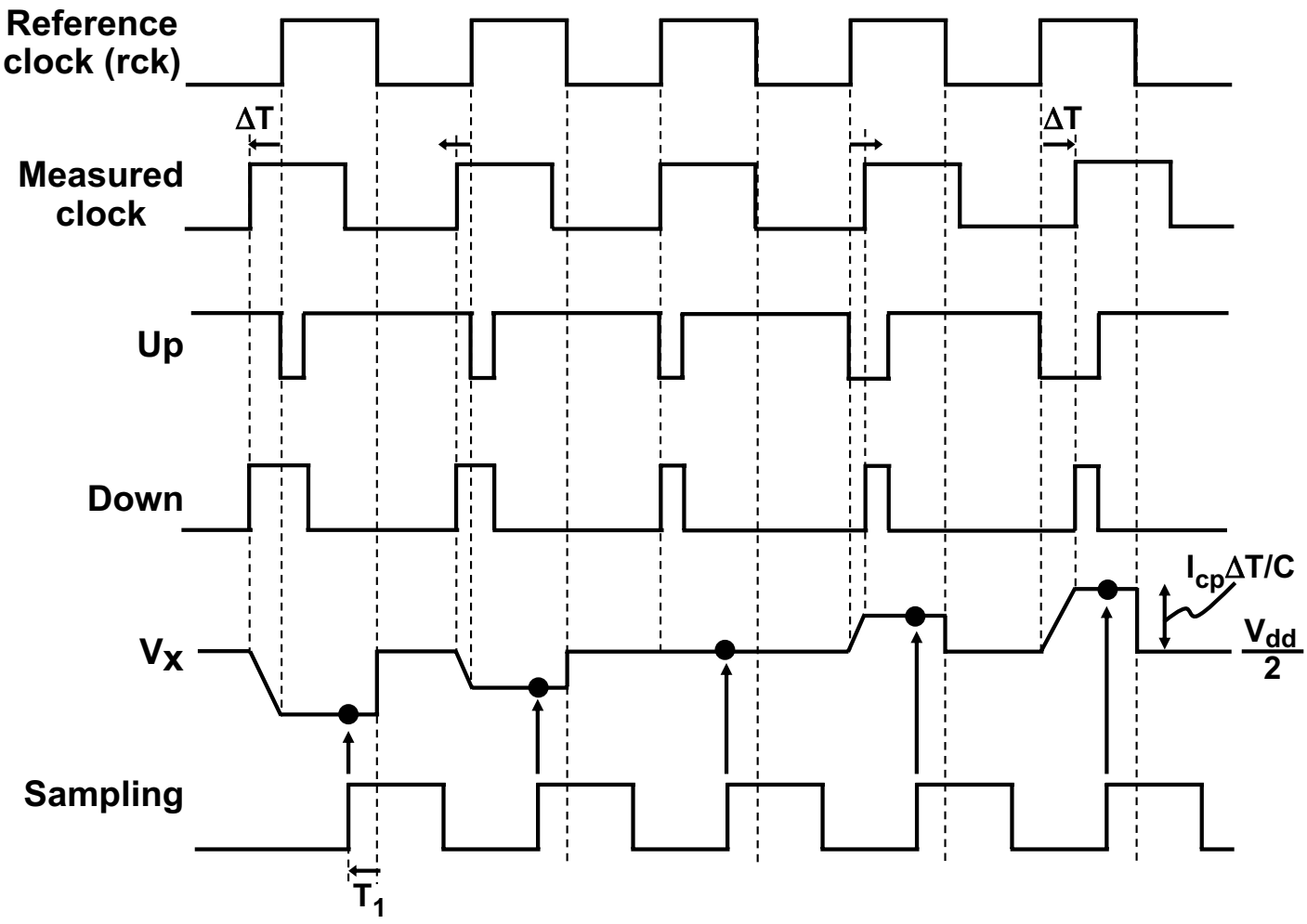


Figure 19.5.4: Timing diagram for analog-type jitter measurement macro.

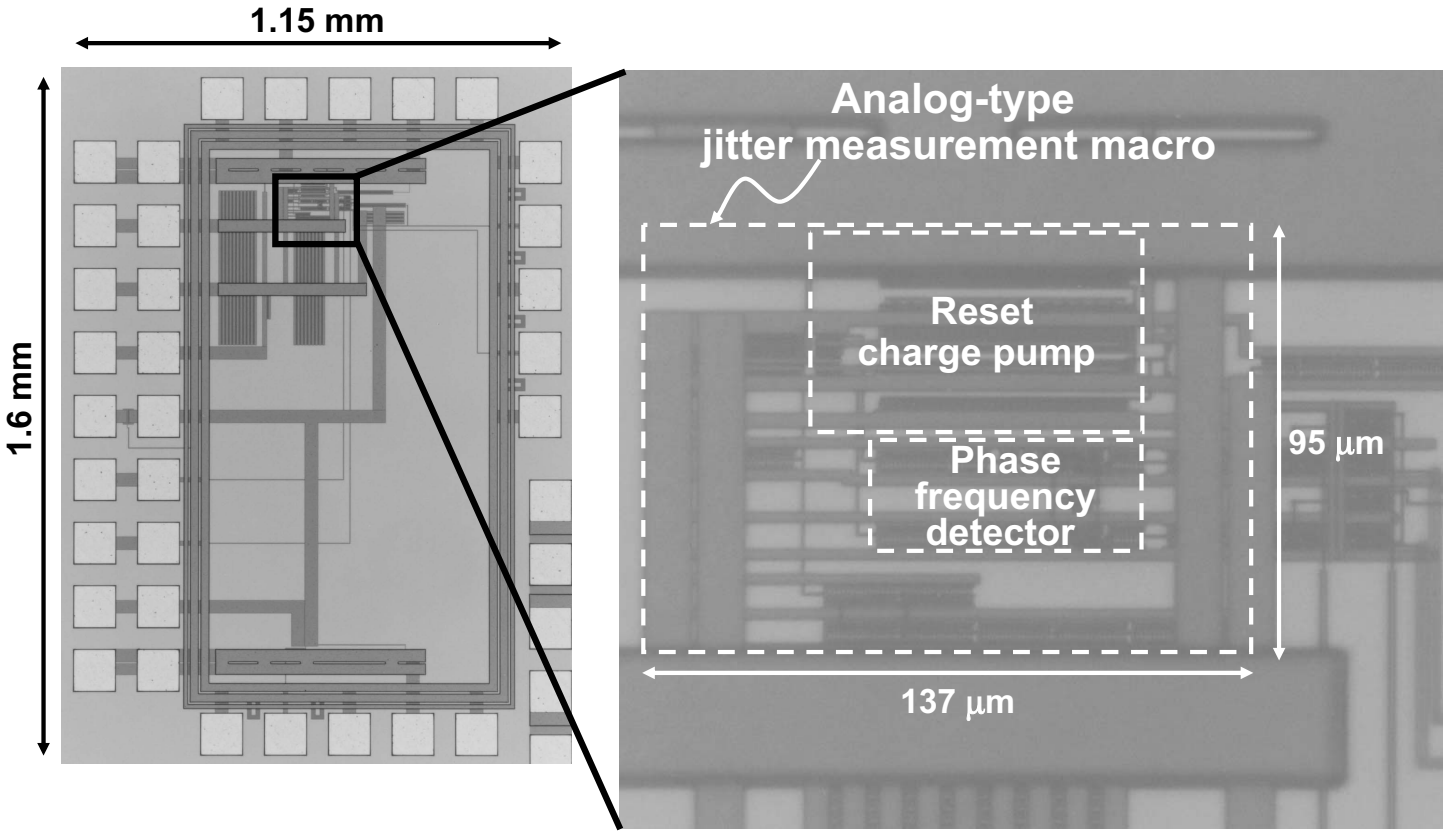


Figure 19.5.5: Chip microphotograph.

0-7803-8267-6/04

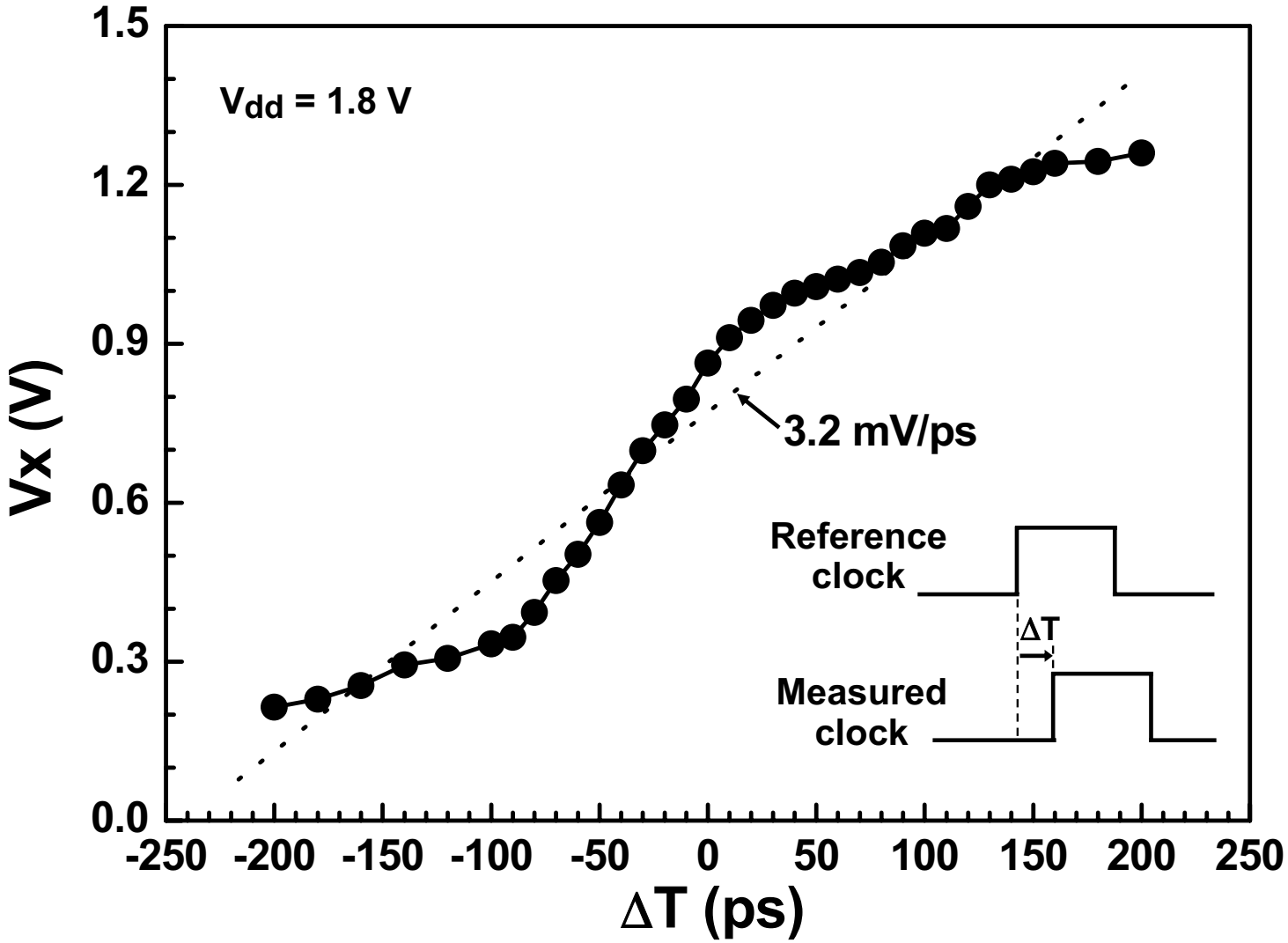
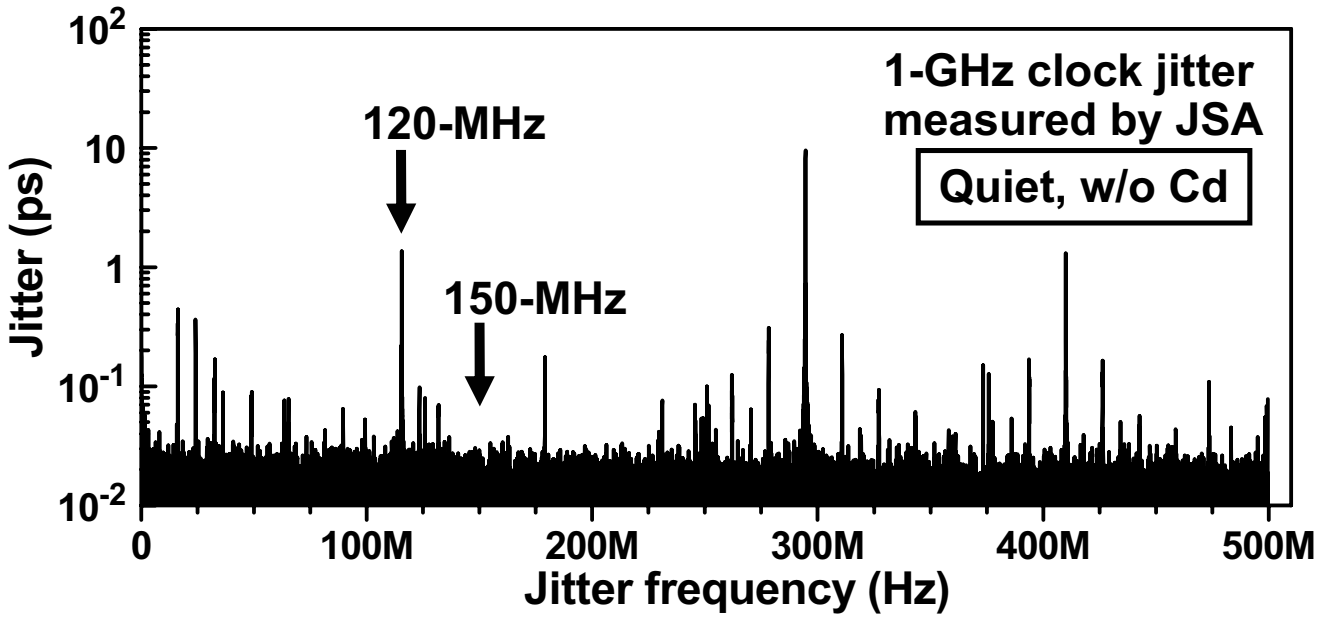


Figure 19.5.6: Measured V_x vs. ΔT, used for calibration.

0-7803-8267-6/04



Power supply	Peak-to-peak jitter	
	Without decoupling capacitors (C_d)	With C_d
Quiet	78.7 ps (Upper spectrum)	23.3 ps
120-MHz noise (*On* the resonant frequency)	281.1 ps	35.7 ps
150-MHz noise (*Off* the resonant frequency)	99.7 ps	26.1 ps

Figure 19.5.7: Jitter spectrum and peak-to-peak jitter measured by JSA.

0-7803-8267-6/04