# A Sampling Oscilloscope Macro toward Feedback Physical Design Methodology

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**Abstract**

A sampling oscilloscope macro which is easily embedded in an actually operating LSI in the field has been developed to enable practical use of the feedback physical design methodology. The macro features (1) a high-speed input-isolated comparator to measure signals on GHz-digital-LSIs, (2) a voltage-range converter to widen the input range to 2 V at a 1-V supply voltage, (3) D/A converters to eliminate the use of analog I/O for the macro, (4) an on-chip power supply noise filter to eliminate the need for a dedicated power supply, and (5) an embedded clock generator to eliminate the need for a dedicated clock signal. By using the macro, the world's first measurement of an undershooting waveform caused by an on-chip inductive effect has been demonstrated.

## Introduction

The rapid speed-up of digital LSIs, such as MPU and SerDes, has been accompanied by problems caused by signal integrity degradation such as power supply noise, substrate noise, and an on-chip inductive effect. This is a serious problem that delays development schedules because of the need to investigate the cause of errors and increases the cost because of unanticipated LSI re-fabrication. To avoid this situation, the design margin has had to gradually become larger with the process scaling, resulting in undesirable constraints on LSI speed, increased area, or greater power consumption. The signal integrity degradation will become more serious in the future, and it will become more difficult to predict the problem, because the advances made in CAD tools are not keeping up with the increasing complexity in the relevant physical phenomena and the increasing VLSI scale.

To solve this problem, a feedback physical design methodology has been proposed [1]. In this methodology, on-chip measurement macros are embedded in an actually operating LSI in the field, simulated results are validated using the measured signal integrity degradation obtained from the macros, and calibrated design tools are then applied to future design. The on-chip measurement is necessary, because it is difficult to measure the on-chip waveform through a conventional probing method because of the difficulty of probing in the flip-chip package and the insufficient bandwidth. The measurement during the actual operations in the field is important, because the degradation depends on the package, the application processing, and the layout of each LSI.

A jitter measurement macro to demonstrate the methodology was discussed in [1]. This paper describes a sampling oscilloscope macro for the methodology, which can capture high-speed waveforms. The conventional measurement macros [2-5] used to measure the on-chip waveforms cannot be used for the feedback physical design methodology because they fall short in one or more of the following circumstances.

1) GHz-clock operations.
2) An input voltage range greater than the supply voltage.
3) No analog I/O. It is impossible to distribute a clean analog signal in a noisy digital LSI.
4) No dedicated power supply. A dedicated power supply raises the cost for the chip area and the package.
5) No dedicated clock signal. The dedicated clock signal raises the package cost.

The proposed sampling oscilloscope macro is able to operate under all of the above circumstances.

## Sampling Oscilloscope Macro

Fig. 1 shows a block diagram of the proposed sampling oscilloscope macro. The macro has been optimized to measure an overshooting/undershooting waveform caused by the on-chip inductive effect in this design, however, it can be applied to another high-speed waveform such as the power supply noise and the substrate noise. To measure the overshooting/undershooting, an input voltage range larger than the supply voltage is needed, so the voltage-range converter reduces the measured signal's amplitude. The output of the converter and the reference voltage are compared by a comparator. The comparator needs to operate at the same speed as the clock of the high-speed digital LSI. An input-isolated comparator enables 68%-increase of the frequency of comparison. To increase the bandwidth of the sampling oscilloscope macro, a high sampling rate is needed. $\Delta T$-step sampling is effectively achieved by sampling the measured signal with a cycle time of T using a sampling clock with a cycle time of $T+\Delta T$. In this design, the minimum $\Delta T$ is 5 ps, which corresponds to a sampling rate of 200 Gsample/s. The cycle time of the macro outputs are $T^2/\Delta T$. The sampling clock need not be supplied from an off-chip pulse generator, because it is generated by the VCO in the macro. Also, neither the reference voltage nor the control voltage for the VCO needs to be supplied from an off-chip voltage source because both are generated by D/A converters in the macro. Therefore, all the inputs and the outputs for the macro are digital signals, and analog I/O is not needed. To suppress the power supply noise from the surrounding digital LSI to

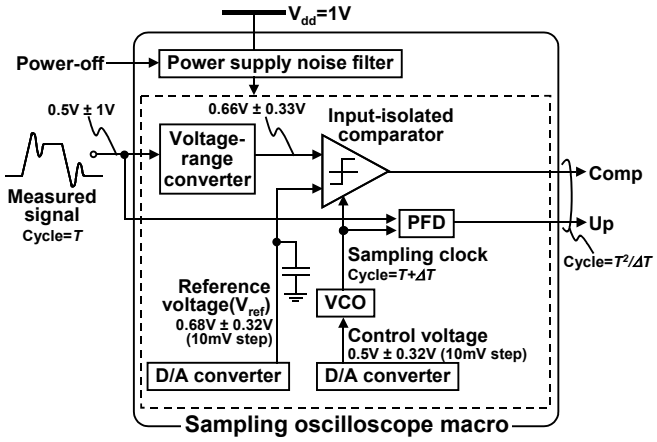



Fig. 1 Block diagram of the sampling oscilloscope macro

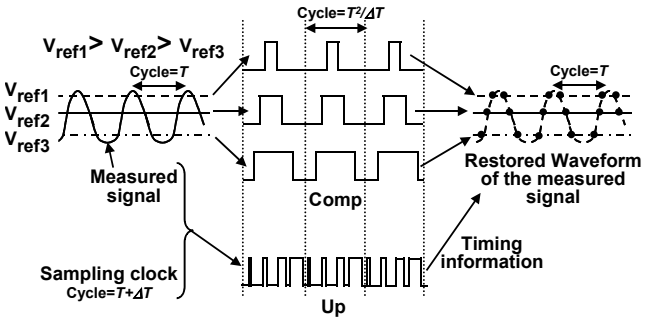



Fig. 2 Procedure to restore the waveform of the measured signal by using both the comparator output (Comp) and PFD output (Up)

the macro, an on-chip power supply noise filter is embedded in the macro; this eliminates the need for a dedicated power supply for the macro.

Fig. 2 shows a procedure to restore the waveform of the measured signal by using both the comparator output (Comp) and the phase-frequency-detector (PFD) output (Up). When only Comp is used, the waveform of the measured signal cannot be restored, because there is no timing information between the Comp signals. We can, however, restore the waveform when the PFD is used in combination with the comparator. When the reference voltage is varied from $V_{ref1}$ to $V_{ref3}$, the duty-ratio of Comp changes. On the other hand, Up indicates the timing information between the measured signal and the sampling clock. We can restore the waveform of the measured signal by simultaneously measuring Comp and Up for the various reference voltages and overlapping the Comp waveforms by using the Up signals as a reference.

## Building Blocks

### *A. Input-isolated Comparator*

Fig. 3 (a) is a schematic diagram of the proposed input-isolated comparator. It compares an input voltage (In) and the reference voltage ($V_{ref}$) at the moment when the Clk signal changes from high to low. Fig. 3 (b) shows the simplified circuits of the comparator. When Clk is high, both the input and the output of the inverters are shorted, which is the fastest condition for the two inverters to become stable. When Clk is low, the output is fixed and is not affected by the transition of In because the Reset-node is isolated from In. To demonstrate the speed advantage of the proposed comparator, we compared its performance with that of a conventional comparator [6] shown in Fig. 4 (a). When Clk is high, both the Reset-node and the Set-node are biased to $V_{dd}$, which is the slowest condition for the two inverters to become stable. While Clk is low as shown in Fig. 4 (b), the comparator output is always affected by the transition of In, because the Reset-node is not isolated from In. Fig. 5 shows the simulated dependence of the maximum clock frequency on the voltage difference ($\Delta V$) between In and $V_{ref}$ for both the conventional and the proposed comparators. As $\Delta V$ increases, the maximum clock frequency also increases. At a fixed $\Delta V$, the maximum clock frequency of the proposed comparator is higher than that of the conventional comparator. For example, at $\Delta V$ of 10 mV, the maximum clock frequency of the conventional comparator is 2.38 GHz, while that of the proposed comparator is 4.0 GHz, which is 68% higher than that of the conventional comparator. Though the lower limit of $\Delta V$ of the conventional comparator is 8 mV, that of the proposed comparator is less than 1 mV.

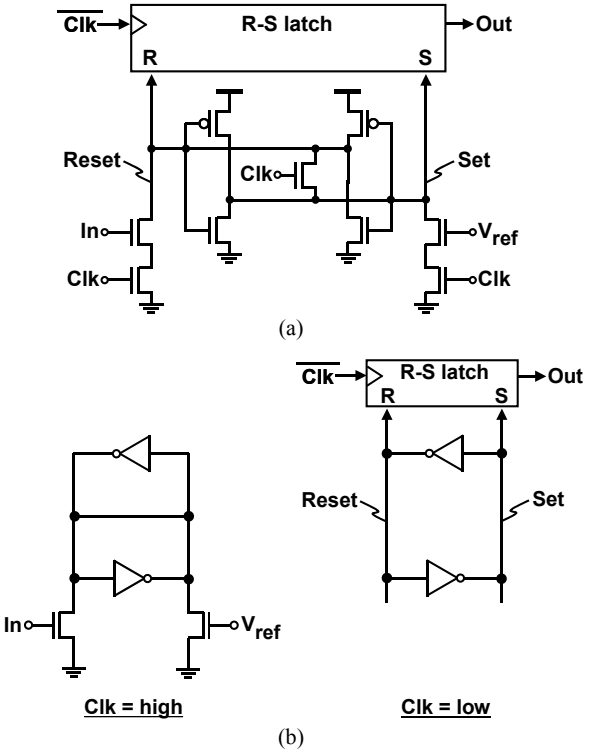



Fig. 3 (a) Schematic diagram and (b) Simplified circuits of the proposed input-isolated comparator

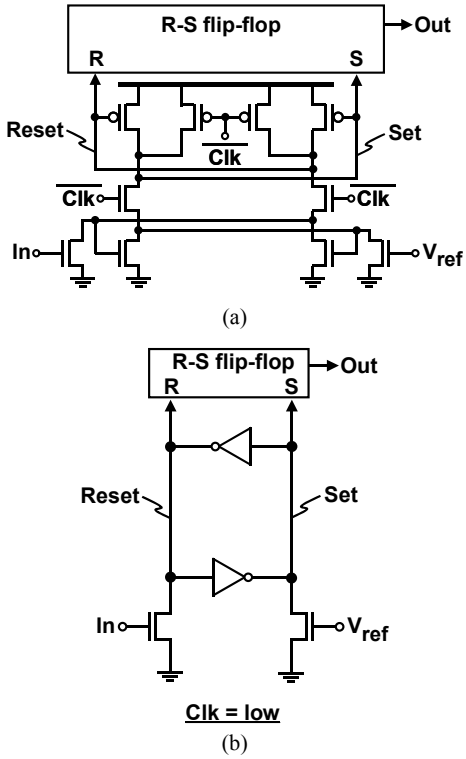



Fig. 4 (a) Schematic diagram and (b) Simplified circuit of the conventional comparator [6]

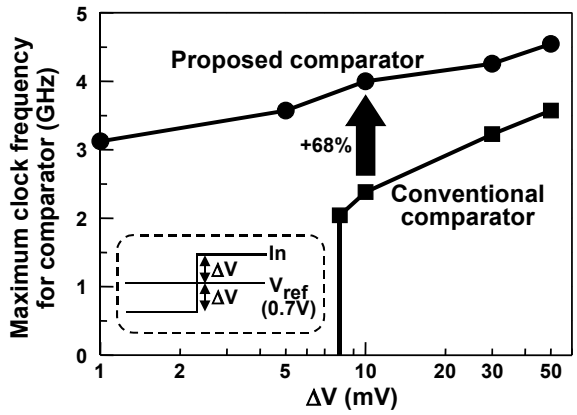
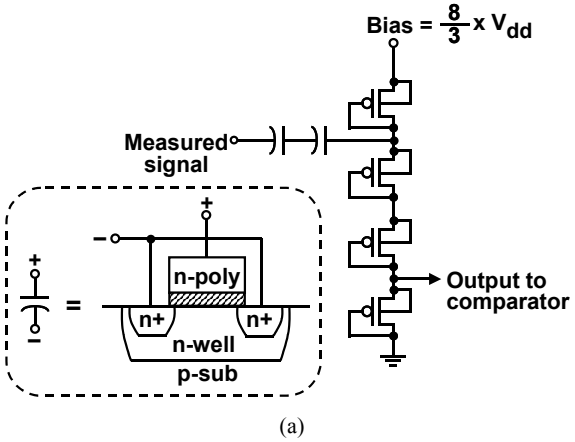


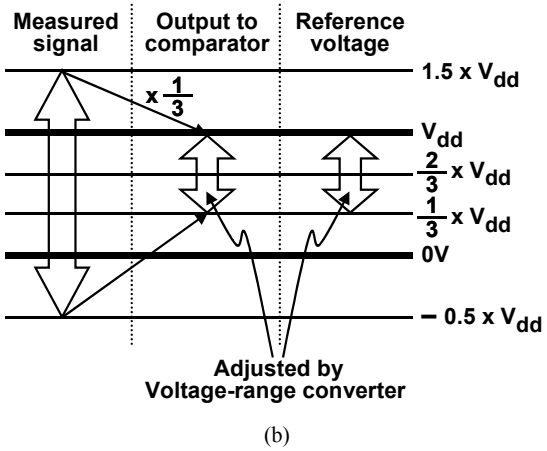

Fig. 5 Dependence of the maximum clock frequency for the conventional and the proposed comparators on the voltage difference (ΔV) between In and $V_{ref}$

*B. Voltage-range Converter*

Fig. 6 (a) shows a schematic diagram of the developed voltage-range converter. The bias voltage, which can be generated by an on-chip boosted-voltage-generator, is divided into quarters through a cascade connection of four pMOSFETs. The MOS gate capacitors are used as the capacitors for the converter. To avoid gate oxide breakdown due to excess voltage, two MOS gate capacitors are connected in series. The converter functions as a high-pass-filter and its cut-off frequency is 20 MHz. At the frequencies higher than 20 MHz, the capacitance of the two MOS gate capacitors is not added to the measured signal. Fig. 6 (b) shows the relation between the input range and the output range of the converter. The converter reduces the voltage amplitude to one-third and shifts the DC-level from $V_{dd}/2$ to 2/3 x $V_{dd}$. Therefore, the voltage-range of the measured signal from -$V_{dd}/2$ to 3/2 x $V_{dd}$ fits in with that of the reference voltage from 1/3 x $V_{dd}$ to $V_{dd}$.




(a)




(b)

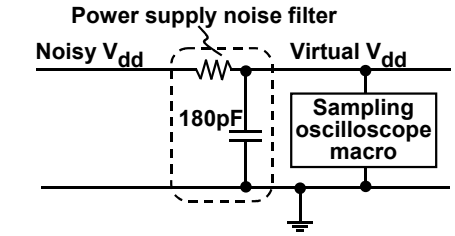
Fig. 6 Voltage-range converter. (a) Schematic diagram. (b) Relation between the input range and the output range of the converter.

*C. D/A Converters*

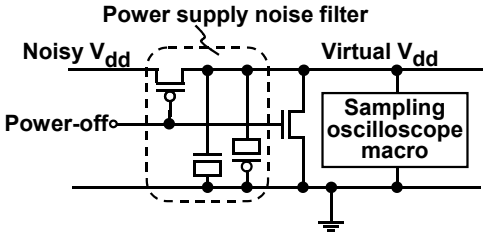
Both the reference voltage and the control voltage for the VCO are generated by the two 6-bit folded-string D/A converters[7]. The layout area of the D/A converter is as small as 120 μm by 20 μm.

*D. Power Supply Noise Filter*

Fig. 7 (a) shows an equivalent circuit for the on-chip power supply noise filter, and Fig. 7 (b) shows its circuit implementation. The power supply noise is blocked by inserting an RC low-pass-filter between a noisy $V_{dd}$ for a digital




(a)




(b)

Fig. 7 (a) Equivalent circuit and (b) Circuit implementation of the on-chip power supply noise filter

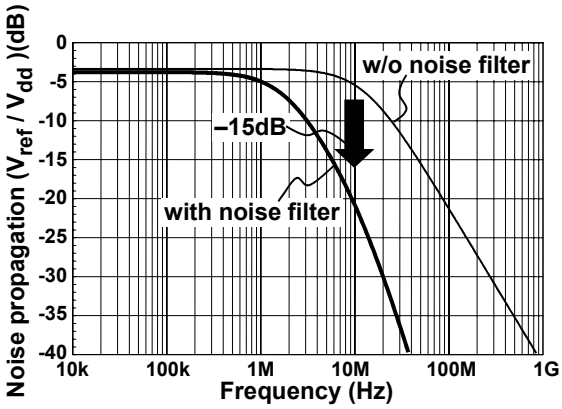



Fig. 8 Frequency dependence of the noise propagation from the noisy $V_{dd}$ to the reference voltage

LSI and a virtual $V_{dd}$ for the sampling oscilloscope macro. MOS gate capacitors are used as the 180-pF capacitors, and a pMOSFET is used as the resistor, which enables the sampling oscilloscope macro to power-off when not being used. Fig. 8 shows the simulated frequency dependence of noise propagation from the noisy $V_{dd}$ to the reference voltage with and without the power supply noise filter. The cut-off frequency of the noise filter was 2 MHz. The low-pass-filter characteristics without the noise filter was caused by the resistance-array for the D/A converter and the capacitance shown in Fig. 1. Use of the noise filter decreased the noise propagation by –15 dB at 10 MHz.

## Experimental Results and Discussions

Fig. 9 shows a micrograph of a sampling oscilloscope macro fabricated with an 1.0 V 90-nm ASPLA CMOS process. The macro area was 350 µm by 140 µm. To demonstrate the performance of the macro, the signal integrity degradation due to the on-chip inductive effect was measured. Fig. 10 shows a measured circuit. The far-end of the 2mm-wire was connected to the sampling oscilloscope macro. The additional capacitance due to the sampling oscilloscope macro was only 10 fF, which was less than 5% of the capacitance of the 2mm-wire, and did not affect the original waveform.

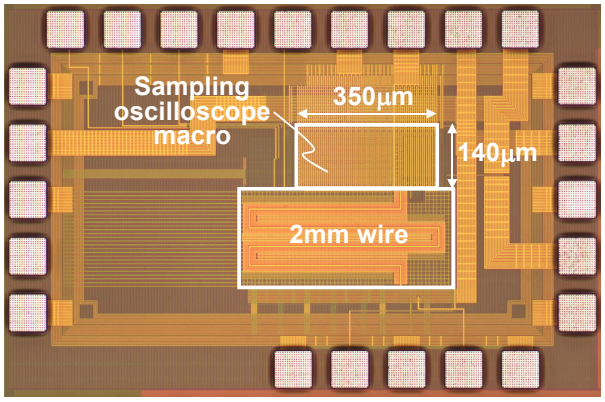



Fig. 9 Chip micrograph

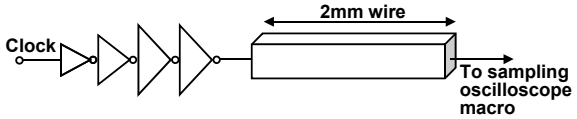



Fig. 10 Measured circuit

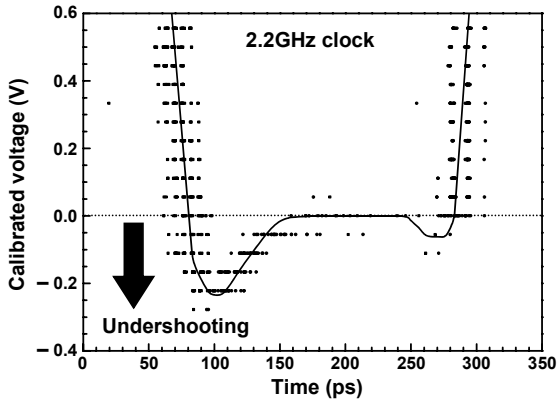



Fig. 11 Undershooting waveform measured by the sampling oscilloscope macro

Table 1 Comparison of on-chip measurement macros

| Reference | [2] JSSC96 | [3] ISSCC2000 | [4] ISSCC2002 | [5] VLSI2003 | This work |
|---|---|---|---|---|---|
| Measured target | Substrate noise | Substrate noise | Power supply & substrate noise | Power supply noise | High-speed signal |
| CMOS process | 0.8 µm | 0.6 µm | 0.13 µm | 0.09 µm | 0.09 µm |
| Clock frequency | 5 MHz | 50 MHz | 800 MHz | √ ~GHz | √ 2.2 GHz |
| Input range | –20 mV ~ 10 mV | –15 mV ~ 15 mV | –0.3 V ~ $V_{dd}$+ 0.3 V | $V_{dd}$ / 2 | √ –0.5 x $V_{dd}$~ 1.5 x $V_{dd}$ |
| Analog I/O | Yes | Yes | Yes | √ No | √ No |
| Dedicated power supply | Yes | Yes | Yes | Yes | √ No |
| Sampling clock | External supply | External supply | √ On-chip generation | √ No need | √ On-chip generation |

Fig. 11 shows an undershooting waveform measured by the sampling oscilloscope macro. The clock frequency was 2.2 GHz. The 0.2-V undershooting of clock signal caused by the on-chip inductive effect has been successfully measured.

Table 1 compares recently reported designs and the proposed sampling oscilloscope macro. The proposed macro has the highest clock frequency and the widest input range. Because the macro requires no dedicated power supply, no analog I/O, and no dedicated clock signal, it is easily embedded in an actually operating LSI, and thus enables the feedback physical design methodology.

## Conclusions

The sampling oscilloscope macro fabricated with a 1.0 V 90-nm CMOS process occupies 350 µm x 140 µm and achieves 68%-increase of the operation frequency and the input voltage range of 2 V. The macro is easy to be embedded in an actually operating LSI, because it requires no dedicated power supply, no analog I/O, and no dedicated clock signal. By using the macro, the world's first measurement of an undershooting waveform caused by an on-chip inductive effect has demonstrated at 2.2-GHz clock.

## References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