A 6.7-fF/μm^2 Bias-Independent Gate Capacitor (BIGCAP) With Digital CMOS Process and Its Application to the Loop Filter of a Differential PLL

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***Abstract*—A linear bias-independent gate capacitor (BIGCAP) with large intrinsic capacitance and low parasitic capacitance is proposed. BIGCAP is composed of a pair of accumulation-mode n-poly gate capacitors in an n-well and a pair of pMOS gate capacitors, which requires no additional fabrication process steps. Measured results with 1.5-V 0.13-μm digital CMOS technology show that the intrinsic capacitance is 6.7 fF/μm^2 (6.7 times bigger than that of typical MIM capacitors) and the parasitic capacitance is 1.9% of the intrinsic capacitance (1/5 that of typical MIM capacitors). The linearity is $\pm$2.9% and capacitance variation across a wafer is as small as $\sigma = 0.096\%$. For a 0.1-V threshold voltage variation, the capacitance variation was only $\sigma = 0.69\%$ and the linearity ranged from $\pm$2.84% to $\pm$2.93%. For three types of BIGCAP using 1.5-V, 2.5-V, and 3.3-V MOSFETs, less than $\pm$4% linearity is achievable by optimizing the ratio (x) of the pMOS gate capacitors' area to the area of the n-poly gate capacitors, and the optimum x value is within a range of 15%–25%.**

BIGCAP has been applied to the loop filter of a differential phase-locked loop (PLL) and reduces the gate area of the largest loop filter capacitor to only 35% of that of the conventional design while achieving reasonable jitter of 7.0 ps (rms) and 74.4 ps (peak-to-peak) at 840 MHz with a 1.5-V supply.

***Index Terms*—Bias dependence, differential, gate capacitor, loop filter, phase-locked loop (PLL).**

I. Introduction

BIAS-INDEPENDENT (i.e., linear) capacitors are needed for many applications such as the loop filter of a phase-locked loop (PLL), level-shifter in I/O buffers, switched-capacitor circuits, phase compensation in operational amplifiers, data converters, and mixers. Metal–insulator–metal (MIM) or poly-to-poly capacitors are often used for bias-independent capacitors. Fig. 1 shows the capacitance density and the linearity of various capacitors in a 0.13-μm CMOS. MIM and poly-to-poly capacitors have excellent linearity. However, they require extra process steps and have small capacitance density. Recently, interdigitated metal capacitors such as vertical parallel plate capacitors [1]–[3] that require no additional process steps have been proposed. Kim *et al.* [3] presented a vertical parallel plate capacitor with 80% greater capacitance density than an MIM capacitor in a 0.12-μm CMOS, however, it used as many as eight metal layers and the capacitance density was less than 1/5 of that of conventional MOS gate capacitors. On the other hand, conventional MOS gate capacitors have large capacitance density and need no extra process steps. However, the linearity in MOS gate capacitors is terrible. There is a large gap between MIM capacitors and MOS gate capacitors in terms of the linearity and the capacitance.

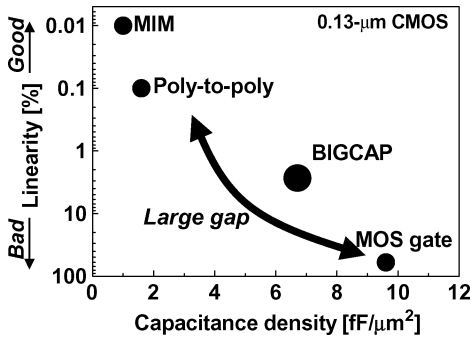

Fig. 1. The capacitance density and the linearity of various capacitors in a 0.13-μm CMOS.

In this paper, we propose a novel bias-independent gate capacitor (BIGCAP) to bridge the gap. The BIGCAP structure can be fabricated using a standard digital CMOS process with no extra process steps, has good linearity performance, and achieves high capacitance density. Bias-independent MOS gate capacitors have also been proposed in [4]–[6]; however, they have the following shortcomings: 1) the capacitance density is small, because the gate capacitors are serially connected [4]–[6], and 2) the functional bias range is narrow [5], [6]. Our BIGCAP solves both of these problems. The BIGCAP was applied to the loop filter of a differential PLL, and normal PLL operation was possible at small area.

II. BIGCAP Concepts and Configurations

Fig. 2 shows the configuration of BIGCAP, which is composed of a pair of accumulation-mode n-poly gate capacitors in an n-well and a pair of pMOS gate capacitors. All these capacitors can be fabricated using the standard digital CMOS process, because the pMOS gate capacitors are the same as pMOSFETs and the n-poly gate capacitors are the same as nMOSFETs with the n-well which is also used for pMOSFETs. In order to obtain symmetrical bias dependence, i.e., bipolarity, each pair has the same layout and only the connections are reversed.

Fig. 3 shows the measured C–V characteristics of n-poly gate capacitors and pMOS gate capacitors fabricated with a 1.5-V 0.13-μm digital CMOS technology [7]. The thin solid lines are

Manuscript received April 21, 2004; revised November 22, 2004.

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Digital Object Identifier 10.1109/JSSC.2005.843620

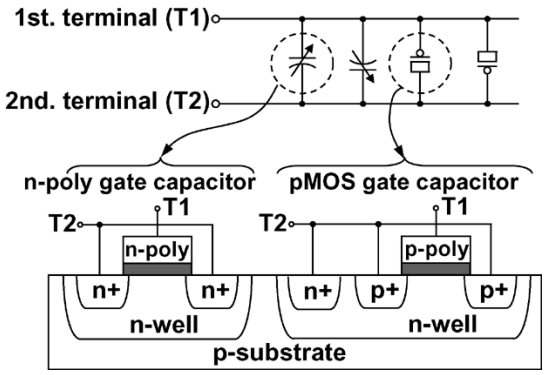


Fig. 2. Configuration of BIGCAP. The bias dependence of the capacitance of the n-poly and pMOS gate capacitors cancel each other out.

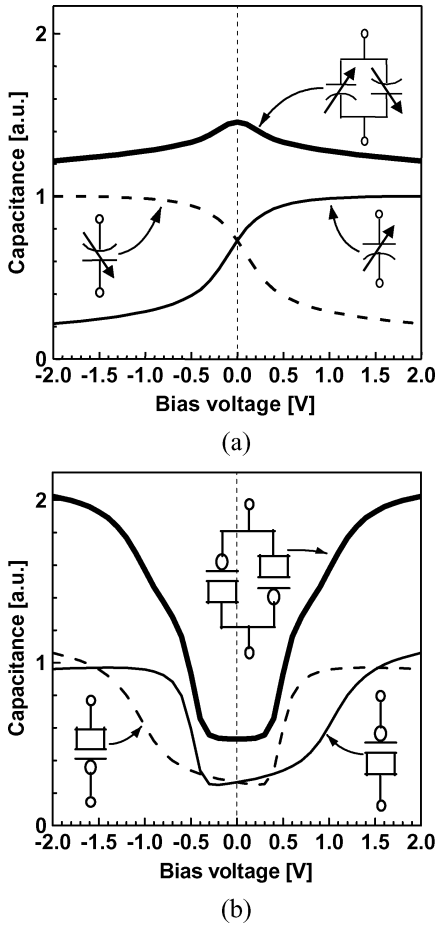


Fig. 3. Measured C–V characteristics. (a) The pair of n-poly gate capacitors. (b) The pair of pMOS gate capacitors.

the data for a single capacitor. The broken lines are the data for a single capacitor where the connection is reversed. The thick lines are the data for the pair of capacitors. The shape of the C–V curve of the single pMOS gate capacitor is different from that of the single n-poly gate capacitor due to its ready access to *both* holes and electrons from n+ and p+ diffusion regions next to the pMOS gate. In contrast, the n-poly gate has ready access *only* to electrons from nearby n+ diffusion regions. As shown in the C–V curve of the single pMOS gate capacitor in Fig. 3(b), an increase of the bias voltage from -2 V to 2 V leads to a capacitance variation from large to small to large as the silicon surface

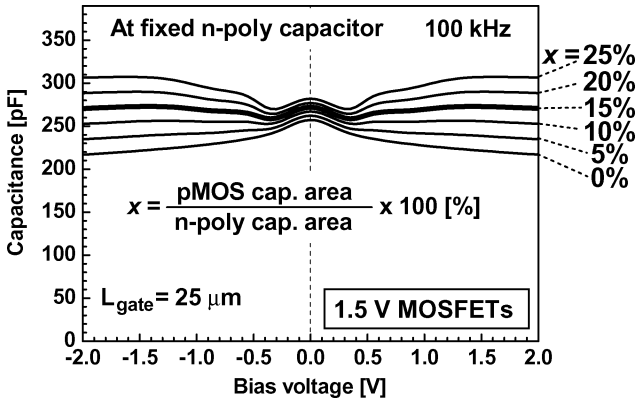


Fig. 4. Measured C–V characteristics of BIGCAP fabricated with a 1.5-V 0.13-μm CMOS for various values of x at a fixed area of the n-poly gate capacitors.

condition under the gate electrode changes from an inversion condition to a depletion condition to an accumulation condition [8]. In contrast, the C–V curve of the single n-poly gate capacitor shown in Fig. 3(a) reveals that the capacitor variation varies from small to large under the same bias conditions as the surface condition changes from the depletion condition to the accumulation condition. As shown in Fig. 3(a), the pair of n-poly gate capacitors shows its maximum capacitance at 0 V, while the pair of pMOS gate capacitors [Fig. 3(b)] shows its minimum capacitance at 0 V. The n-poly and pMOS gate capacitors demonstrate the opposite bias dependence of capacitance. Therefore, by combining them appropriately, the bias dependence of the capacitance of the n-poly and pMOS gate capacitors can be used to cancel each other out and we can achieve a very low dependence of capacitance on bias.

III. Experimental Results of BIGCAP

A. Linearity

Fig. 4 shows the measured C–V characteristics of BIGCAP fabricated with a 1.5-V 0.13-μm CMOS process. The capacitance was measured at 100 kHz with an HP4284A precision LCR meter. The ratio (x) of the pMOS gate capacitors' area to the area of the n-poly gate capacitors was varied by changing the pMOS gate capacitors' area at the fixed area of the n-poly gate capacitors. When x is 0%, BIGCAP uses only the pair of n-poly gate capacitors, which is the same as Fig. 3(a), and it shows its maximum capacitance at 0 V. As x is increased, the C–V curve changes as shown in Fig. 4. When x is 15%, and the curve is the flattest. Fig. 5 shows the dependence of the linearity extracted from Fig. 4 on x. The linearity is defined as the difference between the maximum capacitance and the minimum capacitance normalized by twice the average capacitance from -2 V to 2 V. There is an optimum x to realize good linearity. The best linearity of $\pm 2.9\%$ was achieved when x was 15%. This optimum x value depends on each CMOS process.

In order to investigate the CMOS process dependence of the optimum x value, we studied the optimum x and the best linearity for BIGCAP using two other CMOS processes. In our 1.5-V 0.13-μm CMOS [7], thick-oxide MOSFETs for 2.5-V and 3.3-V I/O are available. Fig. 6(a) and (b) show the C–V

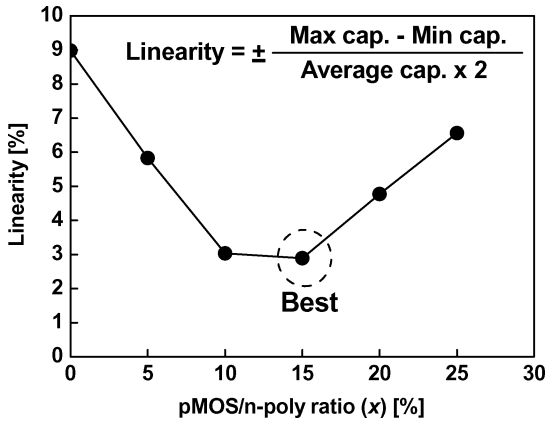
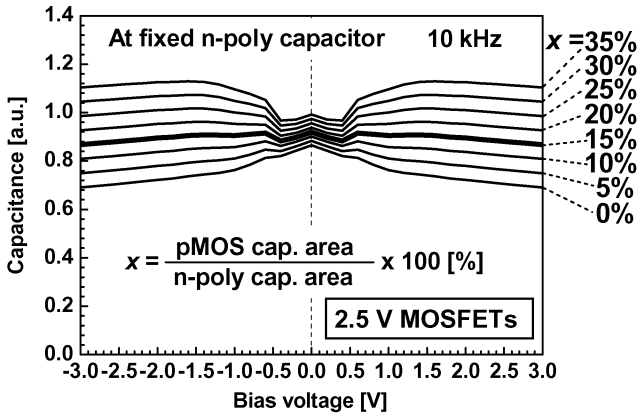
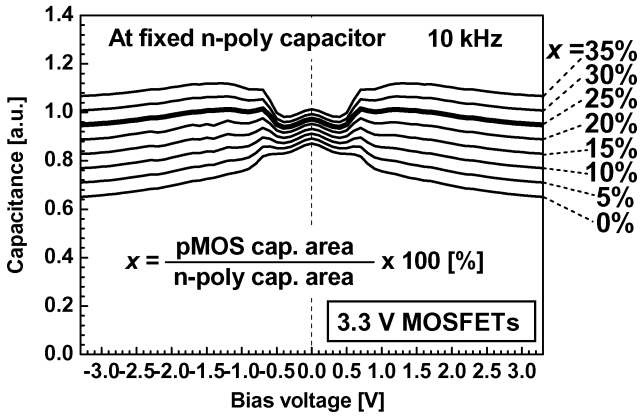


Fig. 5. Dependence of the linearity on x extracted from Fig. 4.



(a)



(b)

Fig. 6. C–V characteristics of BIGCAP using thick-oxide MOSFETs for various values of x at a fixed area of the n-poly gate capacitors. (a) 2.5-V MOSFETs. (b) 3.3-V MOSFETs.

characteristics of BIGCAP using 2.5-V and 3.3-V thick-oxide MOSFETs, respectively. x was varied by changing the pMOS gate capacitors' area while the n-poly gate capacitors' area remained fixed. The capacitance of the 200-μm^2 pMOS gate capacitors and the 200-μm^2 n-poly gate capacitors was measured separately at 10 kHz, and the capacitance of BIGCAP was calculated by combining the measured results. Fig. 7 shows the dependence of the linearity extracted from Fig. 6 on x. The data of BIGCAP using 1.5-V thin-oxide MOSFETs in Fig. 5 are also

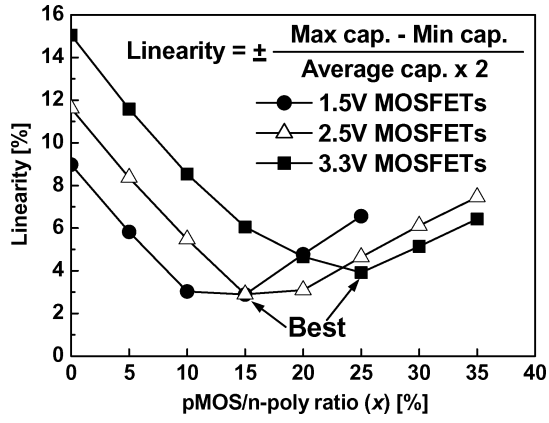


Fig. 7. Dependence of the linearity on x extracted from Fig. 6. The data in Fig. 5 are also included.

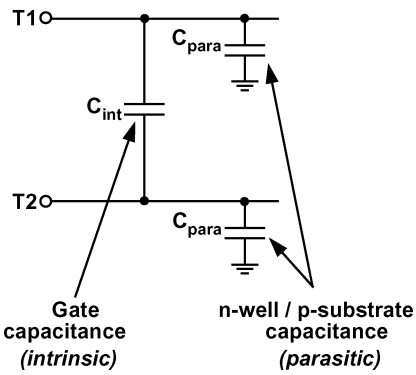


Fig. 8. Equivalent circuit of BIGCAP.

included in Fig. 7. For 2.5-V MOSFETs, the best linearity of $\pm 2.9\%$ was achieved, when x was 15%, which is the same as 1.5-V MOSFETs. For 3.3-V MOSFETs, the best linearity of $\pm 3.9\%$ was achieved, when x was 25%. Therefore, BIGCAP achieves better than $\pm 4\%$ with an optimum x in the range of 15%–25% for each of the three 0.13-μm CMOS process variations considered.

B. Parasitic Capacitance

Fig. 8 shows an equivalent circuit of BIGCAP. The intrinsic capacitance $(C_{\rm int})$ is gate capacitance, and the parasitic capacitance $(C_{\rm para})$ is the capacitance between the n-well and p-substrate. When x was 15%, $C_{\rm int}$ of BIGCAP using 1.5-V thin-oxide MOSFETs was 6.7 fF/μm^2, which is 70% of the gate capacitance of 9.6 fF/μm^2 at inversion. Fig. 9 shows the measured dependence of $C_{\rm para}$ of BIGCAP on the terminal voltage, when x was 15%. The terminal voltage is a voltage between T1 (or T2) shown in Fig. 8 and the ground. The measured sample was the same as that used in Fig. 4. As the terminal voltage increases, $C_{\rm para}$ decreases because the parasitic capacitance is a reverse-biased p-n junction. The measured $C_{\rm para}$ was as small as $1.9\% + 0.5\%/-0.3\%$ of $C_{\rm int}$.

Fig. 10(a) shows the calculated dependence of the relative parasitic capacitance $(C_{\rm rel-para})$ on $C_{\rm int}$ for various gate lengths $(L_{\rm gate})$. Here, $C_{\rm rel-para}$ is $C_{\rm para}$ over $C_{\rm int}$ in percentage. A measured data point at length equal to 25 μm is shown on the same plot. Fig. 10(b) and (1)–(3) show the

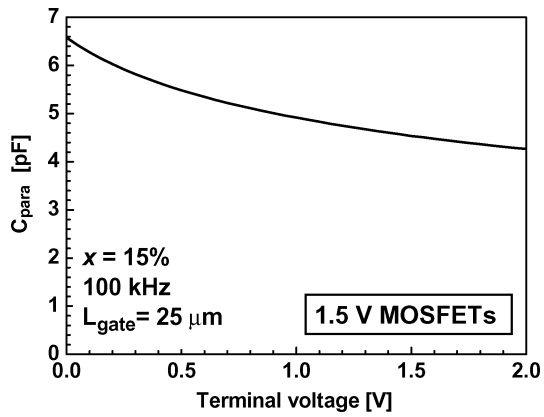


Fig. 9. Measured dependence of the parasitic capacitance of BIGCAP on the terminal voltage, when x was 15%. The measured sample was the same as that used in Fig. 4.

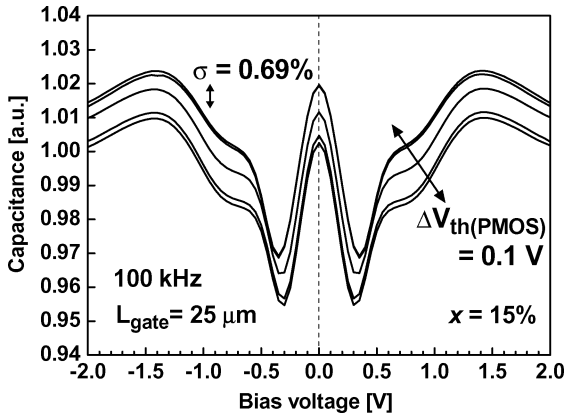


Fig. 11. Measured C–V characteristics of BIGCAP for various pMOS threshold voltages.

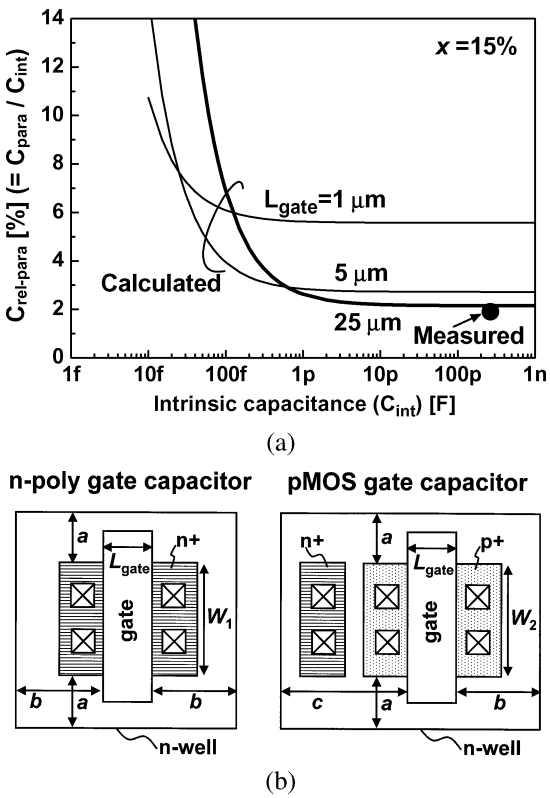


Fig. 10. (a) Calculated dependence of the relative parasitic capacitance on the intrinsic capacitance. (b) Layout of BIGCAP.

layout of BIGCAP and equations used to calculate Fig. 10(a), respectively.

$$W_2 = 0.15 \times W_1 \tag{1}$$

$$C_{\rm int} = L_{\rm gate} \times (W_1 + W_2) \times C_{\rm gate} \tag{2}$$

$$C_{\rm para} = \{(L_{\rm gate} + 2b)(W_1 + 2a) + (L_{\rm gate} + b + c)(W_2 + 2a)\} \times C_{\rm nwell} \tag{3}$$

where W_1 (μm) and W_2 (μm) are the gate width of n-poly gate capacitors and pMOS gate capacitors, respectively, a (μm), b (μm), and c (μm) are the minimum spacing determined by the design rule, $C_{\rm gate}$ (fF/μm^2) is the gate capacitance, and $C_{\rm nwell}$ (fF/μm^2) is the capacitance between the n-well and p-substrate. In (3), the sidewall capacitance of the n-well is neglected so that only the bottom capacitance of the n-well is considered. In Fig. 10(a), $C_{\rm int}$ is varied by changing W_1 and W_2. A long $L_{\rm gate}$ achieves the smallest $C_{\rm rel-para}$ for a *large*, fixed $C_{\rm int}$ because the relative diffusion area resulting from a long $L_{\rm gate}$ is smaller than that with a short $L_{\rm gate}$. In contrast, a short $L_{\rm gate}$ achieves the smallest $C_{\rm rel-para}$ for a *small*, fixed $C_{\rm int}$ because the relative area of a long and narrow n-well (corresponding to a long $L_{\rm gate}$) is larger than the relative area of a square n-well (corresponding to a short $L_{\rm gate}$). These results indicate that there is an optimum $L_{\rm gate}$ to achieve the smallest $C_{\rm rel-para}$ for a given $C_{\rm int}$ When $C_{\rm int}$ is larger than 100 fF, less than 4% $C_{\rm rel-para}$ is achievable.

C. Capacitance Variation

To investigate the capacitance variation, the capacitance value of BIGCAP when x is 15% in Fig. 4 was measured for nine spots across an 8-inch wafer. The average capacitance was 266.6 pF, and the maximum and minimum capacitance was $+0.21\%$ and -0.22% of the average capacitance, respectively. The standard deviation was as small as 0.096% of the average capacitance, which is much smaller than the 1.5% reported in [9] because the capacitance of BIGCAP is determined by the gate-oxide thickness, unlike the inter-layer dielectrics (ILD) thickness in [9]. Commonly, the gate oxide is made by thermally oxidizing the silicon substrate, while the ILD is made by a deposition process such as a chemical vapor deposition (CVD). Therefore, the thickness variation of the gate oxide is much smaller than that of the ILD.

To investigate the process sensitivity, the threshold voltage of MOSFETs was varied. Fig. 11 shows the measured C–V of BIGCAP for different pMOS threshold voltages. The threshold voltage was varied by changing the channel doping concentration of five wafers. For a 0.1-V threshold voltage variation, the capacitance variation was only $\sigma = 0.69\%$ and the linearity ranged from $\pm 2.84\%$ to $\pm 2.93\%$. The parasitic capacitance ($C_{\rm para}$) variation of five samples in Fig. 11 was also measured, and it was $\sigma = 1.0\%$.

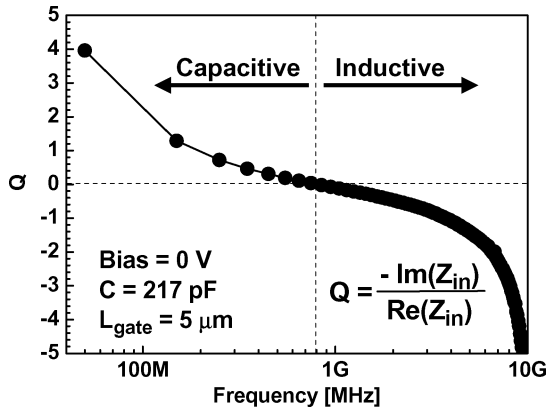


Fig. 12. Measured dependence of the quality factor (Q) of BIGCAP on frequency.

TABLE I
PERFORMANCE SUMMARY

	MIM	Conv. MOS gate	BIGCAP
Linearity	0.01 %	60 %	2.9 %
Capacitance	1 fF/μm^2	9.6 fF/μm^2	6.7 fF/μm^2
Extra process	Yes	No	No
Parasitic capacitance	10 %	1.9 % (+0.5% / –0.3%)	1.9 % (+0.5% / –0.3%)
Variations	10 %	< 1 %	< 1 %

D. Quality Factor

Fig. 12 shows the dependence of the quality factor (Q) of BIGCAP on frequency as measured with an HP8510C vector network analyzer. The Q is defined in the inset. The gate length of BIGCAP is 5 μm. Positive Q means that BIGCAP is capacitive, while negative Q means that BIGCAP is inductive. BIGCAP was capacitive below 800 MHz, while BIGCAP was inductive above 800 MHz due to the parasitic inductance of the test structures. The resonant frequency was as low as 800 MHz because the capacitance of BIGCAP was as much as 217 pF. Therefore, we could not obtain the positive Q at the frequency over 800 MHz with our test structures.

However, BIGCAP has the potential for high Q comparable to MIM capacitors by a careful layout optimization. For example, for accumulation MOS varactors, which are often used in RF applications and are the same as the n-poly gate capacitors in BIGCAP, peak Q of 120 and 56 have been reported at 2.4 and 5 GHz, respectively [10], while MIM capacitors have Q of 166 and 63 at 2.4 and 5 GHz, respectively [10].

E. Performance Summary

Table I summarizes the performance of our proposed BIGCAP using 1.5-V thin-oxide MOSFETs and compares it with conventional MIM and MOS gate capacitors. The linearity of BIGCAP is 1/20 that of conventional gate capacitors. The capacitance of BIGCAP is 6.7 times larger than that of MIM capacitors and 70% that of conventional gate capacitors. BIGCAP needs no extra process steps. The parasitic capacitance and variations of BIGCAP are the same as those of conventional gate capacitors. The parasitic capacitance of BIGCAP is less than 1/5 that of MIM capacitors. The capacitance variations in BIGCAP are less than 1/10 that of MIM capacitors, because the variation in the gate-oxide thickness is smaller than that in the MIM insulator thickness. Therefore, we see that BIGCAP offers significant advantages over both MIM and MOS gate capacitors with regards to simultaneously achieving high capacitive density, good linearity, and low variation.

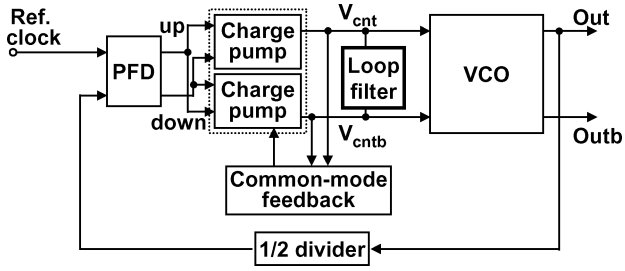


Fig. 13. Block diagram of a fabricated differential PLL.

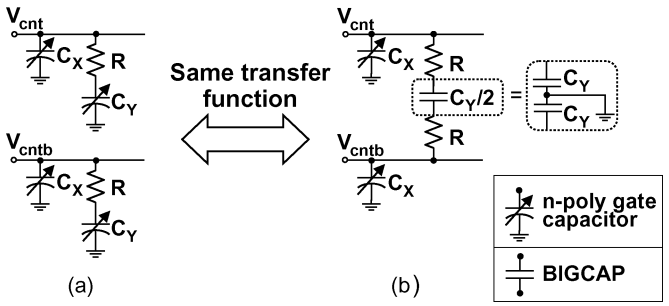


Fig. 14. Configuration of the loop filter of the differential PLL. (a) Conventional configuration. (b) Proposed configuration. BIGCAP was used for $C_{\rm Y}$ in (b), and n-poly gate capacitors were used for the other capacitances.

IV. Application of BIGCAP to the Loop Filter of a Differential PLL

In this section, we discuss the application of BIGCAP to the loop filter of a differential PLL, and achieved normal PLL operation at small area.

Differential PLLs [11]–[16] that have differential control voltages have often been used to avoid the jitter increase created by the power supply noise. Fig. 13 shows a block diagram of a fabricated differential PLL. Two outputs ($V_{\rm cnt}$, $V_{\rm cntb}$) of the two charge pump circuits are differential control voltages of ring-oscillator-type VCO. When one of the differential control voltages increases, the other decreases. The loop filter (LF) is connected between $V_{\rm cnt}$ and $V_{\rm cntb}$. The common-mode feedback circuit sets the common-mode of the differential control voltages.

Here, we discuss the LF configuration and the capacitance of the LF in a differential PLL. Fig. 14(a) shows the conventional configuration of the LF of a differential PLL, and Fig. 14(b) shows our proposed configuration. Both the loop filters have the same transfer function. The conventional LF in Fig. 14(a) requires twice as much capacitance as the LF of a single-ended PLL. Therefore, the PLL area is nearly twice as large, because it is generally determined by the large capacitance of LF which is shown as $C_{\rm Y}$ in Fig. 14. If the capacitor used in the LF is bias-independent, $C_{\rm Y}$ can be inserted between $V_{\rm cnt}$ and $V_{\rm cntb}$

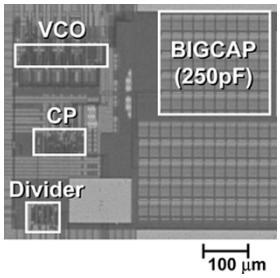


Fig. 15. Microphotograph of the fabricated PLL with the proposed loop filter shown in Fig. 14(b).

as shown in Fig. 14(b). In this case, the capacitance needed to achieve the same transfer function as in Fig. 14(a) is only $C_{\rm Y}/2$, which is 1/4 the size of that in Fig. 14(a) and half the size of that of the single-ended PLL. However, a conventional n-poly gate capacitor, which is widely used in LF, cannot be inserted between $V_{\rm cnt}$ and $V_{\rm cntb}$, because the capacitance of the n-poly gate capacitor changes 60% depending on the bias voltage as shown in Fig. 3(a) and Table I, the transfer function of the PLL changes, and the jitter will increase. It has been reported that the proposed LF in Fig. 14(b) can be made by using a bias-independent poly-to-poly capacitor [14]. However, the area of the PLL is very large, because the capacitance density of the poly-to-poly capacitor is about 1/10 that of the n-poly gate capacitor. To solve this problem, BIGCAP is applied to $C_{\rm Y}$ in Fig. 14(b). BIGCAP is adequately linear for the given PLL application, because the 2.9% capacitance variation depending on the bias voltage as shown in Figs. 4 and 5 is smaller than the typical 20% or more VCO gain variation across the full VCO range and the variation of the transfer function of the PLL due to the nonlinearity of BIGCAP is negligible.

A PLL with the proposed LF in Fig. 14(b) was fabricated using a 1.5-V 0.13-μm CMOS to demonstrate a PLL operation with BIGCAP. Fig. 15 shows a microphotograph of the fabricated PLL. BIGCAP was used for $C_{\rm Y}$, and the n-poly gate capacitor was used for C_X in Fig. 14(b). Parameters of the fabricated LF were $C_X = 5$ pF, R $= 0.5$ kΩ, and $C_{\rm Y}/2 = 250$ pF. As shown in Fig. 16, the measured jitter of the PLL with the proposed LF at 840 MHz was 7.0 ps (rms) and 74.4 ps (peak-to-peak) for a 1.5-V supply. The jitter is larger than the previously reported jitter such as 3.3 ps (rms) and 29 ps (peak-to-peak) at 1 GHz for a 2.5-V supply [17]. We guess that the large jitter is caused not by BIGCAP but by the VCO and the charge pump. Table II compares the gate area of the MOS capacitor for the conventional and proposed LFs shown in Fig. 14. The area of the proposed LF with BIGCAP is only 35% $(= 0.5 \times 0.70)$ of that of the conventional LF without BIGCAP. It is 70% of that of a single-ended PLL. Therefore, by applying the BIGCAP to the LF, we can avoid an increase in PLL area when changing from the single-ended design to the differential design.

V. Conclusion

The proposed BIGCAP showed good linearity of $\pm 2.9\%$, large capacitance of 6.7 fF/μm^2, and as low as 1.9% relative

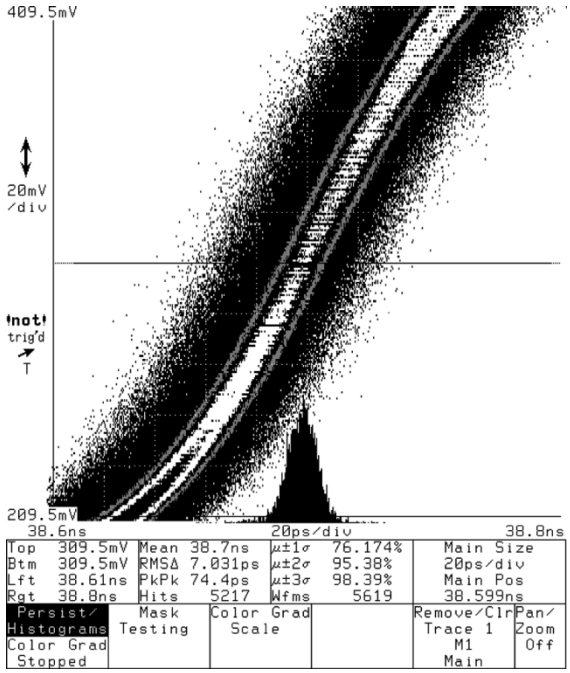


Fig. 16. Measured jitter of the PLL with the proposed loop filter. The jitter at 840 MHz was 7.0 ps (rms) and 74.4 ps (peak-to-peak) for a 1.5-V supply.

TABLE II
Gate Area of MOS Capacitor for the Loop Filter for the Different Loop Filters Shown in Fig. 13

Conventional LF w/o BIGCAP	Proposed LF with BIGCAP
0.104 mm^2 (100%)	0.0373 mm^2 (35%)

parasitic capacitance without any additional fabrication processes on 1.5-V 0.13-μm standard digital CMOS technology. Capacitance variation across a wafer was as small as $\sigma = 0.096\%$. For a 0.1-V threshold voltage variation, the capacitance variation was only $\sigma = 0.69\%$ and the linearity ranged from $\pm 2.84\%$ to $\pm 2.93\%$. In order to investigate the CMOS process dependence of the optimum x value, we studied the optimum x and the best linearity for BIGCAP in three variations of the 0.13-μm CMOS process. For 2.5-V MOSFETs, the best linearity of $\pm 2.9\%$ was achieved, when x was 15%, which is the same as 1.5-V MOSFETs. For 3.3-V MOSFETs, the best linearity of $\pm 3.9\%$ was achieved, when x was 25%.

By applying BIGCAP to the loop filter of a differential PLL, we reduced the gate area of the MOS capacitor for the loop filter to only 35% of that of the conventional design without degrading the performance of the PLL. BIGCAP is adequately linear for the given PLL application, because the 2.9% capacitance variation depending on the bias voltage as shown in Figs. 4 and 5 is smaller than the typical 20% or more VCO gain variation across the full VCO range and the variation of the transfer function of the PLL due to the nonlinearity of BIGCAP is negligible. BIGCAP is widely applicable to many other circuits such as I/O buffers, switched-capacitor circuits, operational amplifiers, data converters, and mixers.

ACKNOWLEDGMENT

The authors would like to thank Y. Hamada and T. Enomoto for providing the chip layout, and M. Yamashina, N. Nishi, S. Ohya, and M. Fukuma for their useful comments and advice during the course of this work.

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