Control of threshold voltage of organic field-effect transistors with double-gate structures

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(Received 11 March 2005; accepted 15 June 2005; published online 8 July 2005)

We fabricated pentacene field-effect transistors with planar-type double-gate structures, where the top- and bottom-gate electrodes can independently apply voltage biases to channel layers. The threshold voltage of organic transistors is changed systematically in a wide range from −16 to −43 V when the voltage bias of the top-gate electrode is changed from 0 to +60 V. The mobility in the linear regime is almost constant (0.2 $cm^2/V\,s$) at various voltage biases of the top-gate electrode and the on/off ratio is 10^6. © *2005 American Institute of Physics*.
[DOI: 10.1063/1.1995958]

Organic field-effect transistors (FETs) have attracted much attention owing to their excellent properties for realizing flexible, large-area electronic devices. Organic-transistor integrated circuits (ICs) for driving paper-like displays[1,2] and large-area sensors[3,4] have been manufactured. Although much progress in organic transistors has been made in the last decade, one of the major remaining issues on organic transistor ICs is the control of their threshold voltage (V_{th}), which is crucial to the design and manufacture of complicated ICs. Silicon metal-oxide-semiconductor FETs, which are mainstream electronic devices, can control V_{th} by changing the doping level of semiconductors and/or by applying voltage bias to conductive substrates.[5,6] However, base films for organic transistors are usually made of nonconductive plastic.[3] Although there are some pioneering works in which V_{th} of organic transistors is changed by doping organic semiconductors[7] and/or by modifying the surface of gate dielectric layers,[8,9] such approaches are still far from practical use due to the reliability of the manufacturing process and/or the distribution of the performance of organic transistors.

In this work, we manufactured pentacene FETs with planar-type double-gate structures on plastic films. In these FETs, pentacene channel layers are sandwiched between polyimide and parylene gate dielectric layers, and the top- and bottom-gate electrodes can independently apply voltage biases to channel layers. V_{th} is systematically decreased from −16 to −43 V when top-gate bias is changed from 0 to +60 V. The mobility in the linear regime is 0.2 $cm^2/V\,s$ and shows no significant changes at various V_{top} biases.

Pentacene FETs with double-gate structures were fabricated on plastic films. The cross-sectional structure of the FETs is schematically shown in Fig. 1(a). First, a bottom-gate electrode consisting of 5-nm-thick Cr and 50-nm-thick Au layers is deposited in a vacuum evaporator on a 75 μm thick polyimide film. Polyimide precursors (Kemitite CT4112, Kyocera Chemical) are then spin-coated and cured at 180 °C to form 620-nm-thick gate dielectric layers.[3,10] A 50 nm thick pentacene film is deposited in the same vacuum evaporator. 50-nm-thick Au drain (D) and source (S) electrodes are evaporated through a shadow mask. The channel length (L) and width (W) of the pentacene FETs are 100 μm and 1 mm, respectively. The base film with transistors is then uniformly coated with a 600 nm thick parylene layer. Finally, a 150 nm thick Au layer is deposited to form top-gate electrodes.[11] Figure 1(b) shows a micrograph of the fabricated FETs. In addition to functionality of the gate dielectric layer, the parylene layer has functionality as a passivation layer, which prevents organic semiconductors from being directly exposed to ambient air. As shown in Figs. 1(a) and 1(b), both source-drain electrodes and channels are completely covered by a 300×1000 μm^2 top-gate electrode.

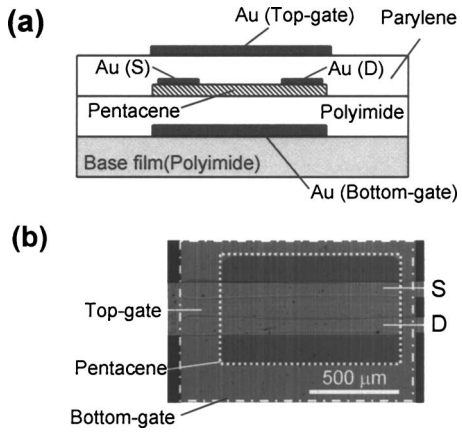

FIG. 1. (a) The cross-sectional illustration of organic transistors on plastic films with double-gate structures. (b) A micrograph of the fabricated FETs. The dashed-line represents the area of pentacene, while the dash-dotted line represents the bottom-gate electrode.

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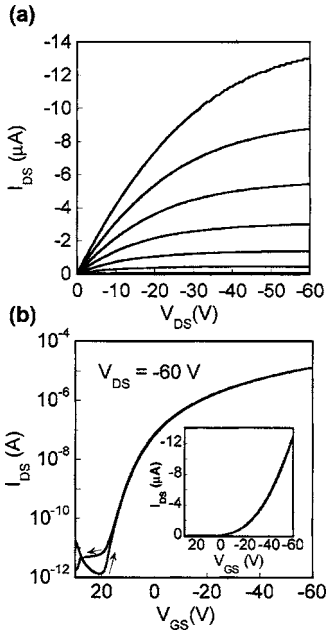

FIG. 2. Typical dc characteristics of the present transistors with double-gate structures, where the top-gate bias V_{top} is floating. (a) The source-drain current (I_{DS}) is measured under ambient environment as a function of source-drain voltage (V_{DS}). Bottom-gate voltage (V_{GS}) is changed from 0 to −60 V in −10 V steps. (b) The corresponding transfer curve of the same FET: V_{GS} is swept from +30 to −60 V with the application of V_{DS} =−60 V, while the top-gate is floating. The inset is the same trace in the linear scale.

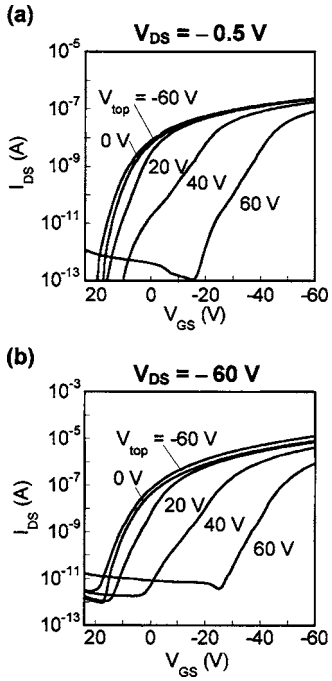

FIG. 3. The transfer characteristics of the present transistors with double-gate structures are measured with the application of (a) V_{DS}=−0.5 V in the linear regimes and (b) −60 V in the saturation regimes, while the top-gate bias (V_{top}) is varied from −60 to +60 V.

To accurately evaluate the capacitances of the top- and bottom-gate dielectric layers, we also prepared capacitor structures on the same base films. The capacitances of the bottom-gate dielectric layer of polyimide (C_{bottom}) and the top-gate dielectric layer of parylene (C_{top}) are 5.4 and 4.5 nF/cm^2, respectively, which are consistent with the relative permittivities of polyimide and parylene provided by the manufacturers, namely, 3.8 and 3.1, respectively.

The current-voltage characteristics of the organic transistors are measured with a precision semiconductor parameter analyzer (4156C, Agilent Technologies). Figure 2(a) shows the typical dc characteristics obtained when the top-gate electrode is in the floating state, hereafter referred to as "floating." Here, we monitor the source-drain current (I_{DS}) of pentacene transistors as a function of source-drain voltage (V_{DS}). Bottom-gate voltage (V_{GS}) is changed from 0 to −60 V in −10 V steps. Figure 2(b) shows a transfer curve of the FET: V_{GS} is swept from +30 to −60 V with the application of V_{DS}=−60 V, while the top-gate electrode is floating. The evaluated mobility is 0.2 cm^2/V s in the linear regime and the on/off ratio is 10^7.

The FETs are functional when voltage bias is applied to the top-gate electrode and the, bottom-gate electrode is floating. /The mobility is only 10^{-4} cm^2/V s, although the channels are produced in the same pentacene layer. In the above operation mode, note that channel formation occurs at the interface of the bottom surface of parylene and the top surface of pentacene. This interface should be very rough since the surface morphology of pentacene shows leaf vein like structures.[12] The leakage current through parylene gate dielectric layers is only 5 pA even at −60 V, demonstrating a good reliability of parylene layers as insulators.

We measure the transfer characteristics of the present FETs with double-gate structures in both the linear and saturation regimes at various voltage biases of the top gate (V_{top}) from −60 V to +60 V. Figures 3(a) and 3(b) show the transfer curves obtained with the application of V_{DS}=−0.5 V (linear regime) and −60 V (saturation regime), respectively. When V_{top} is swept from −60 V to +60 V, the transfer curves systematically shift from left to right along the horizontal axis, or to the negative gate-source voltage (V_{GS}). In particular, the shift is large when V_{top} is greater than +20 V, while it is very small when V_{top} is less than +20 V. Saturation current is systematically decreased by increasing V_{top}. In contrast, minimum (off) current is slightly increased when V_{top} is varied from −60 to +60 V, which is mainly due to the leakage current through parylene gate dielectric layers.

We plot in Fig. 4 mobility in the linear regime and V_{th} as functions of the top-gate bias V_{top}. As shown in Fig. 4, the change in V_{th} is very small when V_{top} is varied from −60 V to+20 V, but V_{th} markedly decreases from −17 to −43 V when V_{top} is varied from +20 to+60 V. Such a large

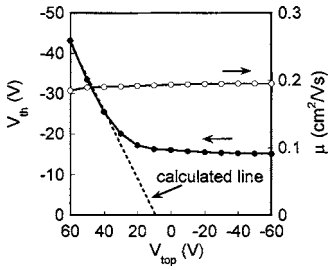

FIG. 4. The threshold voltage (V_{th}) and mobility (μ) evaluated in the linear regime with double-gate structures as a function of top-gate bias V_{top}. The dashed line represents the calculated slope (0.83), or the capacitance of parylene (4.5 nF/cm^2) divided by that of polyimide (5.4 nF/cm^2), which is consistent with the measured slope, $\Delta V_{th}/\Delta V_{top}$ (0.85).

and systematic change in V_{th} has not been achieved in organic transistors so far by other methods.[7–9] In contrast, chemical doping and other approaches can control V_{th} in silicon FETs more conveniently and efficiently,[5,6,13] although double-gate structures are known to change V_{th} in silicon FETs.[14,15] In the case of silicon transistors with double-gate structures, the change in V_{th} can be understood well by a simple analysis of electrostatic potential:[13] $\Delta V_{th}/\Delta V_{top} = C_x/C_1$, $1/C_x = 1/C_2 + /C_3$, where C_1, C_2, and C_3 are the capacitances of the bottom-gate dielectric (polyimide in organic FET), channel semiconductor (pentacene), and top-gate dielectric (parylene), respectively. The slope $(\Delta V_{th}/\Delta V_{top})$ of the present organic transistor in Fig. 4 is 0.85, which is in excellent agreement with $C_x/C_1 \sim 0.83$ culated without taking C_2 into account since the organic semiconductor is much thinner than the parylene layer. Thus, we conclude that the change in V_{th} of organic transistors is well explained by the change in electrostatic potential, similarly to that of silicon FETs. Note that, in organic transistors, pentacene under a positive bias behaves like an insulator rather than a *n*-type semiconductor, because electrons are not induced at the interfaces of polycrystalline pentacene under a positive bias. As a result, a positive bias directly changes electrostatic potential without shielding, and carrier concentration at the channel layer decreases drastically.

It is very interesting to note in Fig. 4 that mobility does not depend on V_{top}, but is maintained at 0.2 cm^2/V s. This suggests that mobility in the linear regime does not depend on the magnitude of electric field in the vertical direction.

Since the top-gate electrode of the present FETs covers channel layers as well as source and drain electrodes, one of the major concerns is that the top-gate electrodes may also have a large influence on the physical properties of the FETs near the source and drain contact regions. Thus, we prepared a control FET in which the top-gate electrodes cover only 80 μm of the 100 μm long channel and no overlap between the top-gate electrodes and source-drain electrodes exists.[16] No significant differences were found between those two FETs, indicating that top-gate bias mainly affects the channel part rather than the source-drain electrode part.

In summary, we controlled the threshold voltage (V_{th}) of organic FETs by employing novel planar-type double-gate structures. V_{th} changes systematically in a wide range from -16 to -43 V with the application of voltage bias on the top-gate electrode, while mobility (0.2 cm^2/V s) in the linear regime shows no significant changes at various V_{top} biases and the on/off ratio is 10^6. The control of V_{th} enables the optimization of high-speed operation and low-power dissipation of integrated circuits, both of which give rise to a trade-off. Therefore, the present double-gate structures will open up a possibility of realizing sophisticated integrated circuits with organic transistors.

We thank Prof. T. Hiramoto for fruitful discussions. We also thank Kyocera Chemical Cooperation for providing high-purity polyimide precursors and Daisan Kasei for providing high-purity parylene. This study is partially supported by the IT Program, MEXT, MPHPT, and NEDO.

Note added to the proof. Recent conference presentations by Gelinck *et al.*[17] and Li *et al.*[18] report a similar effect.

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