

Chip-to-Chip Inductive Wireless Power Transmission System for SiP Applications

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Abstract— A chip-to-chip inductive wireless power transmission system is proposed and the feasibility is experimentally demonstrated for the first time. The circuit realized 2.5mW power transmission at the output DC voltage of 0.5V using 700x700 μ m on-chip planar inductors for the transmitter and the receiver. Methods to optimize the circuit design about the maximum transmission power and the simulated optimization results are discussed.

I. INTRODUCTION

A System-in-a-Package (SiP) is getting a major 3D integration approach in recent years. For data communication among stacked chips in SiP's, wireless data transmission technologies have been investigated for high speed, low power and low cost [1][2]. Power delivery in these systems, however, is not wireless and is based on bonding. Then, it is difficult to get two stacked chips close, since the bonding needs several hundred microns separation between chips. One solution is to skew the stacked chips but this is difficult if the upper chip should be connected in the middle of the lower chip and is covered by the topmost chip.

If the power is supplied wirelessly, the chips can be stacked closely and the wireless data transmission performance will

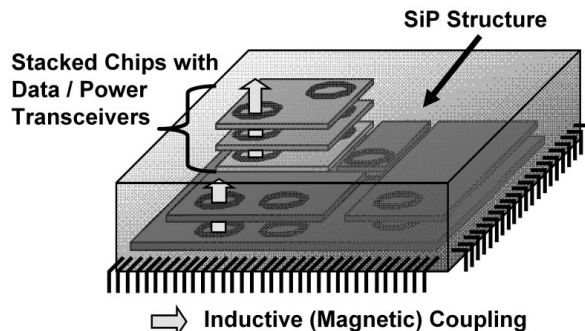


Fig. 1. Concept of chip-to-chip wireless power transmission.

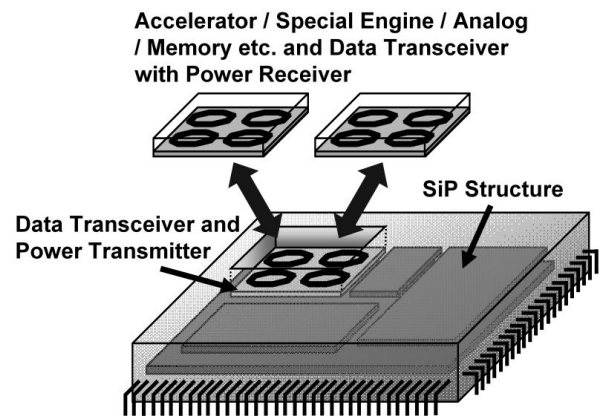


Fig. 2. Concept of system modification after fabrication of SiP's/SoC's.

be increased, since the data bandwidth and communication reliability increases as the chip-to-chip distance is decreased in wireless data communication. The cost is also decreased due to the elimination of mechanical bonding. Furthermore, chip detachability can also be achieved by combining the wireless data and power transmission. This opens up a totally new system customization scheme after the fabrication as we sometimes change a daughter board for system upgrade.

Fig. 1 illustrates a proposed wireless power delivery scheme based on inductive coupling between the lowest chip and upper chips. The shortest inductor-to-inductor distance depends on the thinning of the chip thickness, which is as small as 20 microns. If a face-to-face configuration is possible, the distance is further reduced, which is used in the measurement setup in this paper.

Fig. 2 shows the concept of system customization after the fabrication of an SiP to reduce mask set cost and to increase post-fabrication system modification freedom. Chips like accelerators, special engines, analogs, memories are attached wirelessly on top of the lower base chip. The lower chip embedded in the package has a data transceiver and a "power

transmitter”. The upper chip attached to the package has a data transceiver and a “power receiver”. This system may give users the ability to upgrade the SiP’s like a daughterboard upgrade nowadays. The risk of ESD problem is mitigated because this system eliminates the naked interconnections and metal pads with coils for wireless transmission being covered by passivation layer.

II. CIRCUIT TOPOLOGY

Fig.3 shows the circuit diagram of the proposed system. The lower chip includes a transmitter circuit and an on-chip planar inductor L_1 for magnetic field generation. The transmitter circuit generates an RF signal from the DC supply voltage V_{DD} and activates L_1 . The power is transmitted by magnetic fields rather than radio waves. Fig.4 describes a diagram of the adopted transmitter, where the oscillation frequency f of the ring oscillator is designed to be variable for the experiments. The upper chip includes an on-chip planar inductor L_2 , a full-wave rectifier circuit using MOSFET-based diodes and a smoothing capacitor. Fig.5 shows the circuit diagram of the diode circuit whose two PMOS transistors reduce the undesirable body effect of the main PMOS transistor [3]. k indicates the coupling factor of the inductors.

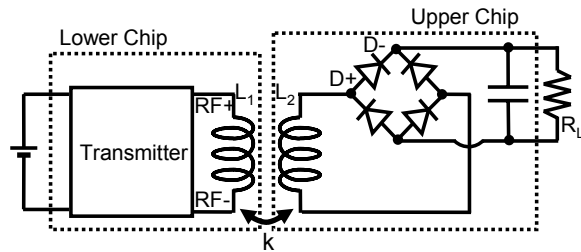


Fig.3. Circuit diagram of proposed system.

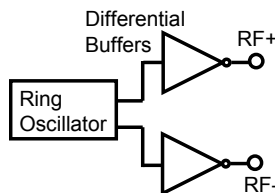


Fig.4. Circuit diagram of transmitter.

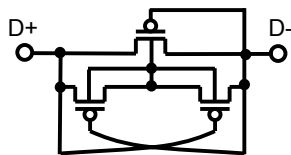


Fig.5. Circuit diagram of PMOS-based diode.

III. SIMULATION AND MEASUREMENT RESULTS

The system shown in Fig.3 was designed in 0.35- μm CMOS and fabricated. Generally, on-chip planar inductors have considerable parasitic capacitive and resistive elements so that the Q factor is not high. Fig.6 shows the simulation model of the planar inductors. R_P and C_P represent the series resistance and the parasitic capacitances of the inductor respectively. The values of R_P and C_P are calculated by approximation formulas and k is derived by Momentum electromagnetic field simulator. The parasitic resistances of buffers, diodes and interconnections were be estimated carefully and minimized in design and layout process.

The outside diameter of the inductor is set to 700x700 μm and k is calculated to be 0.75. RF voltage generated between two terminals of L_2 is set to be twice the nominal V_{DD} when $R_L = \infty$. This RF voltage is better to be higher to reduce the diode voltage loss but it can not surpass twice the tolerant voltage of the PMOS shown in Fig.5. Fig.7 shows microphotographs of the fabricated power transmitter and receiver chips. Fig.8 and 9 show the measurement setup. The lower (upper) chip is mounted on the lower (upper) board and the two chips gets closer together face-to-face.

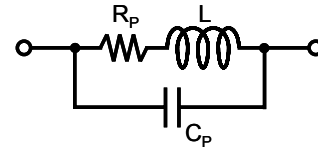


Fig.6. Equivalent circuit of inductor with parasitic elements.

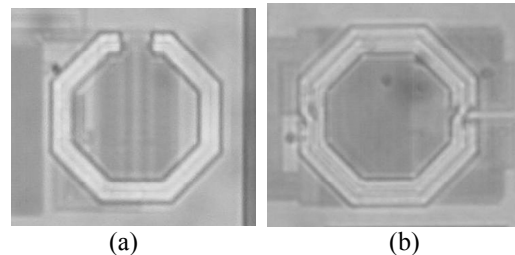


Fig.7. Chip microphotograph of (a) transmitter and (b) receiver.

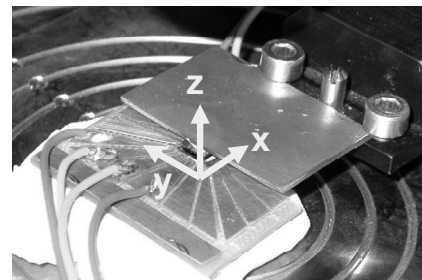


Fig.8. Whole image of measurement setup.

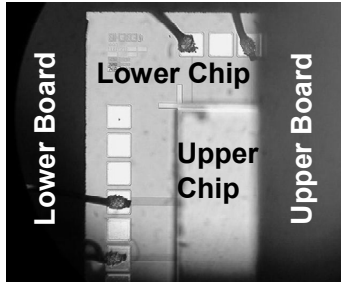


Fig.9. Closeup view of measurement setup.

Fig.10 shows the simulated and measured transmitted power dependence on output DC voltage. HSPICE is used for the simulation. In this implementation, $L_1=1.0\text{nH}$, $L_2=9.3\text{nH}$ and the oscillation frequency is set to $f=330\text{MHz}$ for this graph. Output voltage is varied by changing DC output load R_L . The peak transmitted power is observed when R_L is 100Ω , which is the equivalent source resistance of the wireless power source. The simulated results coincide well with the measured results. Thus the modeling accuracy is considered to be sufficiently high.

Figs. 11, 12 and 13 show the measured output voltage dependence on frequency, Δz (distance between chips) and Δx (misplacement in x direction) and Δy (misplacement in y direction) when the load is open which equals to $R_L=\infty$.

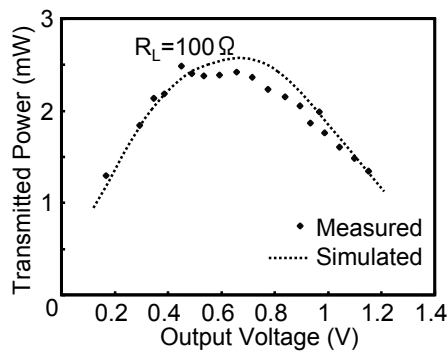


Fig.10. Transmitted power dependence on output voltage.

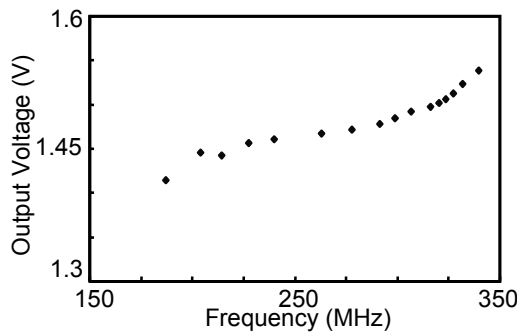


Fig.11. Output voltage dependence on oscillation frequency f .

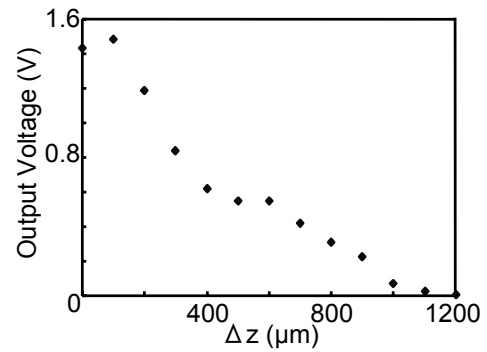


Fig.12. Output voltage dependence on Δz .

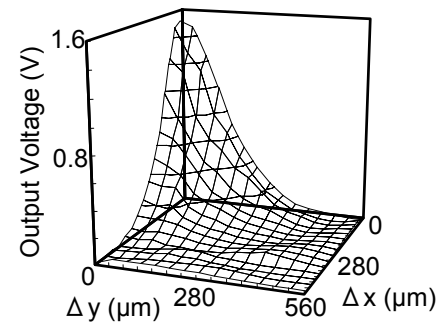


Fig.13. Equivalent circuit of inductor with parasitic elements.

IV. CIRCUIT OPTIMIZATION

Although the feasibility of the wireless power delivery system is demonstrated in the previous sections, it is preferable to increase the transmittable power to further increase the variety of applications. In this section, the methodology for further increasing the transmitted power is described. Improvement can be achieved by adding resonance capacitors C_1 and C_2 as shown in Fig.14. R_S represents parasitic resistances of transmitter

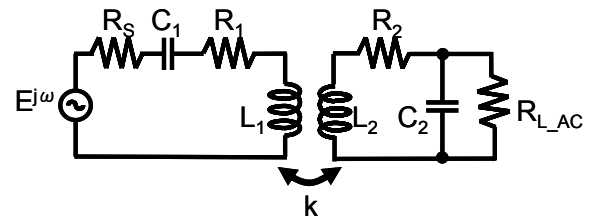


Fig.14. Equivalent circuit of inductor with parasitic elements.

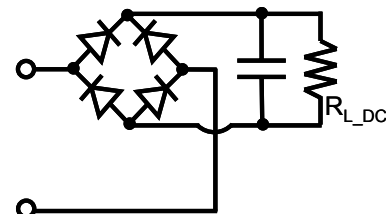


Fig.15. Equivalent circuit of inductor with parasitic elements.

interconnections and driving transistors. R_1 and R_2 indicate series resistances of L_1 and L_2 respectively. Capacitances C_1 and C_2 resonate with L_1 serially and with L_2 in parallel respectively. R_{L_AC} relates to the equivalent total impedance of the rectifier, the smoothing capacitor and the DC load resistance R_{L_DC} as shown in Fig.15. R_{L_AC} was shown to be approximated as follows when the rectifier is ideal and the smoothing capacitor is large enough [4].

$$R_{L_AC} \approx \frac{R_{L_DC}}{2}. \quad (1)$$

Here, we assume the transmitted power is high (if not maximized) when transmitter circuit is in resonance. That is, C_1 is expressed as follows. Although this condition does not give the optimum condition, the resultant transmitted power is at least achievable.

$$C_1 = \frac{I}{4\pi^2 f^2 L_1}. \quad (2)$$

Under this condition, the values of C_2 and R_L expressed as follows maximize the transmitted power, which is exact. Here, $\omega = 2\pi f$.

$$C_2 = \frac{(R_1 + R_s)^2 L_2}{((R_1 + R_s)R_2 + \omega^2 k^2 L_1 L_2)^2 + \omega^2 (R_1 + R_s)^2 L_2^2}. \quad (3)$$

$$R_{L_AC} = \frac{(R_1 + R_s)R_2 + \omega^2 k^2 L_1 L_2}{(R_1 + R_s)(1 - \omega^2 C_2 L_2)}. \quad (4)$$

It is to be noted that this C_2 is independent from R_L , which is nice. Then, the available transmitted power is expressed as:

$$P_{Max_AC} = \frac{E^2 \omega^2 k^2 L_1 L_2}{8[\omega^2 k^2 L_1 L_2 + R_2(R_1 + R_s)](R_1 + R_s)}. \quad (5)$$

The output AC voltage V_{OUT_AC} of the load resistance R_{L_AC} is

$$V_{OUT_AC} = \sqrt{2P_{MAX} R_{L_AC}}. \quad (6)$$

L_2 is determined so that V_{OUT_AC} equals to twice the V_{DD} as is mentioned in section III. For the on-chip planar inductors, the relationship between R_N and L_N is approximated as follows with ζ being a technology parameter.

$$R_N \approx \zeta L_N. \quad (7)$$

P_{MAX_AC} is simplified as follows using (7) and the approximation of $R_s=0$.

$$P_{Max_AC} \approx \frac{E^2 \omega^2 k^2}{8\zeta L_1 (\zeta^2 + \omega^2 k^2)}. \quad (8)$$

The value of L_1 (or the outside diameter of L_1) and k have strong independence thus the maximum power and the value of L_1 is determined by the trade-off.

After all, the capacitances of the resonant capacitors are calculated to be $C_1=281\text{pF}$, $C_2=15\text{pF}$. When these capacitors are added to the original circuit configuration, the

Table I. Power breakdown of R_1 , R_2 and R_L .

	R_1	R_2	R_L
Power(%)	27.3	43.6	29.1

transmitted power is increased to 21.6mW with output DC voltage of 1.8V by simulation, which should be compared with 2.5mW without the resonant capacitors.

The improvement of the rectifier circuit is also effective and simulation shows that the transmitted power is further increased to 35mW if the new rectifying circuit proposed in [5] is employed. Under this condition, power breakdown consumed by R_1 , R_2 , R_L is calculated as shown in Table I. If the area allowed for the wireless power delivery system can be increased to 2.1mm square, 9 parallel power transceivers each of which has $700 \times 700 \mu\text{m}$ in diameter can be implemented and then more than 300mW power transmission is considered to be possible.

V. CONCLUSIONS

In summary, a chip-to-chip 2.5mW wireless power transmission system was proposed and demonstrated by 0.35- μm CMOS technology. A possible increase to 300mW power transmission is also discussed by introducing resonant capacitors.

ACKNOWLEDGMENT

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