

15.4 An Organic FET SRAM for Braille Sheet Display with Back Gate to Increase Static Noise Margin

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Flexible and low-cost organic FETs (OFETs) are suitable for large-area applications. An integrated system of OFETs and pressure sensors was reported in [1], and that of OFETs and photodetector was reported in [2]. In this paper, an integrated system of OFETs and plastic actuators is proposed, and a Braille sheet display is demonstrated. Device and process technology of the OFETs and the actuators are shown in [3]. This paper presents a newly developed back-gated OFETs SRAM and the circuits technology for the Braille sheet display to enhance speed, yield and life time, which will be essential for future large-area electronics made with OFETs. The transition time of the actuator is about 1s. The Braille sheet display has an actuator array. When the actuator is sequentially driven, it takes more than 1 minute to change the Braille, which is impractical. The OFETs also have several problems. Manufacturing variation within a plastic film for the OFETs is large, which is inherent in large-area applications. OFETs are chemically degraded by the oxygen and moisture in the atmosphere. Threshold voltage (V_{TH}) control process technology such as an ion implantation is not yet established for OFETs. To increase the speed of the actuator, OFET SRAM and overdrive techniques for a driver transistor is proposed. To achieve a reliable and stable SRAM operation, a V_{TH} control technology using a back gate is developed. A 5-transistor SRAM cell is also developed to reduce the number of bit lines and cell area.

Figure 15.4.1a shows the developed Braille sheet display. Braille characters in a 6×4 array are shown on the 4×4cm² display. Each Braille character consists of 2×3 dots, and the display has a total of 144 dots. The Braille character is changed by moving the dots up and down by means of the actuator, depending on the input data. As shown in Fig. 15.4.1b, four films (frame, actuator, OFETs driver, and OFETs SRAM) are stacked in the Braille sheet display. Each Braille dot has an OFET SRAM to compensate for the slow transition of the actuator. After the input data are written to all SRAMs within 2s, all the actuators are driven at once using the drivers depending on the data. In this way, the time required to change the whole Braille display is reduced from 144s to 3s.

Figure 15.4.2 shows the circuit of the SRAM and the driver for one actuator. Only pMOS OFETs are used, because the performance of nMOS OFETs is commonly worse than pMOS. The OFETs for SRAM have back gates [4] to control V_{TH} . A write-only SRAM is enough for our Braille application, because the actuator moves depending on the hold data (DATA, DATA_b) and a SRAM read-operation is not required. Therefore, to save film area, a 5-transistor SRAM cell is developed. Compared with a conventional 6-transistor SRAM cell, a 5-transistor SRAM cell reduces the number of the bit lines by one-half and reduces the SRAM cell area by 20%. Figure 15.4.1c shows a micrograph of the 5-transistor SRAM cell. The cell area is 3.7×2.0mm². The whole cell is covered with the back gate.

In the 5-transistor SRAM cell, of primary concern is the slow write-time of DATA_b, because DATA_b has no access transistors. Our design target for the write-time of the whole SRAM (=144 cells) is within 2s. Figure 15.4.3a shows the measured waveforms of DATA and DATA_b during a write-operation. When BL is low, the transition time of DATA_b is 2ms. In contrast, when BL is high, the transition time of DATA_b is 40ms, because the drive current of M1 in Fig. 15.4.2 is small. This slow transition time can be hidden in the SRAM system-level by pipelining the write-operation. Figure 15.4.3b shows the timing chart for the pipeline. By pipelining, the total write-time for the 12×12 SRAM cells is reduced from 5.76s (=40 ms×144) to 1.47s (=10ms×143 + 40ms),

which satisfies our design target. When row-by-row simultaneous writing is available, the total write-time is reduced from 480ms (=40ms×12) to 150ms (=10ms×11 + 40ms).

The V_{TH} control technology using a back gate is shown to compensate for the immature V_{TH} control process technology and to achieve a reliable SRAM operation. Figure 15.4.4a shows the measured butterfly curves of the SRAM. Back gate voltage (V_{BGATE}) is varied. The inverter gain is 2.7. It is difficult to obtain a larger inverter gain, because the SRAM uses only pMOS OFETs. Figure 15.4.4b shows the measured V_{BGATE} dependence of the static noise margin (SNM). The power supply voltage, V_{DD} , is varied and when V_{DD} is 40V, SNM increases as V_{BGATE} increases. In contrast, when V_{DD} is 20V, an optimum V_{BGATE} of 25V achieves the maximum SNM, because there is an optimum $|V_{th}|$ for OFETs. Compared with SNM at $V_{BGATE} = 0V$, by adjusting V_{BGATE} , SNM increases 2.4 and 2.6 times when V_{DD} is 40V and 30V, respectively.

The V_{TH} control technology is also applied to compensate for the chemical degradation of the OFETs and to achieve a reliable SRAM operation. Figure 15.4.5a shows the measured aging characteristics of the inverter in the SRAM. The OFETs were kept in a nitrogen atmosphere except for the measuring time. As time passes, the inverter characteristics show a rightward shift due to the reduced $|V_{th}|$ of the OFETs. Figure 15.4.5b shows the measured aging characteristics of the inverter compensated by the back gate. Figure 15.4.5c shows the aging characteristics of SNM calculated based on Figs. 15.4.5a and b. By compensating the reduced $|V_{th}|$ of OFETs due to the chemical degradation with the back gate, a constant SNM can be achieved. Because the chemical degradation is inherent in OFETs, the proposed compensation technology is essential to OFET applications. Manufacturing variation within a plastic film for the OFETs can also be compensated by dividing the back gate and applying different V_{BGATE} .

Our design target for the transition time of the actuator is within 2s. As shown in Fig. 15.4.2, the actuator has a large capacitance (100μF). The breakdown voltage of the actuator is 3V. Figure 15.4.6 shows the measured waveforms of the actuator voltage (V_{ACT}) and the actuator displacement. The step voltage height (V_X) of V_{PL} is varied. The required displacement by Braille users is 0.2mm. When V_{PL} is equal to the breakdown voltage of -3V, the transition time is 34s, which exceeds our design target. In order to reduce the transition time, V_{PH} and V_{PL} overdrive techniques are proposed. By increasing V_X from -3V to -10V, the transition time is reduced from 34s to 2.0s, which satisfies our design target. In order to avoid a breakdown of the actuator, the overdrive period is determined by the time when V_{ACT} is within ±3V.

Finally, an operation of the Braille sheet display is demonstrated. Figure 15.4.7 shows the measured waveforms of the driver and the actuator for a Braille dot. Movement of the Braille dot, both up and down, has been successfully demonstrated. By using overdrive techniques in V_{PH} and V_{PL} , a 1.6s actuator transition time is achieved.

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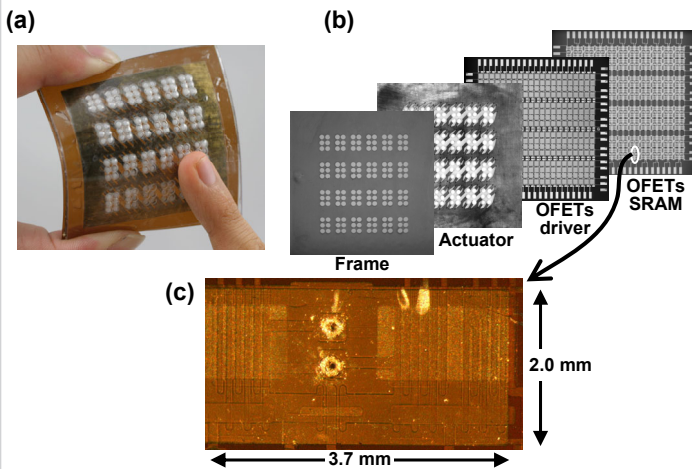


Figure 15.4.1: (a) (b) Braille sheet display. (c) SRAM cell.

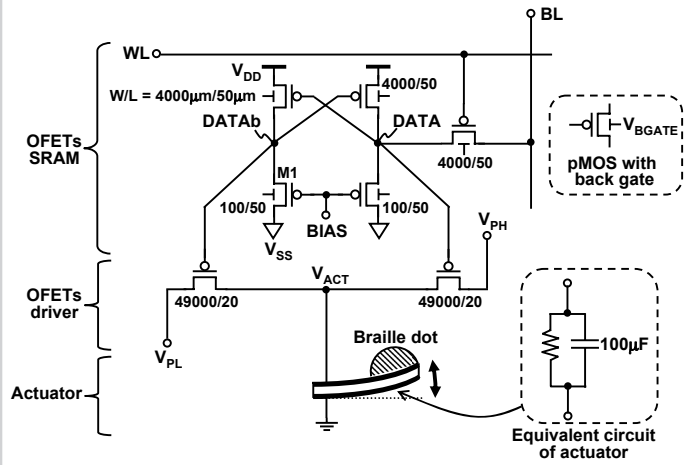


Figure 15.4.2: Circuit of OFETs SRAM and the driver for one actuator.

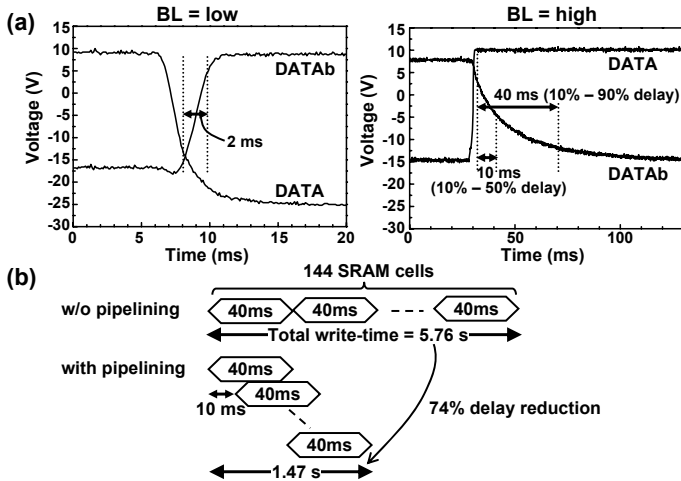


Figure 15.4.3: (a) Measured write-operation. (b) Pipelining for write-operation.

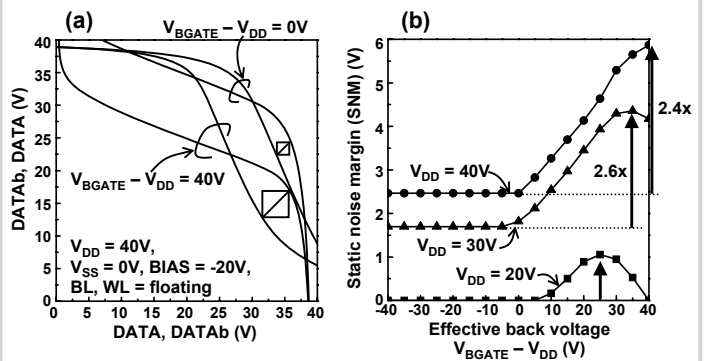


Figure 15.4.4: Measured butterfly curves and SNM of SRAM.

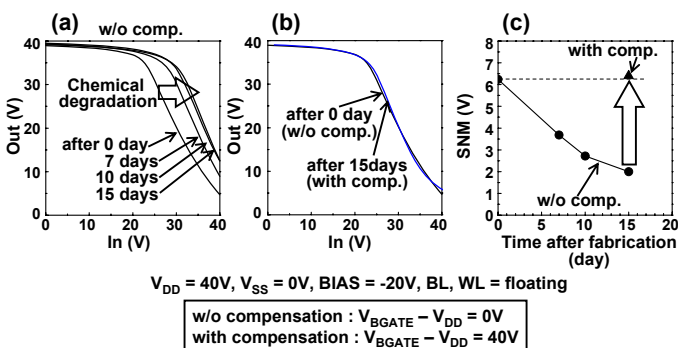


Figure 15.4.5: Measured aging of inverter and compensation for the aging.

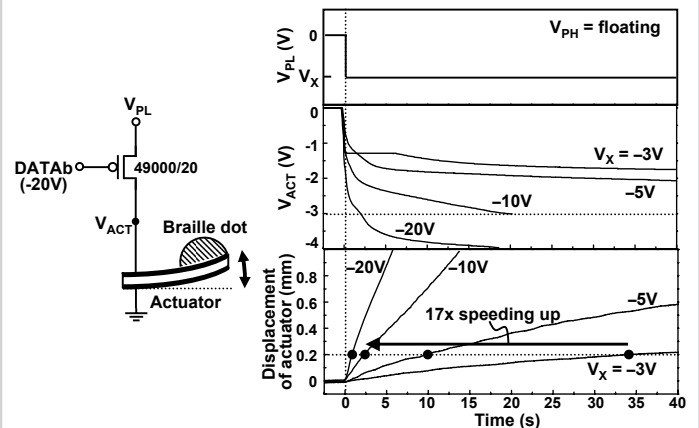


Figure 15.4.6: Measured accelerated actuator by overdrive techniques.

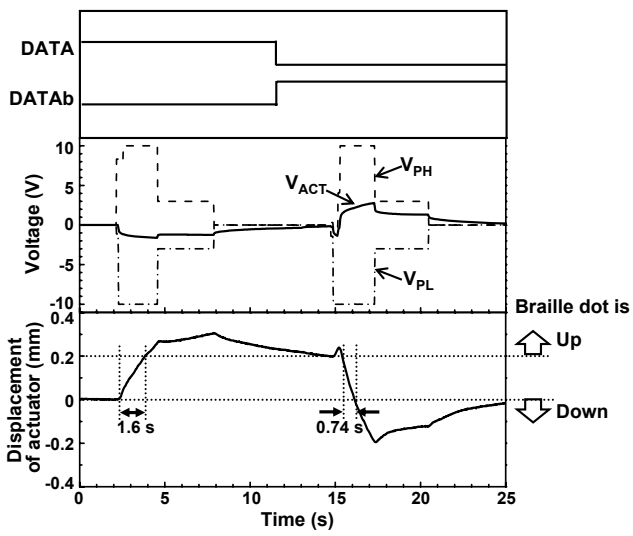


Figure 15.4.7: Measured Braille sheet display operation.