

A 1-V 299 μ W Flashing UWB Transceiver Based on Double Thresholding Scheme

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Abstract

This paper presents an Ultra-Wide-Band transceiver based on a newly proposed double thresholding scheme. The scheme does not require any precise synchronization and thus is practical in ad-hoc networks. The proposed architecture has high noise and multi-path fading signal immunities. All analog blocks are activated in a short period called 'flashing' to suppress total average power. A tested chip is manufactured using 0.15 μ m FD-SOI CMOS technology. The measured average power is 299 μ W at 25kbps data-rate over the distance of 35cm.

Keywords: UWB, low-power, flashing, double thresholding

Introduction

Ad-hoc wireless sensor networks (WSN) are attracting attention as a new field of VLSI applications. An Ultra-Wide-Band (UWB) transceiver is suitable for the WSN applications due to its low-power nature [1]-[2]. The 0-960MHz band is more suitable for low-speed applications like WSN than the 3.1-10.6GHz band in term of power [1][3]-[5]. The existing clocked correlator-based transceiver [1], however, shows more than a mW power which is not ideal for the WSN. Moreover, the correlator-based transceiver requires very precise synchronization which is very difficult to implement in ad-hoc network environments. The proposed architecture does not require the precise synchronization among distributed chips and thus practical and at the same time achieves operation power of less than a mW.

Double thresholding architecture

Fig.1 shows the architecture of the proposed transceiver which is based on bi-phase shift keying (BPSK) modulation method. The transmitter is all digital and generates a signal with positive and negative peaks shown in Fig.1 containing a wide spectrum of frequencies. The out-of-band signal is filtered out by a pulse filter and an antenna. The receiver side is composed of front-end amplifiers, continuous-time comparators, and a phase detector (PD).

An incoming pulse is amplified by the front-end amplifiers and then the amplified pulse is compared with two threshold levels to detect peaks. The comparators generate V^+ and V^- signal when positive and negative peaks are detected. Then, the PD determines the received bit (RxBit) as '1' if V^+ comes earlier than V^- ('0' otherwise) as shown in Fig.2. It is okay even if either of V^+ or V^- is not detected and in this case RxBit is interpreted as '1' if only V^+ is detected ('0' otherwise). Consequently all multi-path signals which are delayed signals are automatically neglected. Since the UWB pulse width is few nanoseconds, the system can be reset after the few nanoseconds to allow the system ready for the next

pulse. The two threshold levels generate a noise gap, between which any input is not recognized as a valid signal. Thus the noise smaller than the gap is rejected by the system. Thus, the proposed architecture can handle both noise and multi-path signal. Fig. 3 shows simulation results for bit error rate (BER) which does not much affect by noise and multi-path signal.

Flashing analog circuits with staggered clocking scheme

A parallel common-gate input amplifier (CGA) shown in Fig.4 is used as the front-end amplifier to obtain wideband impedance matching. Since the proposed architecture has high noise immunity as described above, the resistive termination which may increase input noise is used because it consumes lower power than the transconductance (G_m) termination. DC voltage at the output node of the CGA is stabilized by the opamp. This opamp is designed to have small bandwidth of a few kHz to prevent feedback loop of in-band signal. Three common-source amplifiers (CSA) are cascaded after the CGA for achieving total gain of 50dB.

Since the UWB pulse width is very short compared with the transmission period, flashing concept is effective for power reduction. In the training process, an interval of two adjacent pulses is counted digitally and the counted value is saved as an approximate signal period (PCK). Analog part is in a power-down mode from the time just after a signal pulse is detected and to the time before the next signal comes. The margin is needed to handle variation of clock mismatch among chips. This can be realized by setting the power-down period as around 90% of the PCK. Small replica circuits of amplifiers, called 'bias keeper', are used to keep the DC bias point even when the amplifiers are cut off. It was found that 4 amplifier stages should be waked up in a staggered way. Otherwise, a settling time is increased from 3.1 μ s to 5.5 μ s as shown in Fig. 5.

Measurement and comparison

A tested chip is fabricated with a 0.15 μ m FD-SOI CMOS process (Fig.6) with a die area of 0.4mm². Data rate of 25kbps is measured over the distance of 35cm with power of 299 μ W. The power consumption is almost independent from data rate because duty cycle of the flashing clock is fixed. Power budget of the transceiver is listed in Table 1. BER and comparison with previous works are shown in Fig.7.

Fig.8 shows effectiveness of each power reduction approaches. Elimination of a power-hungry time-continuous correlator, the adoption of low-power wide-band amplifiers and mostly digital scheme, and the flashing concept with staggered activation reduced the power down to μ W order.

Conclusions

A flashing UWB transceiver based on double thresholding

method is proposed and implemented, which does not require precise synchronization and has high noise and multi-path signal immunities. The fabricated test chips show the lowest power consumption ever reported.

References

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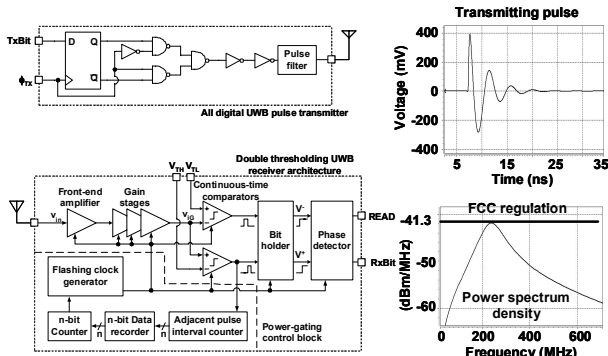


Fig. 1 The proposed UWB architecture.

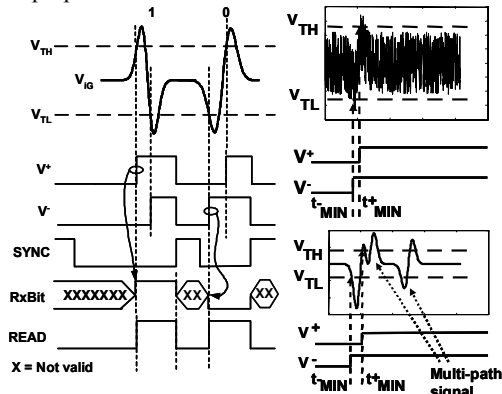


Fig. 2 Operation of the architecture in fig.1.

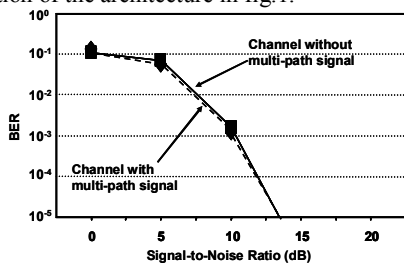


Fig. 3 BER in channel with noise and multi-path signal.

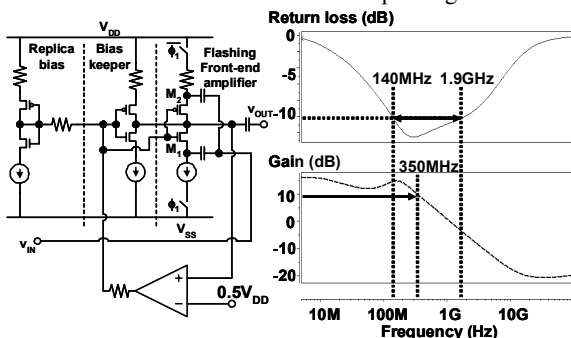


Fig. 4 Low-power front-end amplifier.

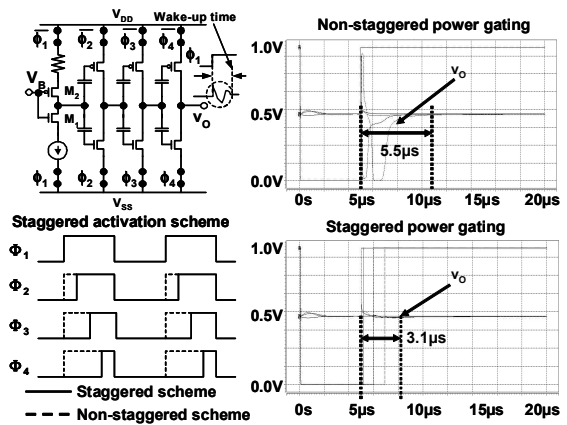


Fig. 5 Staggered activation scheme.

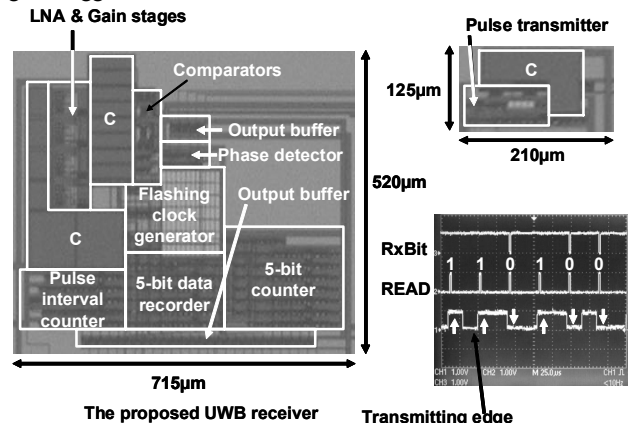


Fig. 6 Chip photograph and measurement result.

TABLE I
POWER BUDGET OF THE PROPOSED TRANSCIVER

	Static power (μW)	Dynamic power (μW)
Transmitter	--	< 1
Front-end amplifier	157	13
CSA Gain stages	360	28
Comparators	1000	78
Bias & bias keeper	150	150
Digital blocks	--	30
Total (measured)	1667	299

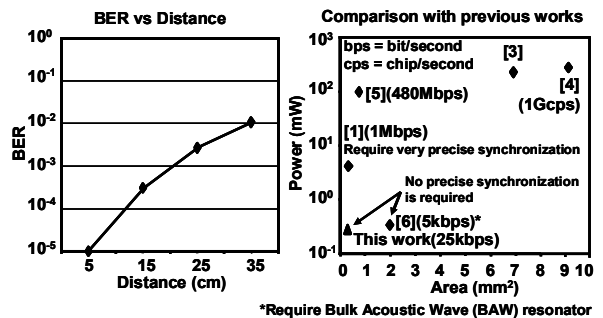


Fig. 7 BER and power comparison with previous works.

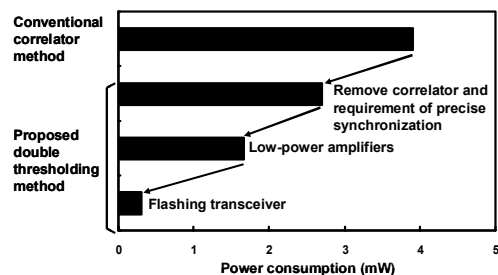


Fig. 8 Effectiveness of power reduction approaches.