An On-Chip Noise Canceller with High Voltage Supply Lines for Nanosecond-Range Power Supply Noise

Yasumi Nakamura, *Makoto Takamiya, and Takayasu Sakurai

Center for Collaborative Research, *VLSI Design and Education Center, University of Tokyo, Japan

Abstract

An on-chip noise canceller with high voltage supply lines for the nanosecond-range power supply noise is proposed. The canceller fabricated with 90-nm CMOS achieves 68% noise reduction with 2.0% power increase. Under the same noise reduction conditions, the area penalty for the canceller is 1/77 and 1/45 of those for the additional on-chip decoupling capacitors and the power supply lines respectively.

Introduction

Recent low power VLSI design techniques such as power gating, clock gating, and dynamic voltage and frequency scaling (DVFS) generate rapid and large change of the power supply current at the moment of the wake-up from the sleep mode to the active mode. The large power supply noise generated by such current change is a serious problem for low power digital VLSIs [1-2]. The noise is nanosecond-range or its frequency is usually from 100 MHz to 500 MHz [3], and is determined by the resonance of the package parasitic inductance and the on-chip decoupling capacitor. The noise suppression by decreasing the package inductance and increasing the on-chip decoupling capacitance leads to the large area penalty. Conventional clock dithering [1] and power switch control [2] to slow the current change increase the wake-up time and are not useful for the frequent wake-up and power-down. To solve these problems, an on-chip noise canceller with small area penalty and the fast wake-up is proposed.

Noise Canceller

Fig. 1 shows the schematic of the proposed circuit. A high voltage supply (V_{DDH}), a switch between V_{DDH} and the normal power supply (V_{DD}), and a level-shifter are added to the normal power supply circuit. When the logic circuit wakes up, the switch between V_{DDH} and V_{DD} is turned on by the level-shifter and the current from V_{DDH} substitutes the current flowing through the bonding wire and the onboard supply lines of V_{DD}. The principle of this circuit is shown in Fig. 2. Point A is the start of the wake-up. And the wake-up current reaches the maximum at the point B. The current from V_{DDH} decreases at C, and reaches zero at D. Without V_{DDH} supply, current via the V_{DD} line increases rapidly from A to B, which induces large di/dt noise on V_{DD} line. In contrast, with V_{DDH} supply, V_{DD} current remains small from A to C, and increases slowly from C to D, suppressing the noise. Since the noise on V_{DDH} does not influence V_{DD}, the impedance of V_{DDH} supply line can be large compared to the main V_{DD} line as long as V_{DDH} can substitute the current for V_{DD}.

Fig. 3 shows the schematic of the test chip. It consists of a 2nF capacitor emulating a 530k-gate logic circuit, M2 to make the supply current increase. M1 is used to monitor V_{DD} via a 50Ω GSG probe. M3 is used as a switch between V_{DDH} and V_{DD}, which is driven by a 0-1.0V to 1.0-2.0V level shifter.

Level shifter circuit is shown in Fig. 4. Diode-connected PMOSs are inserted between the current mirror part and the input pair part to handle 2.0V supply with 1.0V-tolerant transistors.

Experimental Measurements

Fig. 5 shows the micrograph of the chip fabricated with 1V 90nm CMOS process. The circuit capacitor occupies 1450μm x 140μm and proposed canceller occupies 4.4% of the capacitor. Since this capacitor emulates a 530k-gate logic circuit, the area penalty of this canceller is equivalent to 0.6%. Fig. 6 shows the measurement setup. Transient response with proposed canceller is measured and shown in Fig. 7. Without the canceller, the worst voltage in transient is 71mV less than the steady state IR drop, while the canceller suppresses this noise to 32%. The noise canceller consumes 2.0% power overhead of the load current for 25k transitions/sec.

As shown in Fig. 2, the timing setup of thr point C and D is important for the canceller operation, the effect of the slope of CD and timing of C was measured and shown in Figs. 8 and 9. In Fig. 8, quick turnoff of the PMOS switch makes 2nd droop, which becomes larger than the reduced 1st droop. Responses for slower turnoff with 20ns, 40ns and 80ns transition time is also shown, where turnoff slopes slower than 40ns do not make larger droop than the reduced droop. Fig. 9 shows the dependence between turnoff start time and the 2nd droop. It is shown that 2nd droops are not affected by the turnoff start time when turnoff slope is not steep. Fig. 10 shows the relation between the turnoff start time and the noise for turnoff slope of 0ns, 20ns, 40ns, and 80ns, where 100% means the noise without canceller. It is shown that with steep turnoff, the noise cancelling is not effective due to the 2nd droop.

From the results, point C was set to 40ns after the wakeup and the time between point C and D was set to 80ns.

Discussions

The area penalty of the proposed noise canceller was compared to conventional approaches, addition of the decoupling capacitors and additional pads for V_{DD}. Fig. 11 shows the simulated transient responses of conventional approach. Simulated and measured waveform without noise canceller are also shown in the Fig. 11. To obtain the same noise cancelling effect, compared to the area and pad overhead of the proposed circuit, 45 times more pads or additional decoupling capacitor with 77 times larger area is required.

Power consumption depends on the number of transitions per second as shown in Fig. 12. For applications whose sleep/wake-up frequency is below 10s of kHz, the power overhead is less than 1.0%.

Conclusions

A noise canceller using higher voltage supply lines is fabricated and verified. The canceller reduced the power supply noise to 32% with an additional power of 2.0%. With conventional approaches, it is not feasible to achieve the reduction rate since very large area or pin overhead is required.

Acknowledgement

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References

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[2] Y. Kanno *et al.*, "Hierarchical power distribution with 20 power domains in 90-nm low power multi-CPU processor," ISSCC Dig. of Tech. Papers, pp. 540-541, 2006.

[3] T. Rahal-Arabi *et al.*, "Design & validation of the Pentium III and Pentium 4 processors power delivery," Dig. of Symp. on VLSI Circuits, pp. 220-223, June 2002

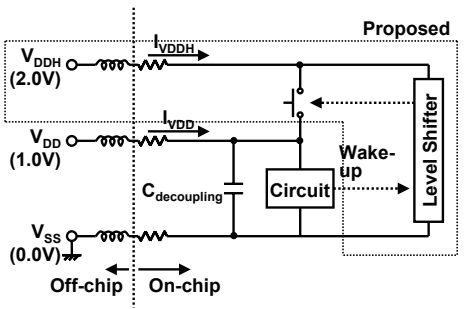


Fig. 1: Configuration of the proposed circuit

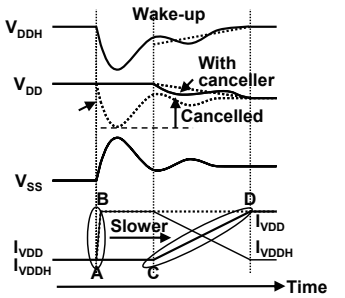


Fig. 2: Principal of cancelling noise

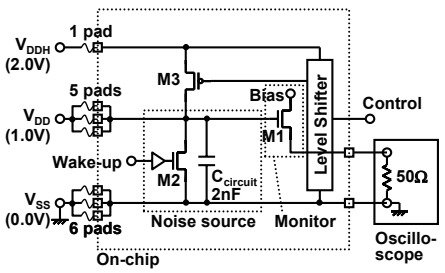


Fig. 3: Schematic of the test chip

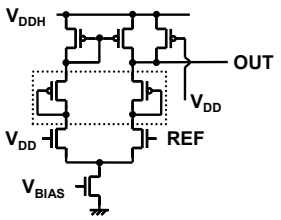


Fig. 4: Schematic of the level shifter

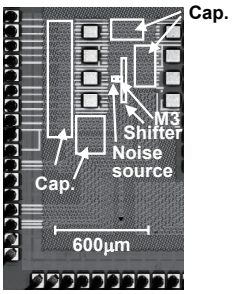


Fig. 5: Micrograph of the test chip

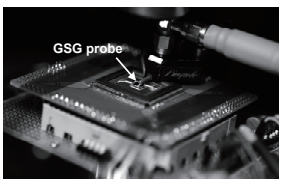


Fig. 6: The photograph of the test setup

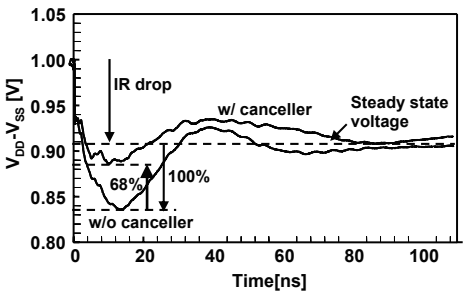


Fig. 7: Measured effect of proposed noise canceller

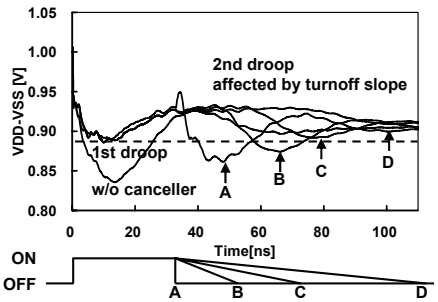


Fig. 8: Measured noise dependence with turnoff slope

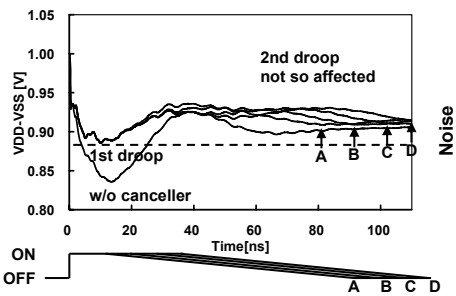


Fig. 9: Measured noise dependence with turnoff start time

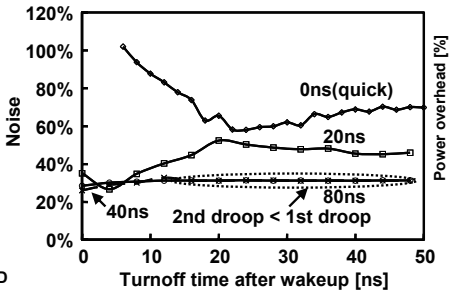


Fig. 10: Measured noise dependence with turnoff start time and slope

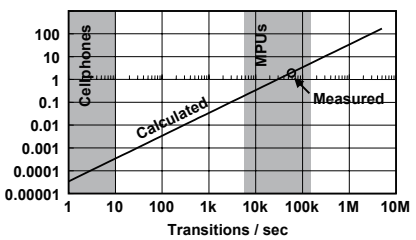
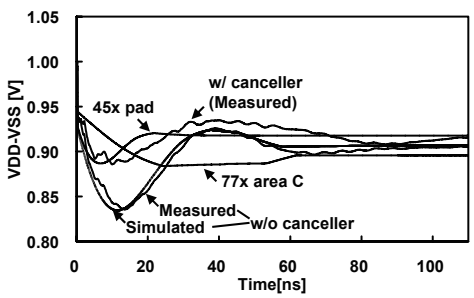
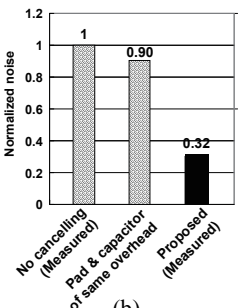


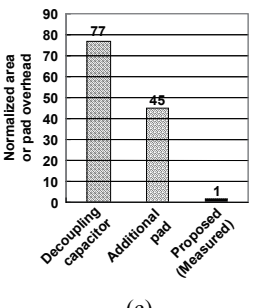
Fig. 12: Measured noise dependence with turnoff start time



(a)



(b)



(c)

Fig. 11: Simulated noise waveform and comparison with conventional approaches