

A Wide Range Spatial Frequency Analysis of Intra-Die Variations with 4-mm 4000 x 1 Transistor Arrays in 90nm CMOS

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Abstract— In order to investigate the systematic intra-die variations, the intra-die threshold voltage and on-current variations are measured thanks to 4-mm 4000 x 1 transistor arrays with 1 μm transistor-pitch in a 90nm CMOS technology, achieving the widest spatial distribution range. The spatial frequency analysis of the variations indicates that both variations are random across 4 mm. The dependence of both variations on body bias is also measured and the relationships between threshold voltage variations and on-current variations are analyzed by using the alpha-power law model.

I. INTRODUCTION

The increased variation of the MOSFET transistor device properties that come with the technology downscaling is a major issue for VLSI designers. The variations usually have systematic and random components. The systematic variations can be compensated with the chip-level or the block-level adaptive techniques, while managing the random variations is a difficult task because the correction of each transistor is not practical. It is therefore very important to distinguish the systematic variations and the random variations. Analyzing the frequency distribution of the spatial variations is an effective method to extract the systematic components. For example, spatial frequency characterization provides an optimum domain size when multi-domain adaptive body bias within a chip [1] is used to compensate the intra-die variations. Although the measurements of the intra-die variations with transistor array circuits have been previously reported [2-6], none of them shows the spatial frequency. Wide spectrum of the spatial frequency is also required, because the minimum pitch of the transistors and the chip size determine the highest and the lowest frequency respectively. The conventional circuits [2-6], provide narrow spectrum, because they have 2-dimensional arrays and are not designed for the spatial frequency measurement. In this paper, the wide spatial

spectrums of intra-die variations are measured and analyzed with the newly developed 4000 x 1 (= 1-dimensional) transistor arrays.

II. TRANSISTOR ARRAY CIRCUITS

Fig. 1 shows the structure of the transistor array circuits. A unit consists of 1000 x 1 transistors array and four units are used for the measurement of the 4000 transistors. The pitch between the transistors is 1 μm . The key challenge for the array circuits is to reduce the subthreshold leakage current due to the 999 unselected transistors well below the drain current of a selected transistor. In order to obtain more than one

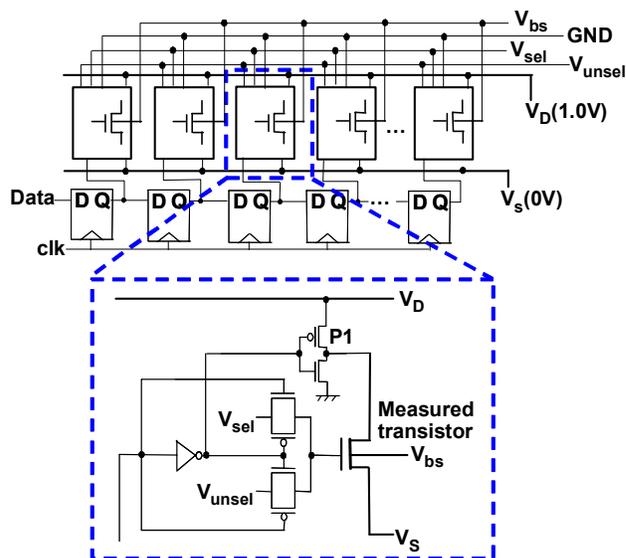


Fig. 1. Transistor array circuits for variability measurement.

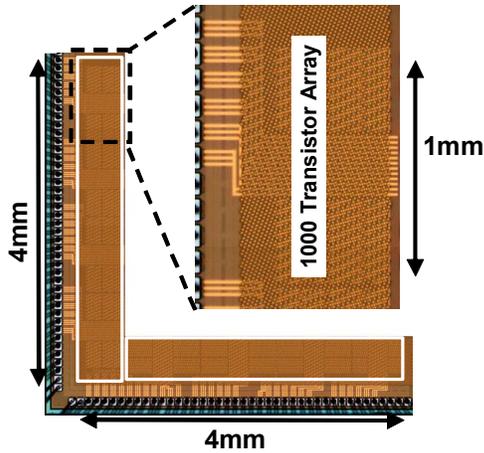


Fig. 2. Chip micrograph of transistor array circuits.

hundred times drain current for the selected transistor of the 999 unselected transistors, the drain voltages of unselected transistors are lowered by P1 to reduce the subthreshold leakage due to DIBL and the gate voltages of the unselected transistors are negatively biased with V_{unsel} . The voltage drops across P1 and V_D/V_S lines are less than 1 mV by using wide transistors and wide metal lines respectively.

Fig. 2 shows the microphotograph of the chip fabricated with 1V 90nm CMOS process. Two sets of 4-mm 4000 x 1 transistor arrays are horizontally and vertically placed on the chip respectively. This chip has four different transistor arrays: both nMOSFETs and pMOSFETs with the minimum gate length and $0.2 \mu\text{m}$ and $1.0 \mu\text{m}$ gate width. A deep n-well is used to externally control the body bias (V_{bs}) of the measured transistors to investigate the effect of V_{bs} on threshold voltage (V_{TH}) variations.

III. EXPERIMENTAL MEASUREMENT

In this chapter, nMOSFETs in the vertical array are discussed, because the measured results show no significant differences between the vertical array and the horizontal array, and the measured trends of pMOSFETs are similar to those of

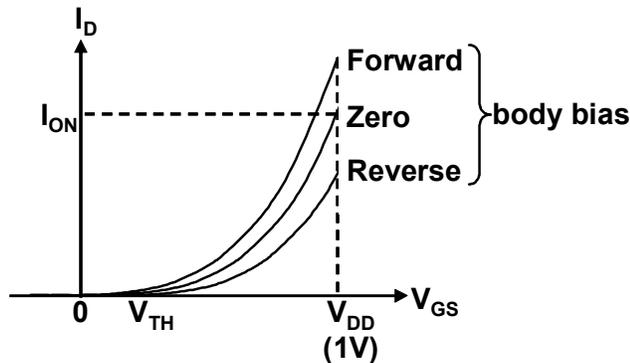


Fig. 3. $I_D - V_{GS}$ characteristics for different body bias conditions.

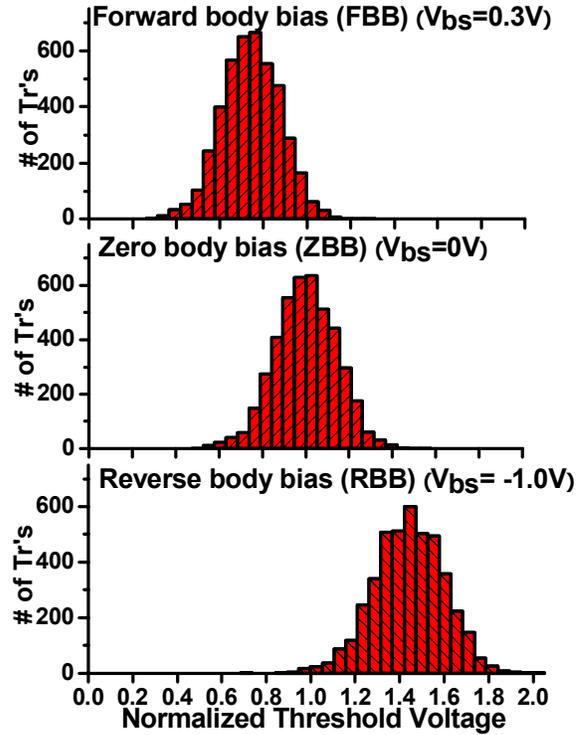


Fig. 4. Measured V_{TH} histogram for different body bias ($W = 0.2 \mu\text{m}$).

nMOSFETs. V_{TH} and the on-current (I_{ON}) of the 4000 nMOSFETs are measured and analyzed with 1 V drain-to-source bias. Fig. 3 shows $I_D - V_{GS}$ characteristics and the relationship between I_{ON} and V_{TH} for different body bias conditions. The line at zero body bias (ZBB) is a starting line. When the positive body bias is applied to the body, the forward body bias (FBB) decreases V_{TH} and increases I_{ON} . In contrast, when the negative body bias is applied to the body, the reverse body bias (RBB) increases V_{TH} and decreases I_{ON} . The relationships between V_{TH} variations and I_{ON} variations are measured and analyzed.

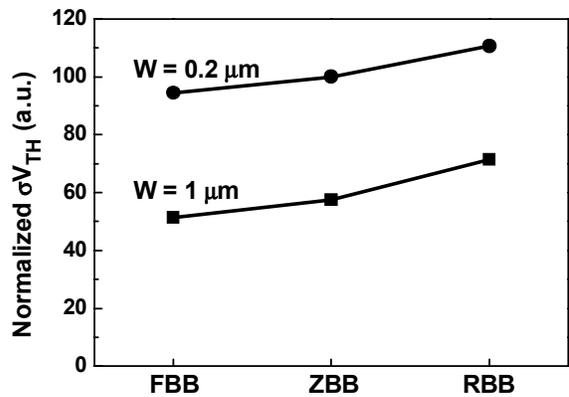


Fig. 5. Body bias dependence of the standard deviation (σV_{TH}).

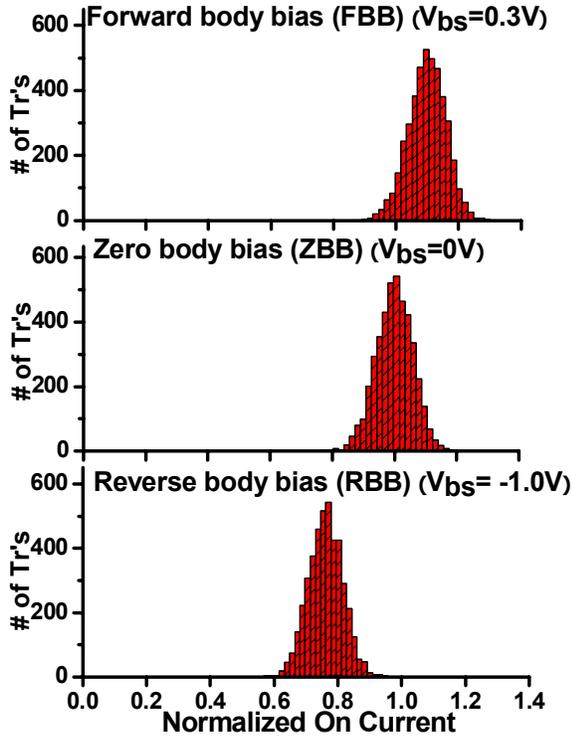


Fig. 6. Measured I_{ON} histogram for different body bias ($W = 0.2 \mu\text{m}$).

Fig. 4 shows the measured V_{TH} histogram for different body bias conditions when the gate width is $0.2 \mu\text{m}$. The histograms show Gaussian distribution. The body bias dependence of the standard deviation (σV_{TH}) of the measured V_{TH} is plotted in Fig. 5 for $0.2 \mu\text{m}$ and $1 \mu\text{m}$ gate widths. FBB decreases both the average V_{TH} and σV_{TH} [7,8] because FBB reduces the channel depletion width. In contrast, RBB increases both the average V_{TH} and σV_{TH} . The increase of σV_{TH} does not directly result in an increase of leakage [9]. σV_{TH} of $0.2\text{-}\mu\text{m}$ gate width is larger than that of $1\text{-}\mu\text{m}$ gate width [10].

Fig. 6 shows the measured I_{ON} histogram for different

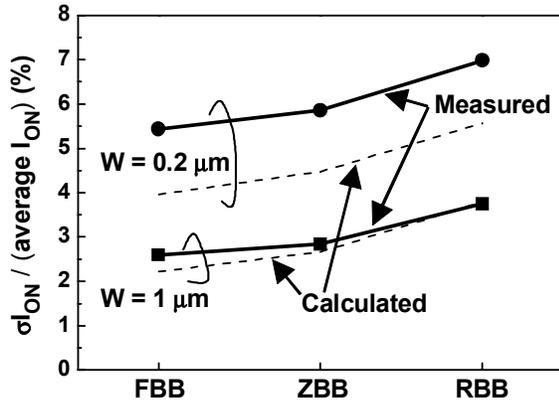


Fig. 7. Body bias dependence of the relative σI_{ON} .

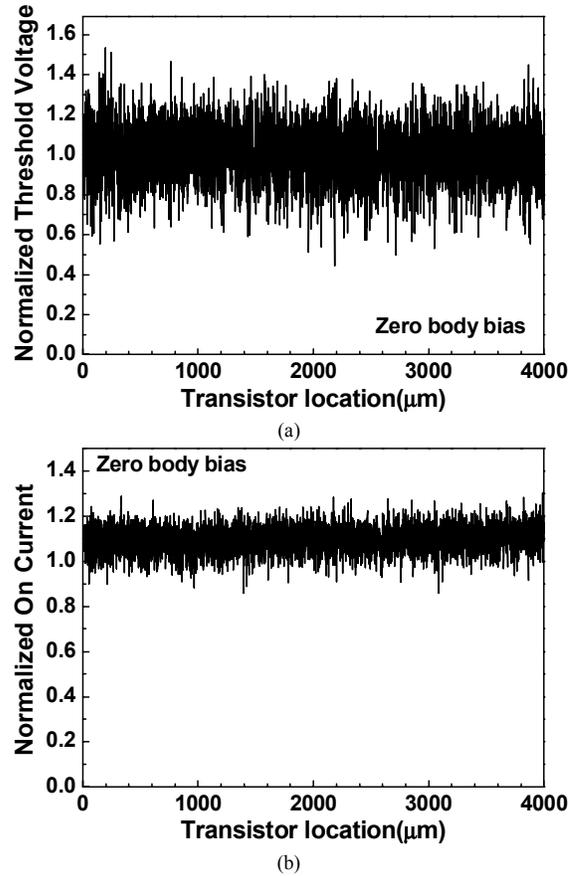


Fig. 8. Position dependence of (a) V_{TH} and (b) I_{ON} in the 4-mm 4000 transistor arrays with $1 \mu\text{m}$ pitch at ZBB ($W = 0.2 \mu\text{m}$).

body bias conditions when the gate width is $0.2 \mu\text{m}$. Fig. 7 show the body bias dependence of the relative standard deviation (σI_{ON}) of the measured I_{ON} when the gate width is $0.2 \mu\text{m}$ and $1 \mu\text{m}$. FBB increases the average I_{ON} but decreases the relative σI_{ON} ($= \sigma I_{ON} / \text{average } I_{ON}$). In contrast, RBB decreases the average I_{ON} but increases the relative σI_{ON} . In order to clarify the relationship between the relative σI_{ON} and σV_{TH} , Fig. 7 also shows the calculated body bias dependence of the relative I_{ON} by using the alpha-power law model [11] in (1) and (2),

$$I_{ON} \propto (V_{DD} - V_{TH})^{1.3}. \quad (1)$$

$$I_{ON} + \sigma I_{ON} \propto (V_{DD} - V_{TH} - \sigma V_{TH})^{1.3}. \quad (2)$$

V_{DD} is a power supply voltage. The calculated body bias dependence partially traces the measured body bias dependence, which indicates that the relative σI_{ON} is highly correlated with the σV_{TH} . The error between the measured and the calculated values at the gate width of $1 \mu\text{m}$ is less than 14%, while the error at the gate width of $0.2 \mu\text{m}$ is less than 27%. The large error is considered to be due to the mobility modulation in the narrow channel MOSFETs.

Fig. 8 gives the position dependence of V_{TH} and I_{ON} in the 4-mm 4000 transistor arrays with $1 \mu\text{m}$ pitch at ZBB and the gate width of $0.2 \mu\text{m}$. Fourier transform of the Fig. 8 gives the

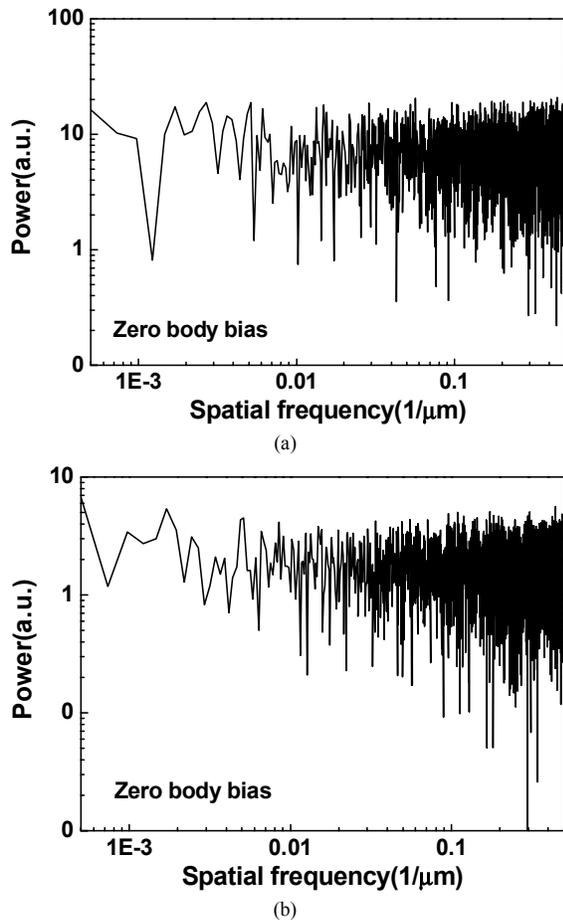


Fig. 9. Spatial spectrum of (a) V_{TH} and (b) I_{ON} in Fig. 8.

spatial spectrum shown in Fig. 9. The horizontal axes are the spatial frequency. For example, a 10- μm cycle V_{TH} variations gives a spatial frequency of 0.1 ($1/\mu\text{m}$). Fig. 9 shows no particular peak, which indicates that the intra-die V_{TH} and I_{ON} variations are random across 4 mm. The intra-die random variations correspond with [5,6].

Fig. 10 shows the comparison of the measured spatial frequency range with the past works [3-6]. This work covers the widest spatial frequency range ever reported.

IV. CONCLUSIONS

The intra-die V_{TH} and I_{ON} variations have been characterized with 4-mm 4000 x 1 transistor arrays with reduced subthreshold leakage of unselected transistors, giving the widest spatial frequency range ever reported. Measurements on a 90nm CMOS technology demonstrate that those variations are not systematic but random across 4 mm. The relationships between the measured σV_{TH} and σI_{ON} for various body biases are also analyzed by using the alpha-power law model, and the close correlation between σI_{ON} and σV_{TH} are confirmed.

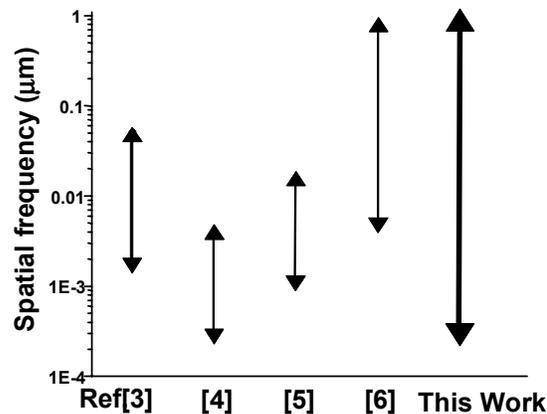


Fig. 10. Comparison of the measured spatial frequency range with the past works [3-6].

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