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Backgate Bias Accelerator for 10ns-order Sleep-to-Active Modes Transition Time

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***Abstract*-Backgate biasing is a promising technique for high-speed systems. Leakage can be reduced during standby periods by reverse bias while adequate bias in active mode can balance process and temperature variations. This technique introduces no delay penalty in active mode but slow wake up time results in system performance degradation. In this paper, a backgate bias accelerator achieving 24ns/V sleep-to-active mode transition rate is demonstrated in a 90 nm CMOS technology. The circuit performs auto-calibration of the transition time as a function of the Sleep and Active mode backgate bias voltages. Those can therefore be tuned on-chip according to process variations and/or operating conditions. The accelerator occupies less than 2.5% of the total chip area, consumes 600µW during the transitions and doesn't add any bias current during active and sleep modes.**

I. Introduction

Reduction of static power dissipation during standby (or 'sleep') periods, i.e. when no data operation must be performed, is a major requirement for any VLSI chip today. Power gating technique, which introduces high threshold voltage (V_{th}) sleep transistors to gate the power supplies of low V_{th} logic blocks during standby periods is widely used now [1] but suffers from some limitations for ultra-high speed applications. The insertion of sleep transistors results in a degradation of circuit speed and consumes silicon area. Their sizing can be a difficult task. The power supply noise induced by the switching of the sleep devices may affect the system reliability and the circuit state is lost when it is disconnected from power line, unless specific flip-flops with state retention capability during sleep modes or additional low standby power memory are used. In this last case, data saving and recovering operations increase the system latency.

An alternative to power gating is backgate/body bias: the V_{th} of the transistors is increased by reverse body bias during sleep mode, resulting in leakage power reduction. Backgate bias shows several advantages compared to power gating:

1) Unlike power gating, there is no data loss during standby mode, eliminating the requirement of specific storage elements.

2) Backgate bias can be used in active mode as well to balance process and temperature variations, and/or tune the circuit speed according to the computation requirements.

A common criticism against backgate bias is that the efficiency of reverse body-biasing degrades as technology scales due to lower body effect factor, Band-to-Band-Tunneling in reverse biased junctions, GIDL, and increased contribution of gate leakage. However, those issues can be solved by fabrication process improvements: in [2] for example, it is shown that backgate bias can reduce subthreshold leakage by one and half order of magnitude in 65nm CMOS technology. Moreover, backgate bias is expected to get increased interest in a near future with the technological evolution towards double-gate devices that demonstrate very high backgate control efficiency, such as FinFETs or SOTBOX [3].

The circuits of this work have been implemented in a 90nm CMOS technology in which the static power can be divided by 4 by applying -1V reverse backgate bias as shown in Fig. 1. In active mode, backgate bias can tune the delay of logic cells by +/- 30% (Fig. 2) to balance process/temperature variations..

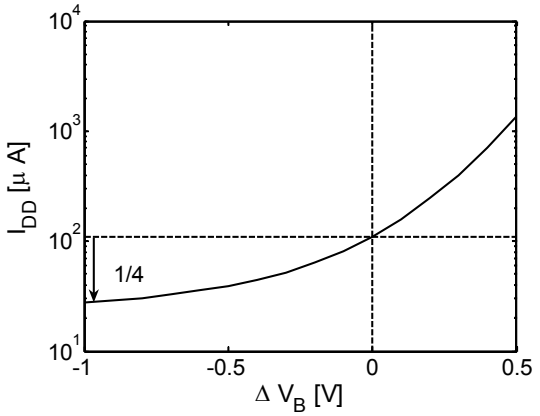

Fig. 1: Measured static current of 40k NAND gates versus backgate bias (V_{DD}=1V, $V_{Backgate}$=ΔV_B for NMOSFETs, $V_{Backgate}$=V_{DD}-ΔV_B for PMOSFETs).

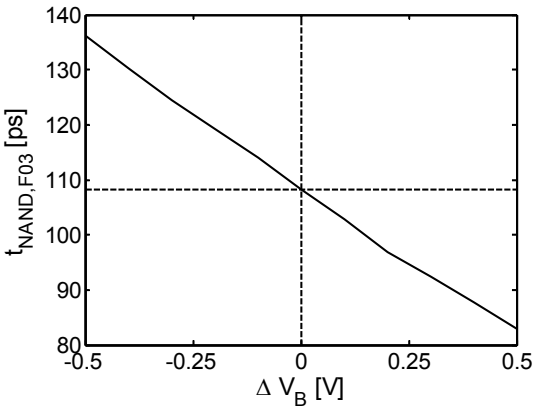

Fig. 2: Measured propagation delay of a 2NAND gate (fanout 3) versus backgate bias (V_{DD}=1V, $V_{Backgate}$=ΔV_B for NMOSFETs, $V_{Backgate}$=V_{DD}-ΔV_B for PMOSFETs).

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Backgate bias, possibly combined with variable V_{DD} [2], is therefore especially appropriate for high speed applications, like servers or super-computers, at the condition to provide fast transitions between sleep and active modes. In active mode, the backgate bias generator must provide adequate backgate bias voltage VBGA to balance process and temperature variations. Typically, this generator can be implemented as a voltage buffer with a simple source follower or an amplifier in a feedback loop [4]. It must dissipate minimum power, provided its output impedance is sufficiently low for not introducing additional noise onto the substrate. Considering this, a conventional backgate generator cannot provide fast charging of the large backgate capacitance to sweep its voltage from negative sleep backgate bias (VBGS) to VBGA in a short time.

In this paper, we present a Backgate Bias Accelerator (BBA) circuit that allows to strongly accelerate the charging of the backgate to have fast transition from sleep to active modes, with VBGA tuning capability. In section II we describe the operation principle of the new accelerator. A description of the circuits is given in section III. An experimental design on a 90nm CMOS technology is presented in section IV.

II. Backgate Bias Accelerator Principle

Let consider the backgate bias technique in the case of NMOSFETs. Fig. 3 illustrates the principle of the proposed circuit to accelerate the sleep-to-active modes transition.

In sleep mode, the sleep control signal is HIGH and the backgate is tied to VBGS (e.g. -1V). The active mode backgate bias generator is turned off and doesn't consume any DC bias current. Once the SLEEP control signal goes down, a large PMOS (the raiser) is turned on and quickly charges the backgate. The raiser is turned off once the backgate voltage has reached VBGA. This voltage is then maintained in active mode by the low power Active Mode Backgate Bias Generator. The raiser must be accurately controlled to avoid backgate charging above (if it is turned off too late) or below (if it is turned off too early) VBGA. If we turn off the raiser after that a comparator has detected that the backgate has reached VBGA, the delays of the comparator and the long raiser buffer chain introduce imprecion in final backgate voltage. In the next section we present a technique to precisely control the gate of the raiser so that it is turned off when the backgate voltage is precisely equal to VBGA.

III. Control Circuits For The Backgate Bias Accelerator

The circuit to generate the control signal for the raiser is shown in Fig. 4. It is based on the use of a mirror-delay circuit whose principle has been introduced in [5]. The operation can be explained with the timing diagram that is plotted in Fig. 5. In sleep mode (i.e. Sleep=HIGH), the backgate is reverse biased to VBGS. When the sleep (respectively sleepB) signal goes low (resp. high), the raiser is turned on and begins to charge the backgate. At the same time, the capacitor C1 is charged by a current I_C.

After a time interval t_x, the backgate reaches half of its total variation (i.e. (VBGA-VBGS)/2) causing the output of comparator I to go high. If the charging process of the backgate is sufficiently linear, we can expect that the same time interval t_x will be required to conclude the charging of the backgate up to VBGA. The rising edge at the output of the comparator stops the charging of capacitor C1 and starts the charging of an identical capacitor C2 by the same current I_C. C2 will reach the same voltage than C1 after a time t_X. At this moment the raiser can be turned off, and the backgate voltage is then kept equal to VBGA by the low power active mode backgate bias generator (ABBG). The proposed circuit automatically adapts the backgate charging time depending on the VBGA and VBGS voltages, allowing on-chip tuning of the backgate bias in both active and sleep modes as function of the process variations and/or the operating conditions.

The principle of the backgate bias accelerator relies on a linear charging of the backgate. This is only the case if the backgate capacitance is charged by a constant current. The raiser transistor must therefore operate in saturation during the complete transition. Since the raiser signal that controls its gate is grounded during the transition, saturation is guaranteed for any VBGA<V_{tp}=0.4V, where V_{tp} is the threshold voltage of the raiser.

The logic gates and the comparators of the control circuits, and the buffer chain to drive the raiser introduce additional delays that must be taken into account. A simple timing analysis shows that a proper control of the raiser requires the introduction of a delay replica as shown in Fig. 4 with a propagation delay t_{repl}:,

$$t_{repl} = 2t_{comp,I} + t_{comp,II} + 4t_{NAND} + 2t_{BUFF}$$

where $t_{comp,I}$ and $t_{comp.II}$ stand for the delays introduced by comparator I and II respectively, t_{NAND} is the propagation delay of a NAND gate and t_{BUFF} is the propagation delay through the buffer chain that drives the PMOS raiser.

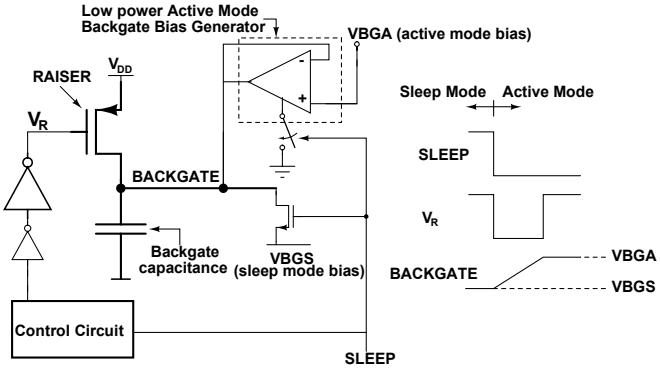


Fig. 3: Backgate Bias Accelerator Principle

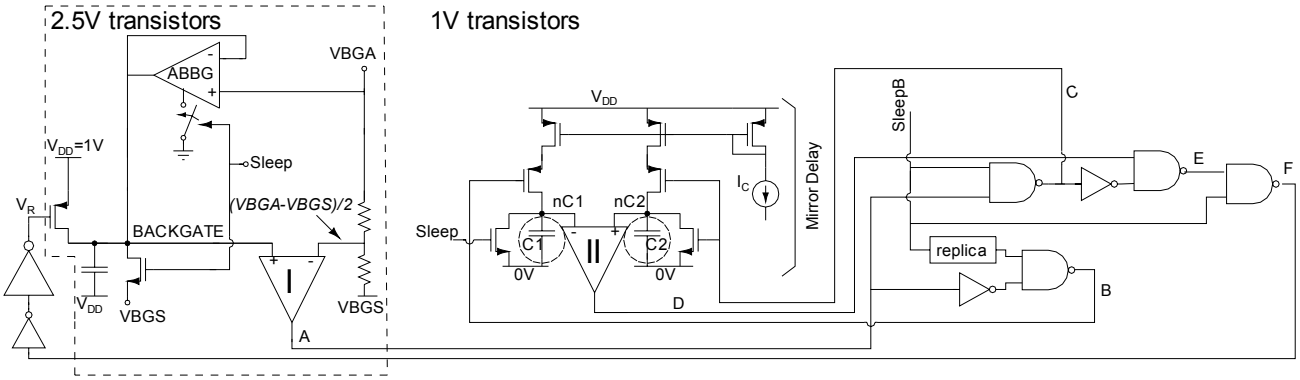


Fig. 4: Schematic of Backgate Bias accelerator

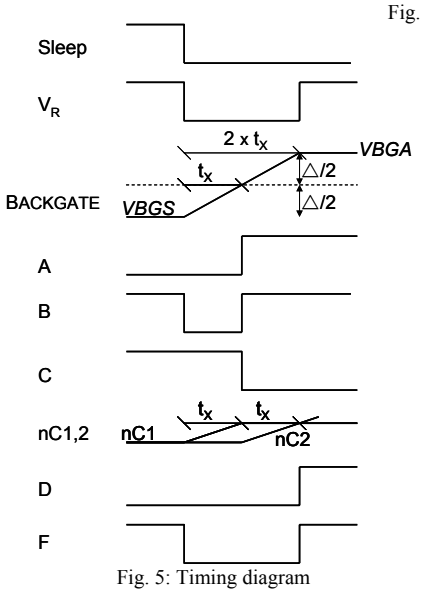


Fig. 5: Timing diagram

IV. Implementation on 90nm Process

The circuit has been implemented and measured on a triple-well 90nm CMOS technology. The same circuit could be used in a double-gate technology [3]. As a test vehicle, the BBA is connected to the P-well of 40k NAND gates. The circuits inside the dotted rectangle in Fig. 4 are supplied between V_{DD}=1V and V_{SS}=VBGS<0V (e.g. -1V). Their transistors must operate with drain-to-source voltage superior to the standard 1V supply voltage. They were therefore implemented with 2.5V I/O devices. The other circuits are conventionally supplied between V_{DD}=1V and ground.

A. Raiser

The raiser has been implemented with a PMOSFET with non-minimum length (W=40x10µm, L=1µm) for higher output impedance and better linearity of the backgate charging.

B. Comparators

The voltage stored on nC1 when the backgate has reached the half of its final value depends on VBGS, VBGA. By a proper choice of the capacitors C1 and C2 and of the current I_C, we can ensure that it lies between 0 and V_{DD} for all possible (VBGA, VBGS) pairs. Comparator II must have a relatively constant delay for any stored voltage on C1. We therefore implemented a rail-to-rail comparator that combines operational transconductance amplifiers (OTAs) with NMOSFETs and PMOSFETs differential pairs.

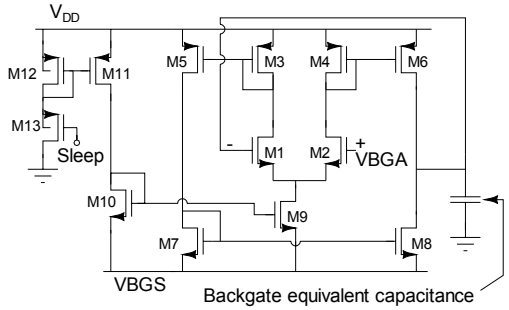
Comparator I, which is supplied by V_{DD} and VBGS lines is an OTA made of 2.5V transistors.

The DC bias of the comparators is controlled by the sleep signal to guarantee zero DC current during sleep mode.

C. Active mode backgate bias generator

The active mode backgate bias generator (ABBG) consists of an OTA in voltage follower configuration (Figs. 4, 6). It has been designed following a power constrained methodology. Its DC power dissipation must be strongly inferior to the active power dissipated by the logic. The power dissipation of a chip with an area equivalent to the 40k NAND gates test vehicle has been estimated to 50mW for a 1GHz clock frequency. The maximum DC power of the ABBG has been fixed to 3% of the total chip power. The output impedance of the ABBG must be minimized in order to reduce the noise impact on backgate voltage variations [4]. The maximum DC power fixes the maximum DC bias current of the differential pair of the OTA, and consequently determines the minimum achievable output impedance of the ABBG.

The designed ABBG provides 285Ω output impedance. The OTA shows a 47dB DC gain, its DC power dissipation is equal to 1.5mW in active mode and 72nW in sleep mode.



Transistors	Width/Length
M1,2	100/0.3 µm/µm
M3,4,5,6	30/1 µm/µm
M7,8	40/1 µm/µm
M9	60/0.5 µm/µm
M10	12/0.5 µm/µm
M11,12,13	6.5/0.5 µm/µm

Fig. 6: Active Mode Backgate Bias Generator.

D. Experimental results

A picture of the test chip is shown in Fig. 7. The total area of the backgate bias accelerator represents less than 2.5% of the total area for the 40k NAND gates. 40% of the area of the BBA is occupied by C1 and C2 that were implemented with MIM capacitors. The area overhead of the BBA could be therefore significantly reduced by the use of MOS capacitors.

The voltage of the p-well of the 40k NAND gates is measured by a high frequency active probe. BBA and the pad for probing are located on different sides of the 40k NAND block in order to take into account any RC-delay for the backgate bias.

Fig. 8 shows the measured backgate bias during sleep-to active modes transitions. VBGS is fixed to -1V, while VBGA is swept between -0.4V and 0.4V. The BBA efficiently control the ON time of the raiser according to the VBGA value, allowing on-chip tuning of both sleep and active backgate bias voltages. Without BBA, the active mode backgate bias generator alone takes up to 1µs to charge the backgate. With the BBA, the transition time between sleep and active mode ranges from 12ns to 35ns, that is more than 28 times faster. Simulations show that 5ns rising time is possible by enlarging the raiser transistor without any modification to the rest of the circuit. Without mirror-delay to precisely predict the required ON time of the raiser, the delays of the comparator and the raiser buffer would introduce higher than 100mV imprecision in final backgate voltage.

The total power dissipation of the BBA during the sleep-to-active mode transition is 600µW. Once final voltage has been reached, it can be switched off and consumes negligible power.

V. Conclusion

A backgate bias accelerator that achieves fast transition between tunable sleep and active mode backgate voltages has been designed. Conventional active mode backgate bias generators have poor drivability, resulting in slow wake up time. Our circuit achieves 0.5V change of backgate voltage in 12ns and 1.5V change in 35ns (i.e ≈24ns/V). It doesn't degrade the leakage in sleep mode and occupies less than 2.5% of the chip area, further area reduction being possible with the use of MOS capacitors.

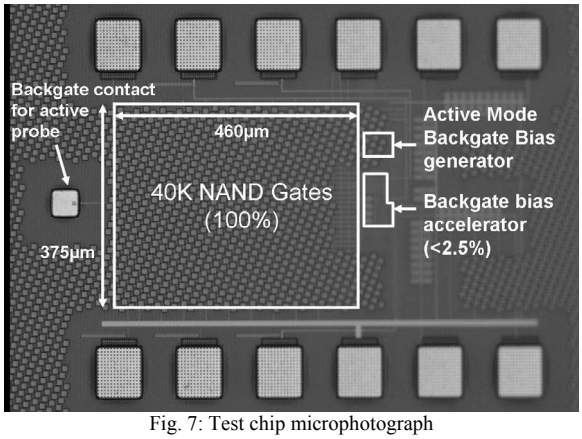


Fig. 7: Test chip microphotograph

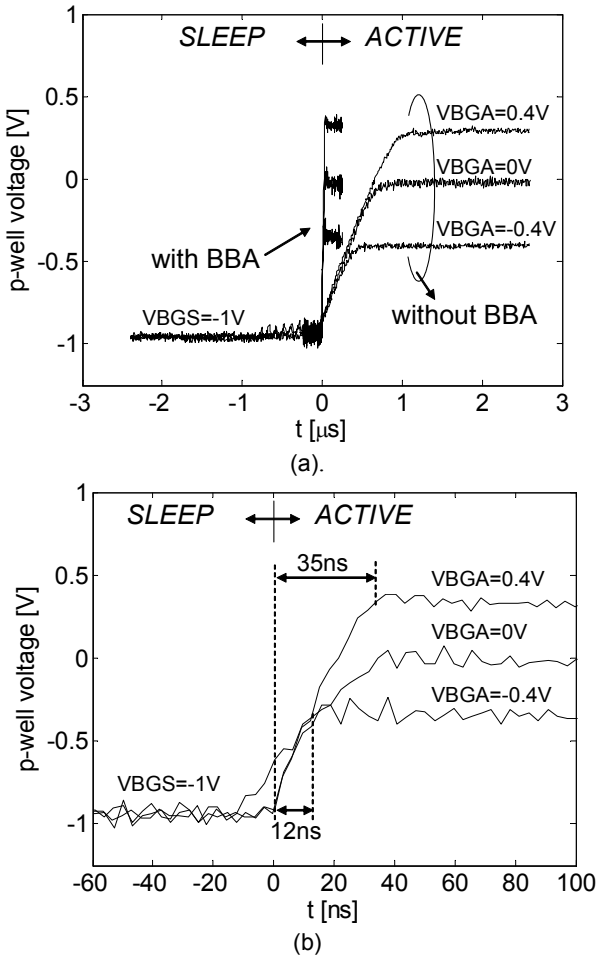


Fig. 8: Sleep-to-active voltage transitions of the backgate of 40K NAND gates: (a) with and without BBA; (b) detail of transition with BBA (VBGS=-1V, VBGA=-0.4, 0 and 0.4V).

Acknowledgments

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