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An Outside-Rail Opamp Design Relaxing Low-Voltage Constraint on Future Scaled Transistors

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SUMMARY An opamp design with outside-rail output relaxing a low-voltage constraint on future scaled transistors is presented. The proposed opamp realizes 3-V output swing without gate-oxide stress although implemented in a 1.8-V 0.18-μm standard CMOS process. The 3-V-output operation is experimentally verified. The outside-rail output design with scaled transistors shows area advantage over un-scaled and inside-rail design while keeping signal-to-noise ratio and gain bandwidth constant. The chip area is estimated to be 47% of the conventional opamp using a 0.35-μm CMOS and about an order of magnitude smaller compared with the conventional inside-rail 0.18-μm CMOS design due to reduced capacitor area. The proposed design could be extended to n-tuple V_{DD} operation and applied to circuits with a feed back loop such as gain stage and filters. The extendibility of n-tuple V_{DD} operation and its application are discussed with simulation results.

key words: *outside-rail, opamp, scaling*

1. Introduction

Signal-to-noise ratio (SNR) is a key performance factor for analog circuits. Since the SNR is proportional to the signal swing, scaled CMOS technology, which tolerates only low voltage, tends to give negative impact to the SNR. In particular, the scaled CMOS technology would considerably increase both circuit area and power consumption of analog circuits in order to keep SNR and gain bandwidth (BW) constant. Thus scaling has not been pursued extensively in analog designs.

On the other hand, for the forthcoming ubiquitous electronics applications, realizing smaller electronic systems is becoming important, and combining digital and analog on a chip is a promising solution. Therefore, analog circuit implementation using the advanced digital process whose supply voltage is sub-1 V is getting essential. The area and cost of analog circuits, however, have dominated the total chip area and cost of system-on-a-chip (SoC) in recent CMOS technology [1].

If analog circuits can be operated with a signal swing higher than the standard V_{DD}, that is, if outside-rail design is possible, the scaled CMOS technology is beneficial even to analog circuits. In this context, several outside-rail designs have been published recently [2]–[5]. An open-drain I/O buffer based on double-cascode structure [2], [3] and a push-pull buffer were presented [4]. They are, however, designed as digital output buffers. For analog circuits, an RF power amplifier based on double-cascode structure [5] was discussed but it is limited to non-push-pull output amplifier without differential input stages which is not directly applicable to widely used opamp design.

Although an opamp is a mainstream analog component, outside-rail opamp designs have not been published. There was a report on a high-voltage opamp [6] but does not realize outside-rail output swing. Thus it is not effective for improving the SNR.

In this context, we proposed a high-voltage tolerant opamp with outside-rail output swing in order to relax the low-voltage constraint of future scaled transistors [7]. In this paper, Sect. 2 briefly reviews issues on the conventional analog scaling and introduces the concept of the outside-rail design with another analog scaling. Section 3 presents details of the proposed outside-rail output opamp. Section 4 demonstrates experimental results from the test chip that manufactured in a 0.18-μm standard CMOS process, and discusses comparison with conventional opamps, extendibility to n-tuple V_{DD} operation, and its application. Finally, the conclusions are given in Sect. 5.

2. Analog Scaling and Outside-Rail Concept

2.1 Conventional Analog Scaling

This section briefly reviews area and power issues on the conventional analog scaling. At first, some preconditions of this work are mentioned. The drain current I_D of the scaled short-channel transistors is given by (1) with the alpha-power law [8].

$$I_D = \frac{W}{L} P_C (V_{GS} - V_{TH})^{\alpha}, \tag{1}$$

where P_C is process dependent parameter and the alpha is also a process dependent parameter ranging from 1 to 2 and not simply scaled. V_{GS}-V_{TH} is typically around 0.2 V and hard to be scaled. Therefore, both the alpha and V_{GS}-V_{TH} can be assumed to constants for the area estimation based

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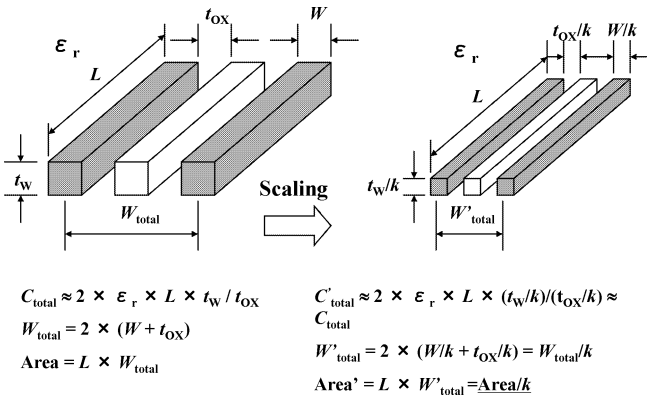

Fig. 1 Scaling on metal-insulator-metal capacitor with parallel interconnection configuration.

on gate oxide thickness t_{OX}, W, and L since whose result is almost equal to the result by the square law. Thus, the area comparison is made using the square law in this work. Another precondition is the scalability of an on-chip capacitor. If the metal thickness, line space, and line width are scaled with the factor k and permittivity is constant, an on-chip metal-insulator-metal capacitor such as a comb capacitor can be realized with $1/k$ of the area of the un-scaled case as shown in Fig. 1.

For digital circuits, the process scaling brings benefits such as lower power, shorter delay, and smaller area [9]. On the contrary, power, delay, and area in analog circuits are determined by SNR and BW. Assuming that the signal bandwidth equals to circuit bandwidth, the SNR of the analog circuit is expressed as

$$SNR = \frac{v_S^2}{v_N^2} = \frac{v_O^2}{k_B T/C}, \tag{2}$$

where v_S^2 is the signal power proportional to the square of the output voltage swing, v_N^2 is the thermal noise power, v_O^2 is the output voltage swing, which has a close relation to the supply voltage, k_B is the Boltzmann's constant, T is the absolute temperature, and C is the load capacitor of the circuit [10]. Thus, the load capacitance is expressed as

$$C = \frac{k_B T}{v_N^2}. \tag{3}$$

When the supply voltage V_{DD} is lowered by the process scaling with factor k, the signal dynamic range is limited to approximately $1/k$ of the un-scaled signal dynamic range. In order to keep the SNR constant, k_BT/C noise should be suppressed and consequently the load capacitor of the scaled circuit must be k^2 times the load capacitor of the un-scaled circuit. The area of the load capacitor scaled by k, therefore, would be k times the area un-scaled although an area of an on-chip capacitor could be shrunk by the process scaling as previously mentioned. In addition, the power consumption of the scaled circuit, P', is k times the power of the un-scaled circuit, P, in order to charge the larger load capacitor, k^2C, in the same BW as expressed as

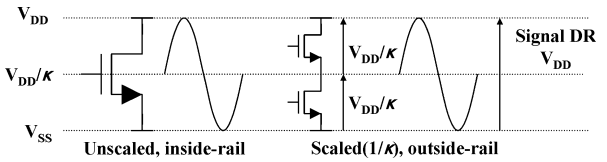

Fig. 2 The concept of the outside-rail amplifiers with scaled devices.

$$\begin{aligned} P' &= \left(\frac{V_{DD}}{k}\right)\left(\pi(k^2C)G_{BW}(V_{GS} - V_{TH})\right) \\ &= \left(\frac{V_{DD}}{k}\right)(k^2 I_{Bias}) = kP, \end{aligned} \tag{4}$$

where G_{BW} is gain bandwidth. Thus the process scaling has not been pursued extensively in the conventional analog designs so far.

2.2 Concept of Out-Side Rail Design and Another Analog Scaling

If analog circuits could be operated with larger output swing exceeding the standard V_{DD}, in other words, if an outside-rail design is possible, the process scaling is beneficial even to analog circuits. Figure 2 shows the concept of an outside-rail design. V_{DD} is a typical supply voltage for an un-scaled device. The conventional inside-rail design can handle the signal whose dynamic range is up to V_{DD}. On the other hand, the outside-rail design consists of scaled devices. Each scaled MOSFET tolerates only V_{DD}/k due to the gate oxide reliability. The signal dynamic range, however, achieves V_{DD} that is equal to un-scaled inside-rail design since the voltage stress is relaxed by the staking structure. In other words, the outside-rail design can almost double the output voltage. Since the signal dynamic range is kept constant, the same load capacitance is required in order to realize the same SNR. Therefore the area of capacitors in the outside-rail design is given by

$$A'_C = A_C/k \quad (\because C' = C), \tag{5}$$

where Ac' is the area of capacitors in the scaled outside-rail design and Ac is the area of the un-scaled inside-rail design. Similarly, the total area of MOSFET's is given by

$$\begin{aligned} g'_m &= g_m/k^2 = \frac{(W/k^2)}{L} P_C(V_{GS} - V_{TH}) \\ A'_M &= (W/k^2)L = A_M/k^2 \\ A_{M'total} &= kA'_M = A_M/k, \end{aligned} \tag{6}$$

where g'_m and gm are mutual conductance of the outside-rail design and the inside-rail design respectively and A'_M and A_M are the area of the MOSFET used in the outside-rail design and the inside-rail design respectively.

Both the area of capacitors and area of MOSFETs in the outside-rail design can be reduced while keeping power consumption, SNR, and BW constant. That is, the scaled CMOS technology is beneficial even to analog circuits with the outside-rail design. Table 1 summarizes the analog scaling by both the conventional un-scaled inside-rail design and the proposed outside-rail design.

Table 1 Summary of the analog scaling with the conventional inside-rail design and the outside-rail design.

Device or circuit parameter	Conventional approach inside-rail	Proposed approach outside-rail
Device dimensions t_{OX}	$1/k$	$1/k$
Device dimensions L	$1/k$	$1/k$
Device dimensions W	1	$1/k$
Supply voltage V	$1/k$	1
Signal voltage V_{signal}	$1/k$	1
SNR	1	1
Capacitance $C_{eff} \propto (SNR/V_{signal})^2$	k^2	1
Current $I_{bias} \propto C_{eff}$	k^2	1
Power VI_{bias}	k	1
Area of MOS A_M=WL	$1/k$	$1/k$
Area of capacitor A_C	k	$1/k$

k:Scaling factor

3. Circuit Design

In order to realize outside-rail output design, the voltage over-stress on gate oxide is to be overcome. On the other hand, junction breakdown problem is not that severe since the breakdown voltage of the drain-substrate junction is typically 3–4 times higher than that of the gate oxide [2].

A schematic of the proposed outside-rail output opamp is depicted in Fig. 3. The first stage of this opamp should accept twice the standard V_{DD} as a power supply. M_2, M_5, and M_6 are added to solve the gate over-stress problem on M_1, M_3-M_4, and M_7-M_8. Since the output swing of the first stage is limited by the additional transistors, a level shifter and an output buffer are added. The level shifter driving class AB push-pull output buffer consists of stacked current sources, M_9 and M_{12}, and resistors R_1-R_2. In order to avoid over-stress problem, M_{10}-M_{11} are added and R_1-R_2 are made of n-well. The double-cascode structure based on [2] is adopted for the push-pull analog output buffer to realize outside-rail output swing. The top pmos transistor M_{13} and the bottom nmos transistor M_{22} operate in the saturation region, and the remaining stacked transistors M_{14}-M_{15} and M_{20}-M_{21}, dynamically switched by M_{16}-M_{18}, operate as resistors in the linear region. The drivability of the output buffer is, therefore, dominated by output load capacitance and mutual conductance of M_{13} and M_{22}.

In order to show that the circuit solves over-stress problem, SPICE simulation is carried out using 0.18-μm 1.8-V standard CMOS process assuming 3.6-V input and 3.6-V power supply. Figure 4 shows the schematic of an inverting amplifier using the double V_{DD} opamp and the result of transient analysis. V_{GS}-V_{GD} trajectories extracted from the transient analysis including the initial settling states are plotted in Fig. 5. As is seen form the figure, all V_{GS}-V_{GD} trajectories are within -1.8 V to 1.8 V and this verifies that each transistor is free from over-stress voltage across gate oxide even in transients with the output swing of the circuit being twice the standard V_{DD}.

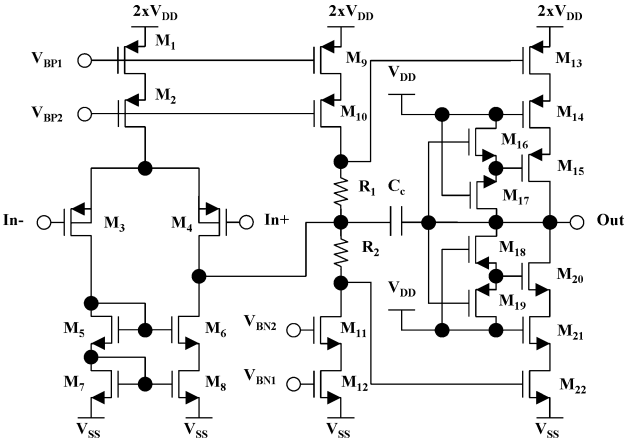

Fig. 3 A schematic of proposed opamp with outside-rail output swing.

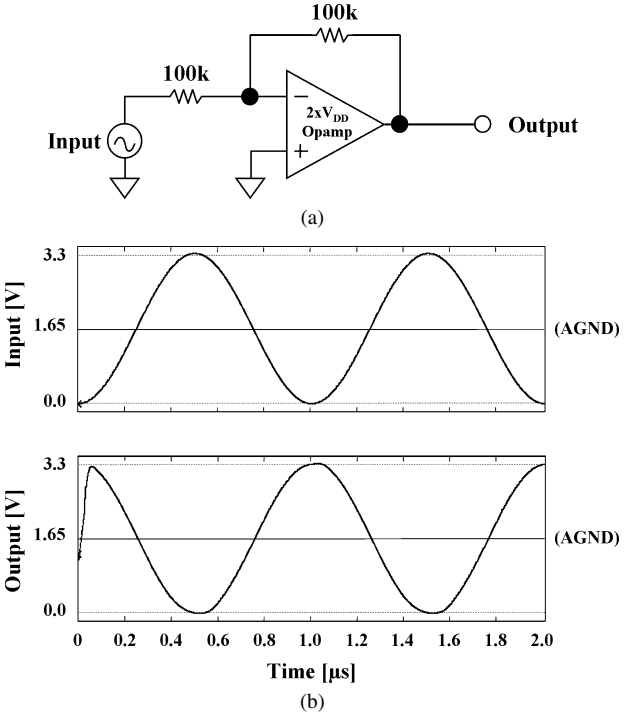

Fig. 4 (a) A schematic of an inverting amplifier using the outside-rail opamp. (b) SPICE simulation result of transient analysis.

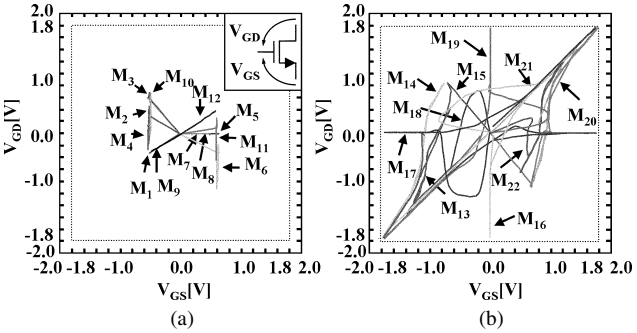

Fig. 5 Simulated VGS-VGD trajectories whose output swing is twice the standard VDD. (a) Input stage and level shifter. (b) Output buffer.

4. Measurement Results and Discussions

4.1 Measurement Results

A test chip is designed and fabricated using 1.8-V 0.18-μm standard CMOS process without thick-oxide transistors. The microphotograph of the test chip is shown in Fig. 6, and the chip area is $100\,\mu\text{m} \times 160\,\mu\text{m}$. Measured open loop frequency response is plotted in Fig. 7. In this design which aims at audio applications, the measured open loop gain is 45 dB and the gain bandwidth is 13 MHz with the phase margin of 60 degrees at 20-pF load capacitance. The open loop gain is slightly low due to stability and power requirement. The open loop gain, however, could be achieved to around 60 dB with this topology by either increasing gain bandwidth of output stage or inserting additional resistor in the phase-compensation loop. The area of the opamp will be still smaller than that of un-scaled opamp design, although the total area of the opamp may be increased by a few tens percent because of either the additional resister or widened MOSs in order to improve the open loop gain.

A schematic of an inverting amplifier using proposed opamp and the measured large-signal waveform are shown in Fig. 8. The chip works successfully with 3-V outside-rail sinusoidal wave, with 0.9% total harmonic distortion. Although the stack structure tends to increase distortion, a reasonable performance can be realized with the outside-rail design.

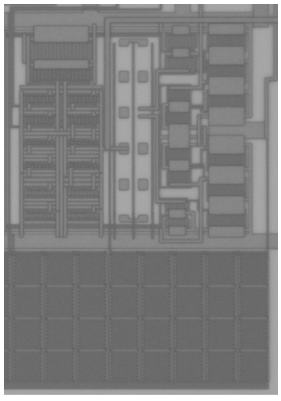

Fig. 6 A chip microphotograph of the proposed opamp implemented by a 0.18-μm 1.8-V standard CMOS process.

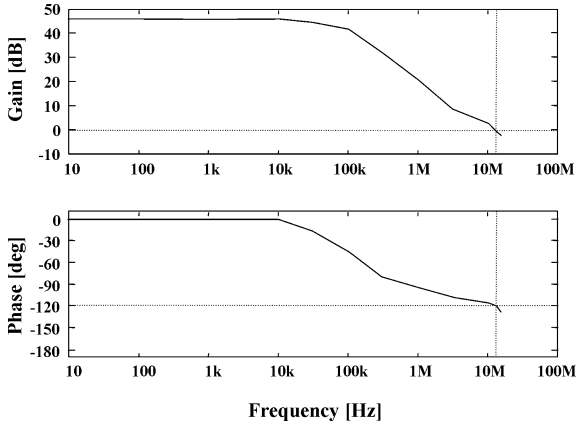

Fig. 7 Measured open loop frequency response. The gain bandwidth is 13 MHz with the phase margin of 60 degrees.

4.2 Area Comparison

An area comparison is made with conventional design choices as shown in Fig. 9. The proposed outside-rail design is smaller than un-scaled 0.35-μm and scaled 0.18-μm CMOS designs with the conventional two-stage opamp configuration keeping the SNR constant. Table 2 summarizes an area and power comparison among design choices. The values are measured for the proposed outside-rail design and estimated for other design options using SPICE.

The outside-rail design can almost double the output voltage compared with the scaled inside-rail design, and consequently the requirement of noise floor can be relaxed up to double the v_S. Therefore the load capacitance can be

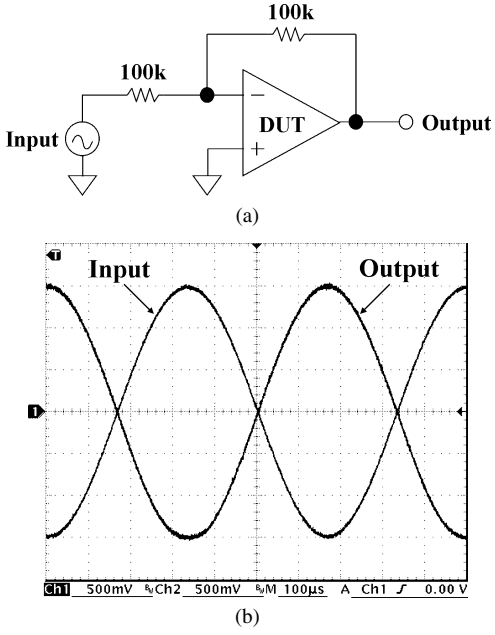

Fig. 8 (a) A schematic of an inverting amplifier using proposed opamp. Gain is −1. (b) Measured large signal inverting output. Input signal is 1.5-kHz sinusoidal wave with amplitude of 3 VPP. An outside-rail output swing is achieved.

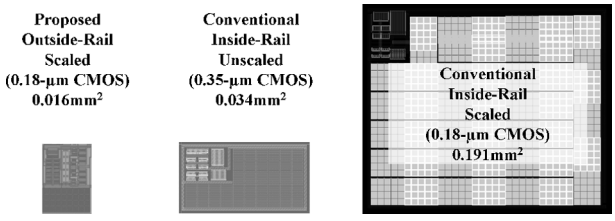

Fig. 9 Chip areas comparison with other design choices. The conventional cases are designed but not manufactured.

Table 2 Comparison between proposed opamp (0.18-μm) and conventional opamp(0.35-μm, 0.18-μm).

	Proposed outside-rail 0.18-µm (Measured)	Conventional inside-rail 0.35-µm (Estimated)	Conventional inside-rail 0.18-µm (Estimated)
Supply	3.3V	3.3V	1.8V
Output swing , v_S	3V	3V	1.5V
Power	2.1mW (96%)	2.2mW (100%)	4.7mW (213%)
GBW	13MHz	13MHz	13MHz
C_{LOAD}	20pF	20pF	80pF
$v_N^2 = k_B T/C$	$(14.4\mu V)^2$	$(14.4\mu V)^2$	$(7.2\mu V)^2$
Capacitor area	0.007mm²	0.025mm²	0.179mm²
Total area	0.016mm² (47%)	0.034mm² (100%)	0.191mm² (562%)

reduced to a quarter. This decreased capacitance reduces required g_m of transistors and the compensation capacitor in the condition that a GBW is kept constant. The reduced g_m and the compensation capacitor are beneficial to reduce both area and power compared with the inside-rail design.

On the other hand, compared with the un-scaled inside-rail design, the outside-rail design needs the same g_m of the input transistor in order to achieve the same SNR and GBW, since g_m is proportional to SNR $\times$ GBW. The area of the input pair can be reduced to 1/4 because g_m of each transistor is proportional to $(1/t_{OX}) \times (W/L)$ where W, L and t_{OX} are scaled as $W \times 2 \times (1/2)$, $L \times 1/2$, and $t_{OX} \times 1/2$ respectively to achieve the same g_m. The same effective g_m of the output stage is required to achieve the sufficient stability. This can be implemented by using double stacked structure of $W \times 1/2$, $L \times 1/2$, and $t_{OX} \times 1/2$ transistors. Thus, area of the output stage is reduced by almost 2. Considering that most of the circuit area is based on stacked structures including the telescopic configuration of input stage, the total area can be reduced to 1/2. Since the V_{TH} variation is generally proportional to t_{OX} and inversely proportional to square root of $W \times L$, the V_{TH} variation is not an issue for the outside-rail design. Since the current of the circuit is also proportional to $(1/t_{OX}) \times (W/L)$ of the input transistor pair, the total current of the circuit is almost the same as in the un-scaled design.

An area of an opamp includes a MOS area and a capacitor area. The ratio of the MOS area to the capacitor area is varied by several factors such as process rules and circuit preciseness. The outside-rail opamp design, however, can reduce both the MOS area and the capacitor area, and is effectual in various applications.

4.3 Extendibility of n-Tuple V_{DD} Outside-Rail Opamp

The proposed opamp can be extended to an opamp with the output swing of n times the standard V_{DD} as shown in Fig. 10. The additional stacked transistors in the output buffer behave as resistors in the phase compensation loop from the viewpoint of the stability. The drain-source resistance of the additional transistors must be sufficiently low to meet the application-specified stability. When the drain-substrate junction breakdown voltage is an issue, for example 4 times the standard V_{DD}, each well voltage should be controlled dynamically by a similar way to the gate-voltage control. In that case, the proposed outside-rail opamp should be implemented into the process with well-isolation structure such as triple well or implemented into SOI that is inherently free from the drain-substrate junction breakdown issue. SPICE simulation is carried out using the aforementioned 0.18-μm CMOS process assuming 5.4-V input and 5.4-V power supply. Simulated output waveform and V_{GS}-V_{GD} trajectories of an opamp with three times the standard V_{DD} are shown in Fig. 11 and Fig. 12 respectively. The output swing achieves three times the standard V_{DD} as show

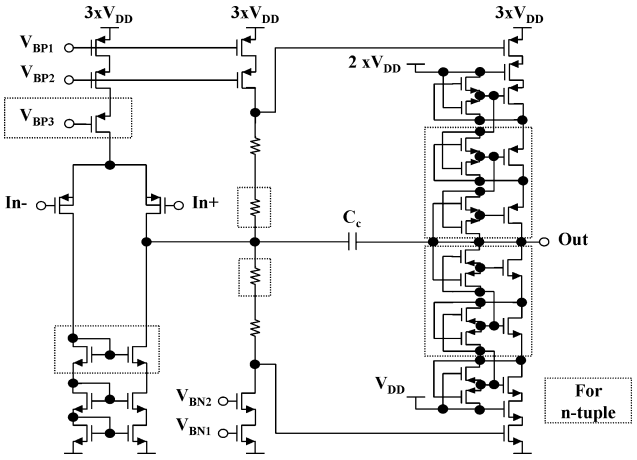

Fig. 10 Extendibility of n-tuple V_{DD} opamp with outside-rail output.

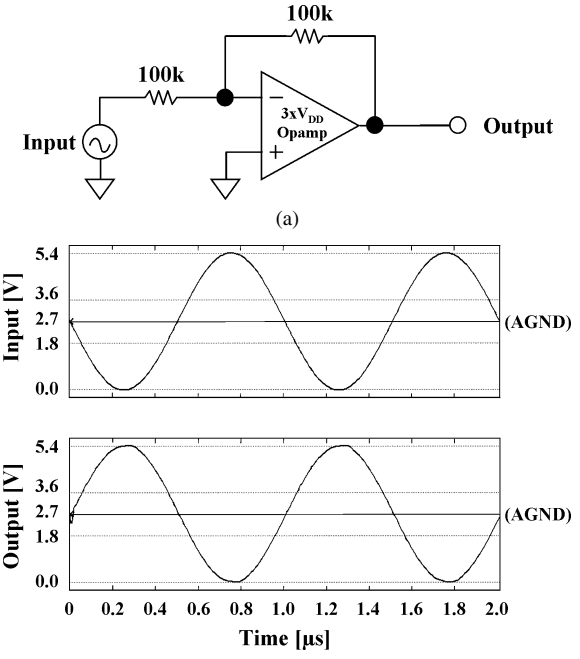

Fig. 11 (a) A schematic of an inverting amplifier using the triple V_{DD} opamp. (b) Simulation result of transient analysis. The output swing achieves three times the standard V_{DD}.

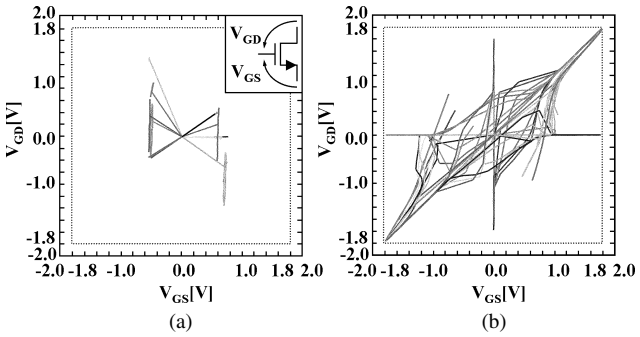

Fig. 12 Simulated V_{GS}-V_{GD} trajectories of which output swing is three times the standard V_{DD}. (a) Input stage and level shifter. (b) Output buffer. Each transistor is free from the gate-oxide stress.

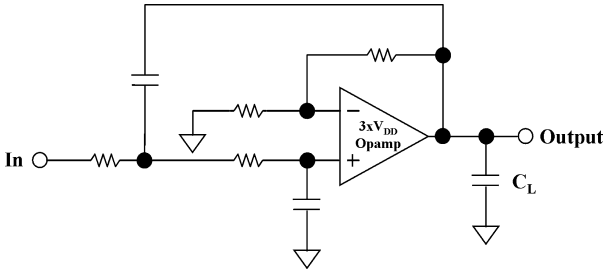

Fig. 13 A schematic of an of the Sallen-Key active low-pass filter as an application of the proposed outside-rail opamp.

in the figure. All V_{GS}-V_{GD} trajectories extracted from the transient simulation are shown to be within −1.8 V to 1.8 V and this verifies that each transistor is free from voltage over-stress across gate oxide even when the output swing of the circuit is three times the standard V_{DD}. Thus the extendibility to higher voltages is shown and it could be said that the proposed approach is promising in the further scaled environments where each transistor tolerates the lower voltages.

4.4 Application of the Outside-Rail Opamp

Figure 13 depicts a schematic of the Sallen-Key active low-pass filter as an application of the proposed outside-rail opamp. Figure 14 shows a simulation result of the second-order Sallen-Key filter designed for sound processing circuitry whose cutoff frequency is 10 kHz using the triple V_{DD} opamp, and the 1 dB compression point is 10.8 dBm. The simulation results verifies that the proposed opamp could be applied to various analog building blocks with a feed back loop such as gain stage, integrators, filters and so forth.

5. Conclusion

An opamp with 3-V outside-rail output swing in a 1.8-V 0.18-μm standard CMOS process is presented and verified by measurement. The outside-rail opamp shows smaller area with the same SNR and power consumption compared with the un-scaled option and inside-rail design style. The outside-rail design could be extend to n-tuple V_{DD} opamps

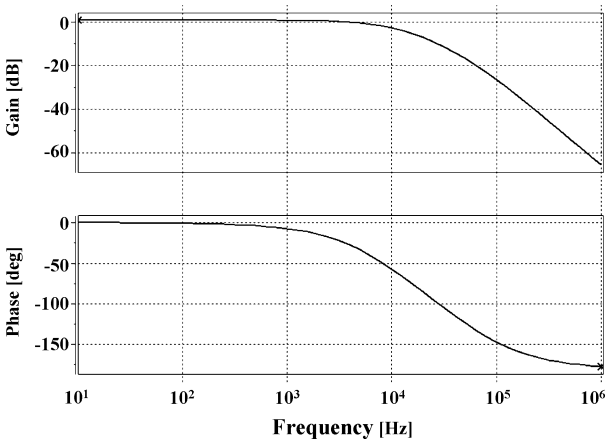

Fig. 14 Simulated frequency response of the second-order Sallen-Key filter with the triple V_{DD} opamp.

and applied to various analog building blocks with a feed back loop such as gain stage and filters. Thus, the proposed outside-rail opamp is beneficial to reduce area of the circuit in future scaled transistors designs.

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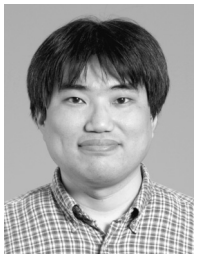

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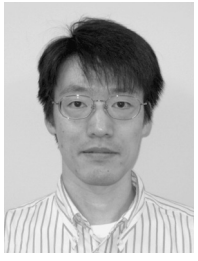

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