Dependence of Minimum Operating Voltage (V_{DDmin}) on Block Size of 90-nm CMOS Ring Oscillators and Its Implications in Low Power DFM

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Abstract

The minimum operating voltage (V_{DDmin}) of 90-nm CMOS ring oscillators (RO's) is investigated in order to clarify the lower limit of supply voltage (V_{DD}) for logic circuits. The measured V_{DDmin} is determined by the intra-die threshold voltage random variations and increased from 91 mV to 224 mV when the number of RO stages increased from 11 to 1001, which hinders the V_{DD} scaling. Lowering V_{DDmin} is difficult, since it would require an impractical inverter-by-inverter adaptive body bias control. Therefore, the fine-grain adaptive V_{DD} control will be more effective for the ultra low voltage logic circuits to reduce the power consumption.

1. Introduction

Very low voltage operation of VLSI's is effective in reducing both dynamic and leakage power. Thus many works have been carried out on the subthreshold operation of circuits [1-3], where the supply voltage (V_{DD}) is less than the threshold voltage (V_{TH}) of transistors. The subthreshold operation of logic circuits is strongly affected by the variation of V_{TH}. However, systematic measurements of the V_{DDmin} of CMOS logic circuits made with scaled devices have not been reported yet.

This paper reports the measured V_{DDmin} variations in CMOS ring oscillators (RO's) in 90 nm technology for the first time. It is shown that V_{DDmin} depends on the number of devices in a circuit block. The measurement results give new insight to the subthreshold logic design especially from the low power DFM point of view, because the design margin of V_{DD} is the critical issue. They also provide a basis for a new approach in characterizing CMOS logic for the very low voltage operation and a guideline to determine the circuit blocks size in fine-grain adaptive body bias and V_{DD} designs.

2. Measured V_{DDmin} of 90-nm CMOS RO's

Figure 1(a) shows the schematic of the proposed RO circuits to enable the V_{DDmin} measurement. The low swing output of RO is amplified to 1-V swing by the output buffer, because both V_{DD2} and V_{SS2} of RO are

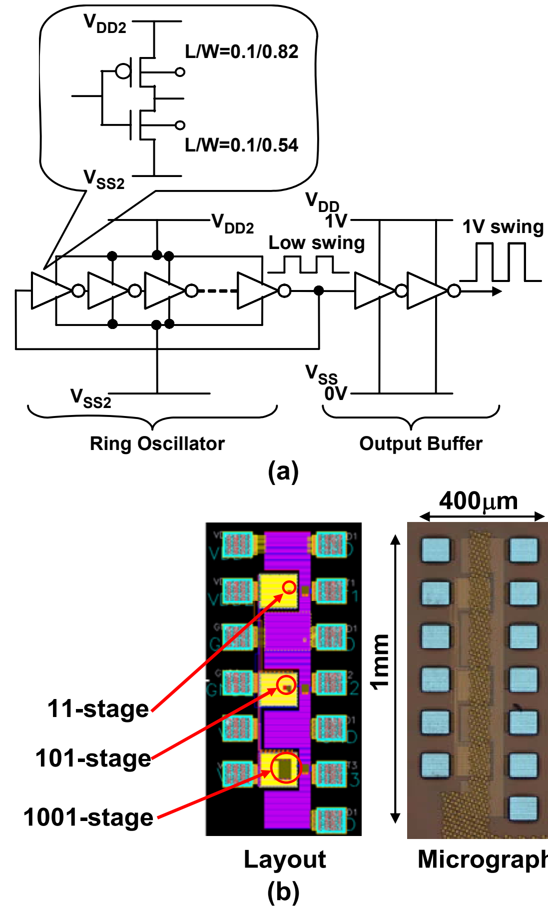

Figure 1. CMOS ring oscillators (RO's). (a) Schematic of the proposed circuits to enable the V_{DDmin} measurement. (b) Layout and micrograph.

separated from the V_{DD} and V_{SS} of the output buffer by the triple well process and V_{SS2} is manually tuned to the optimum input level for the output buffer in the measurement. The inverters in RO have the body bias terminals. Figure 1(b) shows the layout and the micrograph of the chip fabricated with 1 V 90 nm CMOS process.

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The chip has three RO's (11-stage, 101-stage and 1001-stage) and its area is 1000µm×400µm. The smallest size inverter in the primitive cell libraries is used.

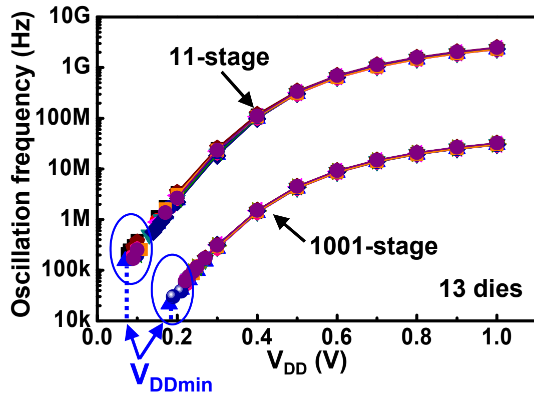

Figure 2. Measured V_{DD} dependence of the oscillation frequency of 11-stage and 1001-stage RO's.

Figure 2 shows the measured V_{DD} dependence of the oscillation frequency of 11-stage and 1001-stage RO's for 13 dies. V_{DDmin} is defined as the supply voltage (= V_{DD2}−V_{SS2}) when the RO's stop oscillation and no voltage transitions from the output buffer are observed, which corresponds to the function errors in logic LSI's. It should be noted that V_{DDmin} of 11-stage RO's is lower than that of 1001-stage RO's.

Figure 3 shows the V_{DD} dependence of the inter-die oscillation frequency variations of 11-stage RO's extracted from Figure 2. When V_{DD} is reduced, the relative frequency variations increase [4] because the relative on-current variations of transistors due to the threshold voltage variations increase. The frequency variations, for example, increase from 3% to 14%, as V_{DD} is reduced from 1 V to 0.2 V. The large variations are one of the most serious issues in the subthreshold logic circuits.

Figure 4 shows the measured distribution of V_{DDmin} of RO's with different number of stages. The lowest V_{DDmin} was 50 mV for the 11-stage RO's. Average V_{DDmin} of 11-stage, 101-stage and 1001-stage RO's were 91mV, 158mV and 224mV, respectively. As the number of stages is increased, V_{DDmin} increase, because V_{DDmin} is determined by the worst inverter(s) in each RO. The results indicate that V_{DDmin} for logic circuits depends on the scale of the circuits and large scale logic circuits have high V_{DDmin}.

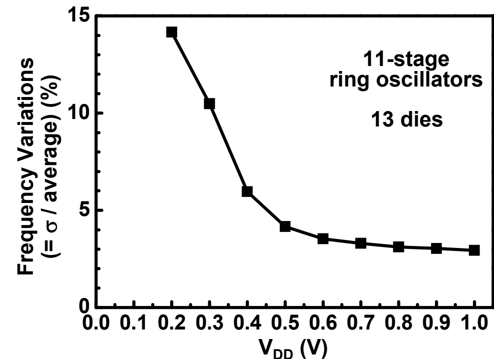

Figure 3. V_{DD} dependence of the inter-die oscillation frequency variations extracted from Figure 2.

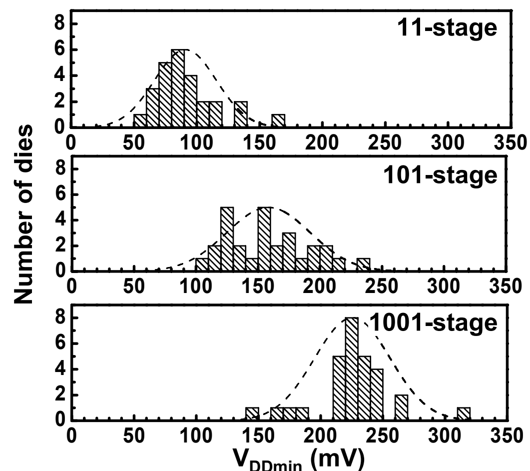

Figure 4. Measured distribution of V_{DDmin} of RO's with different number of stages.

3. Analysis of V_{DDmin} with Monte Carlo Simulations

The V_{DDmin} variations are mainly caused by the intra-die V_{TH} variations. Figure 5(a) shows the measured position dependence of the intra-die V_{TH} of a 4-mm 4000×1 transistor array [5] with the same 90 nm technology. Fourier transform of the Figure 5(a) gives the spatial spectrum shown in Figure 5(b). It doesn't show distinctive peaks at particular spatial frequencies, which indicates that the intra-die V_{TH} variations are not systematic but purely random across 4 mm [5].

The origin of the V_{DDmin} variations is analyzed with Monte Carlo SPICE simulations. Figure 6(b) shows the simulated V_{DDmin} distribution of the 11-stage RO's(Figure 6(a)) where each transistor has random V_{TH} determined from the Pelgrom plot provided by the foundry. Figure 6(c) shows and V_{TH}'s of 22 transistors in the RO with the highest V_{DDmin} in Figure 6(b). The highest V_{DDmin} is caused by a pair of a FS (fast nMOS

and slow pMOS) inverter and a SF (slow nMOS and fast pMOS) inverter as shown in Figure 6(d). When the #10 inverter has the low input, the high output voltage level of the #10 inverter is reduced and the #11 inverter outputs the incorrect high, which stops the RO oscillation.

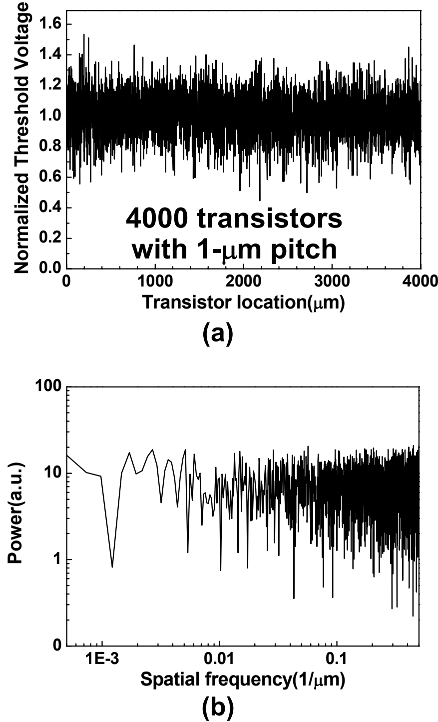

Figure 5. Measured intra-die V_{TH} of a 4000×1 transistor array [5]. (a) Position dependence. (b) Spatial spectrum.

4. Fine-Grain Adaptive Body Bias Control to Reduce V_{DDmin}

A higher V_{DDmin} as the number of stages increases is not acceptable. The fine-grain adaptive body bias control is an effective technique to compensate for the intra-die *systematic* V_{TH} variations [6]. The effectiveness for the intra-die *random* V_{TH} variations, however, is not clear. The required circuit block size for the fine-grain control is also unclear. Therefore, V_{DDmin} has been extracted by simulations for different grain sizes. Figure 7 shows the initial and compensated V_{DDmin} for the 11-stage RO that demonstrates the highest V_{DDmin} in Figure 6(b). The body bias of pMOS is adaptively controlled to minimize V_{DDmin} and the body bias of nMOS is fixed. When a common body bias is applied to the 11 inverters(Figure 7(b)), V_{DDmin} is improved from 89 mV to 87 mV. The V_{DDmin} reduction by common body bias control is also verified by the measurement.

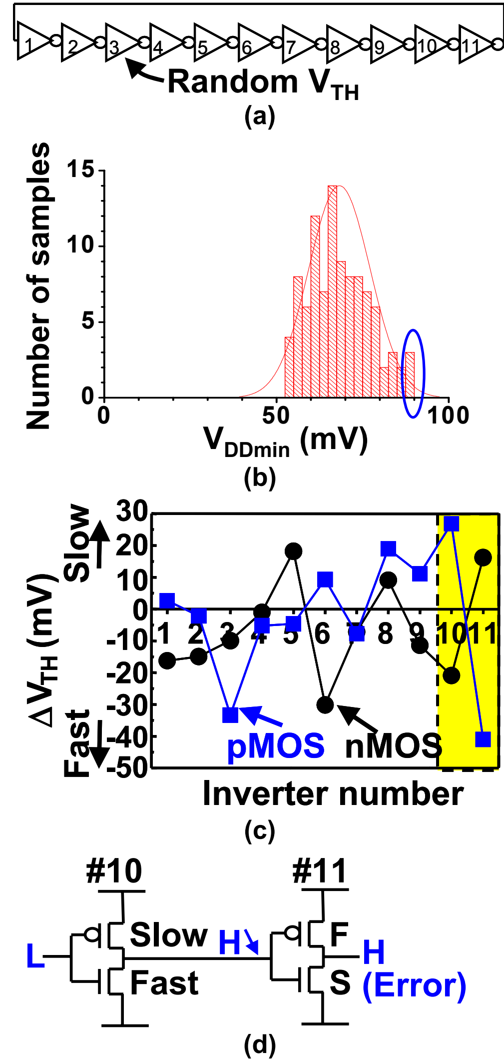

Figure 6. (a) Schematic of the circuit of the 11-stage RO. (b) Simulated V_{DDmin} distribution of the 11-stage RO's where each transistor has random $V_{TH.}$ (c) V_{TH}'s of 22 transistors in the RO with the highest V_{DDmin}. (d) A pair of a FS inverter and a SF inverter that stops the RO operation.

Figure 8 shows the measured V_{DDmin} dependence on the body bias of both nMOS and pMOS for an 11-stage RO. When V_{TH} of nMOS and that of pMOS are balanced, V_{DDmin} is low.

In contrast, when they are unbalanced, V_{DDmin} is high [2-3]. The initial V_{DDmin} is 91mV when both body biases are 0V. Common body bias control allows to reduce V_{DDmin} to 87mV, i.e. by 4mV only. This is coherent with the simulation results and shows that the coarse-grain body bias control is not effective to significantly reduce V_{DDmin}. When independent body bias is applied for every 2 inverters, V_{DDmin} lowers to 85mV as shown in Figure 7(c). In contrast, when inverter-by-inverter body

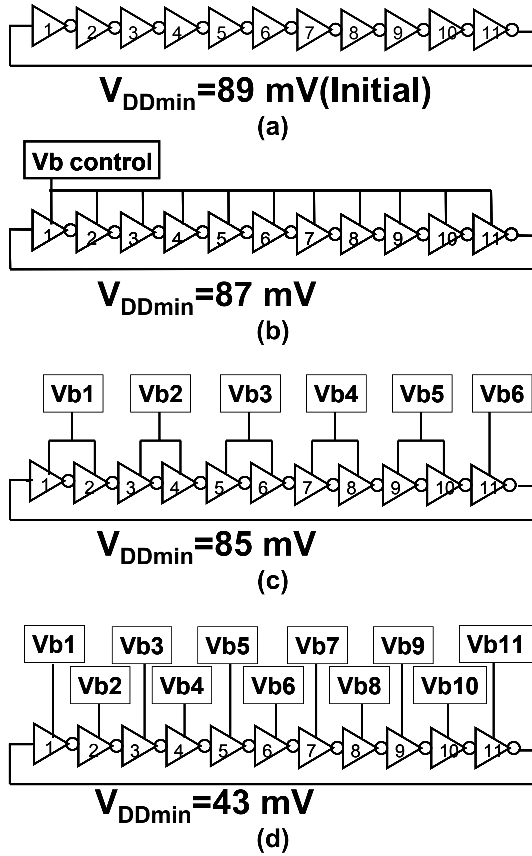

Figure 7. Initial and compensated V_{DDmin} by the various fine-grain adaptive body bias controls for the 11-stage RO. (a) No body bias. (b) Common body bias. (c) Body bias for every 2 inverters. (d) Inverter-by-inverter body bias.

bias is applied, V_{DDmin} is drastically reduced to 43mV as shown in Figure 7(d). Despite the significant improvement, the inverter-by-inverter body bias control is impractical due to large area penalty. Therefore, fine-grain adaptive body bias control is not effective to compensate the intra-die *random* V_{TH} variations in ultra low-voltage logic circuits. Instead, fine-grain adaptive V_{DD} control should be preferred.

5. Conclusions

Subthreshold behavior of RO's in 90-nm CMOS has been investigated. The lowest measured V_{DDmin} was 50 mV for an 11-stage RO. The measured average V_{DDmin} increased from 91mV to 224mV when the number of RO stages increased from 11 to 1001, which hinders the V_{DD} scaling. Lowering V_{DDmin} is difficult, because the compensation of purely random V_{TH} variations would

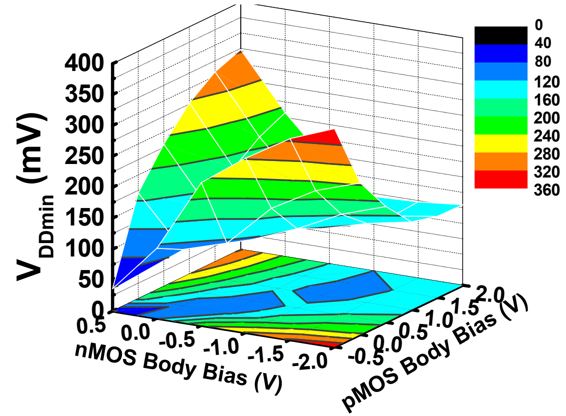

Figure 8. Measured V_{DDmin} dependence of the body bias of both nMOS and pMOS for a 11-stage RO.

require impractical inverter-by-inverter adaptive body bias control. Instead, the fine-grain adaptive V_{DD} control will be more effective for the ultra low voltage logic circuits.

Acknowledgement

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