A Design Methodology of Chip-to-Chip Wireless Power Transmission System

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***Abstract*— A design methodology to transmit power using a chip-to-chip wireless interface is proposed. The proposed power transmission system is based on magnetic coupling, and the power transmission of 5mW/mm^2 was verified. The transmission efficiency trade-off with the received power is also discussed.**

I. Introduction

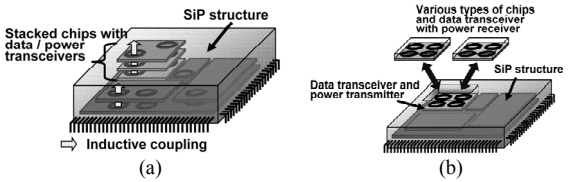
A System-in-a-Package (SiP) is getting a major 3D integration approach in recent years. For data communication among stacked chips in SiP's, wireless data transmission technologies have been investigated for high speed, low power and low cost [1]. Power delivery in these systems, however, is not wireless and is based on bonding. Then, it is difficult to get two stacked chips close, since the bonding needs several hundred microns separation between chips. One solution is to skew the stacked chips but this is difficult if the upper chip should be connected in the middle of the lower chip and is covered by the topmost chip.

If the power is supplied wirelessly, the chips can be stacked closely and the wireless data transmission performance will be increased, since the data bandwidth and communication reliability increases as the chip-to-chip distance is decreased in wireless data communication. The cost is also decreased due to the elimination of mechanical bonding. Furthermore, chip detachability can also be achieved by combining the wireless data and power transmission. This opens up a totally new system customization scheme after the fabrication as we sometimes change a daughter board for system upgrade. Fig.1 illustrates the proposed concepts.

II. Test Circuit

A. Circuit Topology

Fig.2 shows the circuit diagram of the proposed system. The lower chip includes a transmitter circuit and an on-chip planar inductor L_1 whose outer diameter is 700μm for magnetic field generation. The transmitter circuit generates an RF signal from the DC supply voltage V_{DD} and activates L_1. The power is transmitted by magnetic fields rather than radio waves. The upper chip includes an on-chip planar inductor L_2, a full-wave rectifier circuit using MOSFET-based diodes and a smoothing capacitor.



(a) (b)

Fig. 1. Concept of chip-to-chip wireless power transmission (a) assisting wireless interchip communication and (b) for system modification after fabrication.

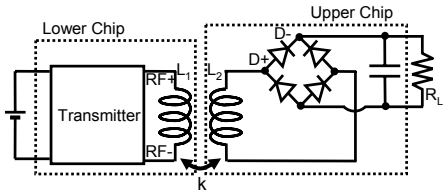
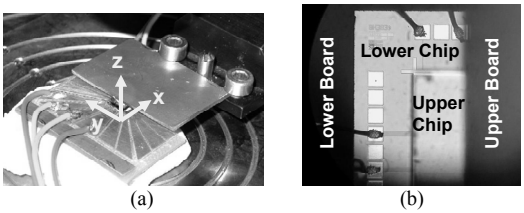


Fig. 2. Circuit diagram of proposed system.



(a) (b)

Fig. 3. (a) Whole image and (b) closeup view of measurement setup.

B. Simulation and Measurement Results

The system shown in Fig.2 was designed in 0.35-μm CMOS and fabricated. Fig.3 shows the measurement setup. The lower (upper) chip is mounted on the lower (upper) board and the two chips gets closer together face-to-face. Fig.4 shows the simulated and measured received power dependence on output DC voltage. In this implementation, L_1=1.0nH, L_2=9.3nH and the oscillation frequency is set to f_{TX}= 330MHz for this graph. Output voltage is varied by changing DC output load R_L. The peak transmitted power 2.5mW which equals to 5mW/mm^2 is observed when R_L is 100Ω, which is the equivalent source resistance of the wireless power source. Fig.5 show the measured output voltage dependence on Δx and Δy, and Δz when the load is open which equals to R_L=∞.

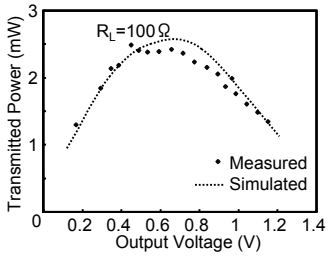


Fig. 4. Transmitted power dependence on output voltage.

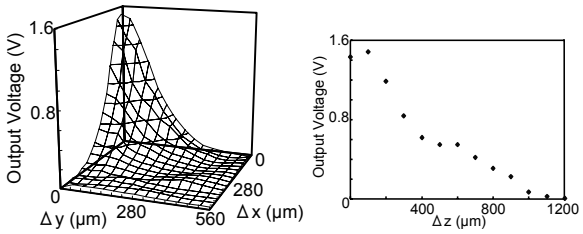


Fig. 5. Output voltage dependence on Δx and Δy, and Δz.

III. CIRCUIT OPTIMIZATION

A. Circuit Model

Although the feasibility of the wireless power delivery system is demonstrated in the previous sections, it is preferable to increase the transmittable power and to maximize the power efficiency to further increase the variety of applications. Improvement can be achieved by adding resonance capacitors C_1 and C_2 as shown in the equivalent circuit model in Fig.6 (a). R_S represents parasitic resistances of transmitter interconnections and driving transistors which equals to the internal impedance of the transmitter. R_1 and R_2 indicate series resistances of L_1 and L_2 respectively. Capacitances C_1 and C_2 resonate with L_1 serially and with L_2 in parallel respectively. R_{L_AC} relates to the equivalent total impedance of the rectifier, the smoothing capacitor and the DC load resistance R_{L_DC}. R_{L_AC} was shown to be approximated as follows when the rectifier is ideal and the smoothing capacitor is large enough [2].

$$R_{L\_AC} \approx \frac{R_{L\_DC}}{2}. \tag{1}$$

Here, we assume the transmitted power is high (if not maximized) when transmitter circuit is in resonance. That is, C_1 is expressed as follows. Although this condition does not give the optimum condition, the resultant transmitted power is at least achievable.

$$C_1 = \frac{1}{4\pi^2 f_{TX}^2 L_1}. \tag{2}$$

On the other hand, C_2 resonates under the following condition and the circuit model can be converted to a simple resistance model as shown in Fig.6 (b).

$$4\pi^2 f_{TX}^2 R_{L\_AC}^2 L_2 C_2^2 - R_{L\_AC}^2 C_2 + L_2 = 0. \tag{3}$$

R_X and R_Y are the transformed impedances of R_2 and R_L. In this system, high power efficiency is as important as the transmitted power to increase the variety of applications. The power transmission efficiency for R_Y is maximized when

$$R_Y = R_X \sqrt{\frac{R_S + R_1}{R_S + R_1 + R_X}}. \tag{4}$$

In case of on-chip planar inductors, the relationship between R_N and L_N is approximated as $\zeta = L_N/R_N$ with ζ being a technology parameter because both R_N and L_N are roughly proportional to the square of turns. The optimum values of C_2 and R_{L_AC} are calculated as functions of k, f_{TX}, ζ, R_S, R_1, R_2 by using formulas (3) and (4). Fig.7 shows the calculated transmitted power and power efficiency η when f_{TX}=900MHz,

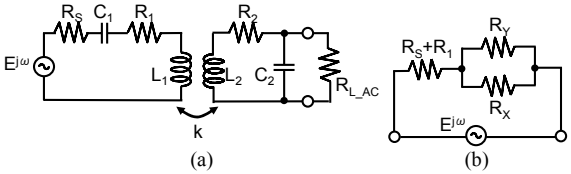


Fig. 6. (a) Simplified circuit model and (b) equivalent circuit under resonance condition.

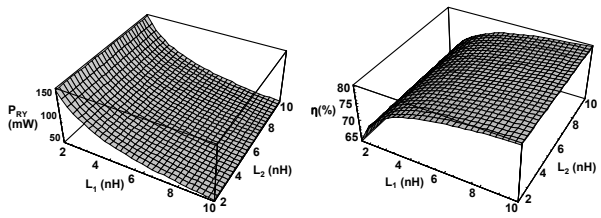


Fig. 7. Calculated (a) received power and (b) efficiency dependence on L_1 and L_2.

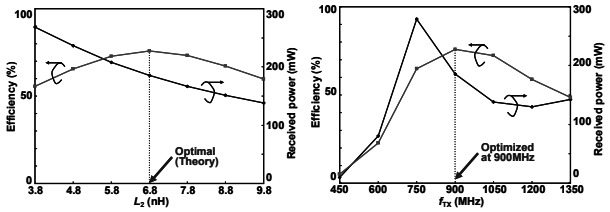


Fig. 8. Simulated results on received power and efficiency when (a) L_2 and (b) f_{TX} are varied.

k=0.75 and ζ=2.6×10-9 and R_S=2 assuming 90-nm CMOS technology with input voltage of 2.5V. In this design region, the power efficiency improves as the value of L_1 increases although the transmitted power degrades. On the other hand, both the power efficiency and the transmitted power are independent of the value of L_2. To verify the optimization theory, two types of simulations were performed. Fig.8 shows the simulated results on received power and power efficiency using HSPICE around the theoretically optimal values of L_2 and f_{TX}. In both cases, the optimal values correspond well with the simulated results.

IV. CONCLUSIONS

In summary, a chip-to-chip 5mW/mm^2 wireless power transmission system was demonstrated by 0.35-μm CMOS technology. Maximization of the power efficiency is also discussed.

ACKNOWLEDGMENT

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[2] G.A.Kendir, Liu Wentai, Wang Guoxing, M.Sivaprakasam, R.Bashirullah, M.S.Humayun, J.D.Weiland, *IEEE Transactions on Circuits and Systems I* Volume 52, Issue 5, May 2005.

A Design Methodology of Chip-to-Chip Wireless Power Transmission System

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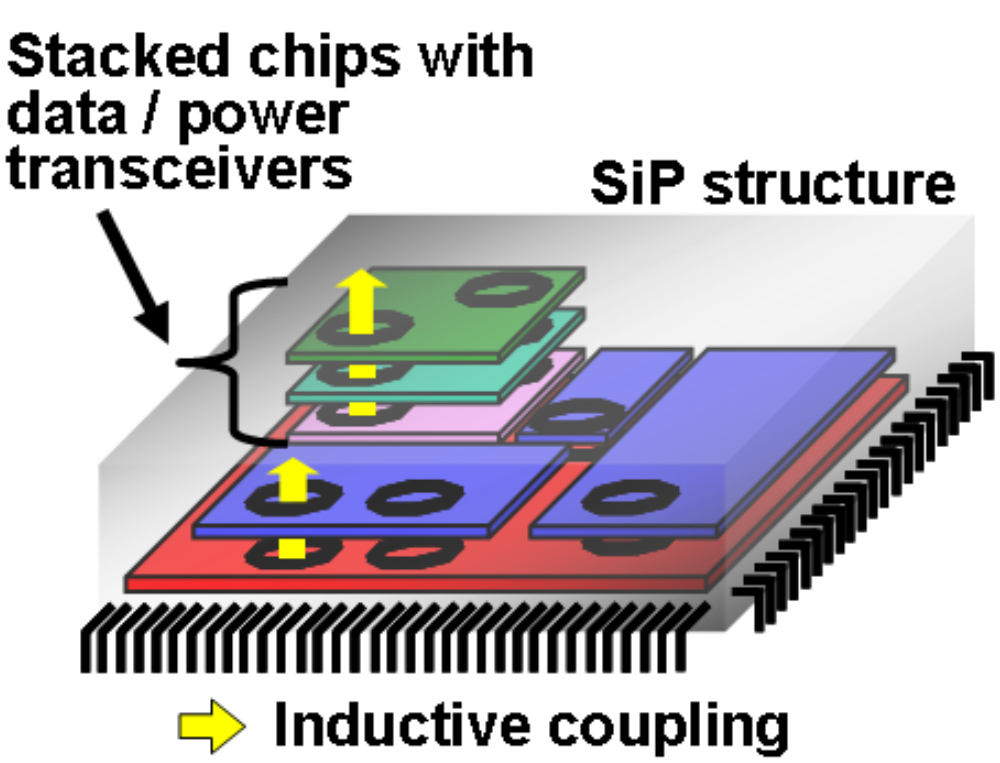
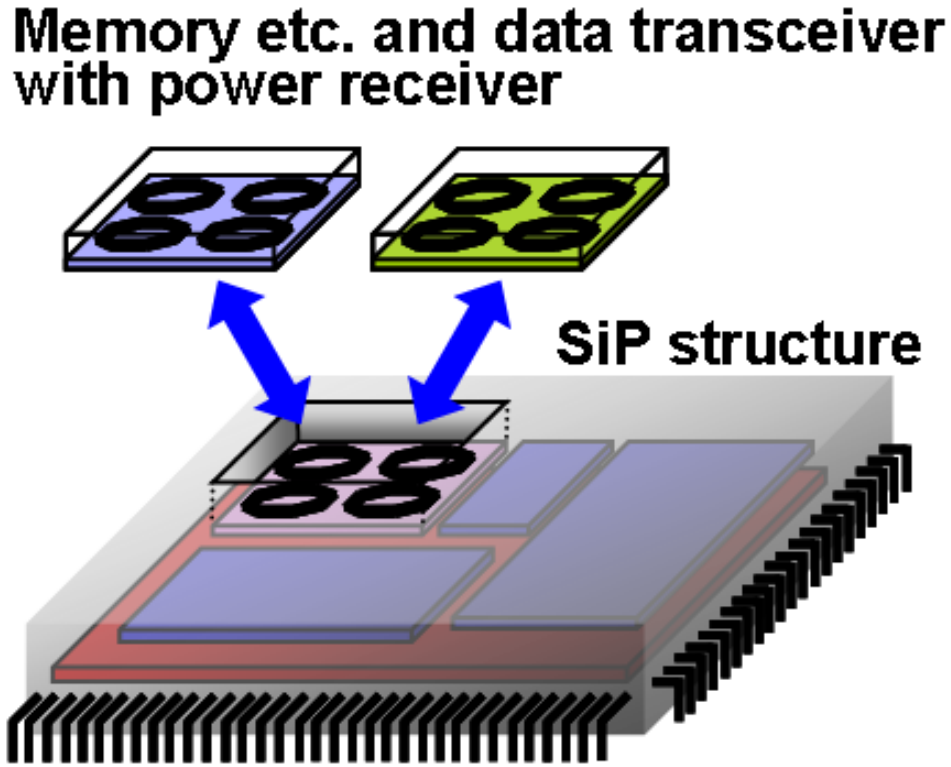
Wireless power transmission over chips

Assisting wireless data link

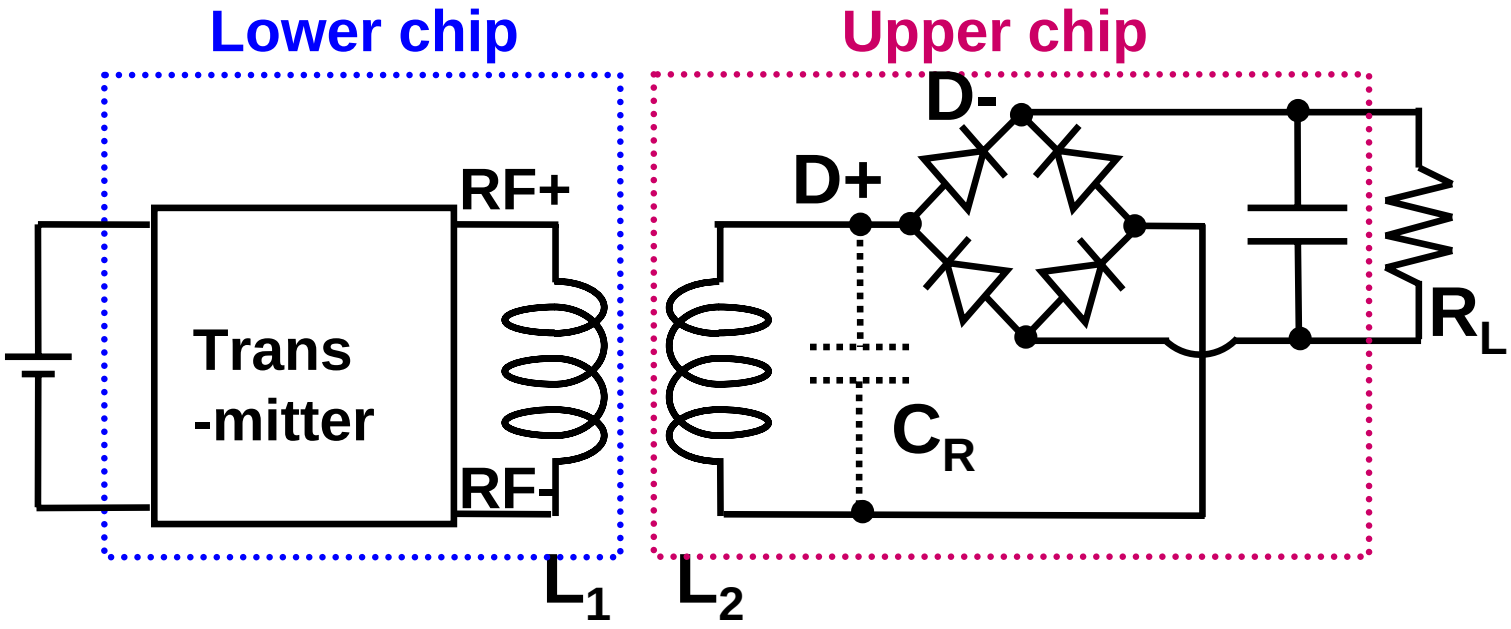


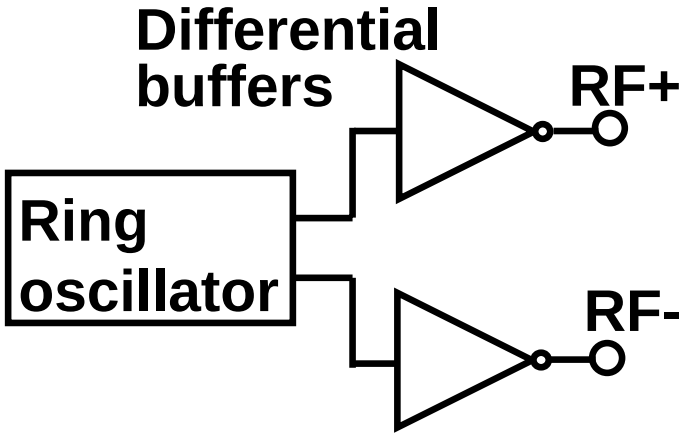
Slip-on structure



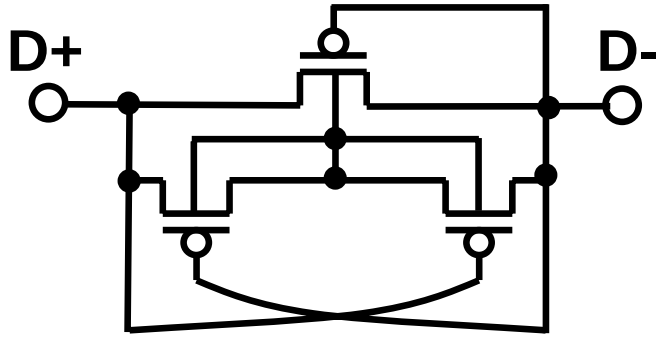
- Improvement in assembly flexibility & data link performance
- Detachable structure for system upgrade by users

Circuit implementation (pulse-based)



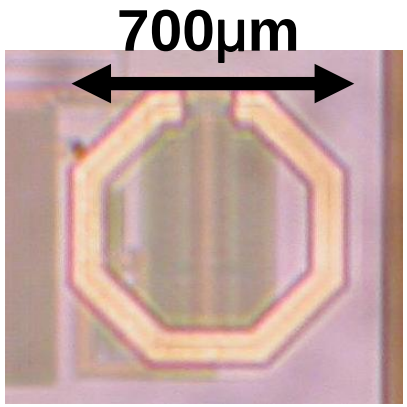


Transmitter



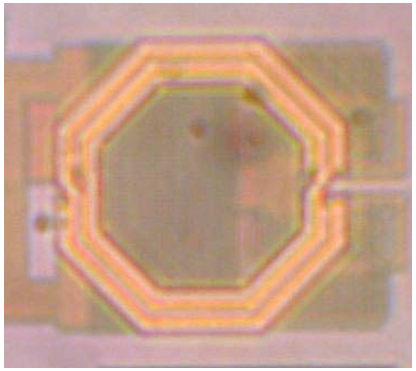
Rectifier unit

Fabricated chip & measurement setup



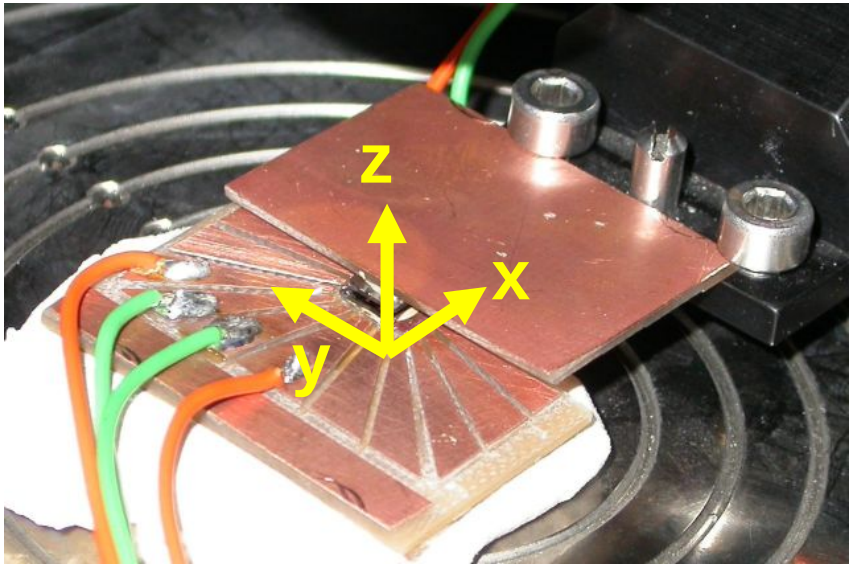
Lower chip
(Transmitter)

L_1=1.0nH

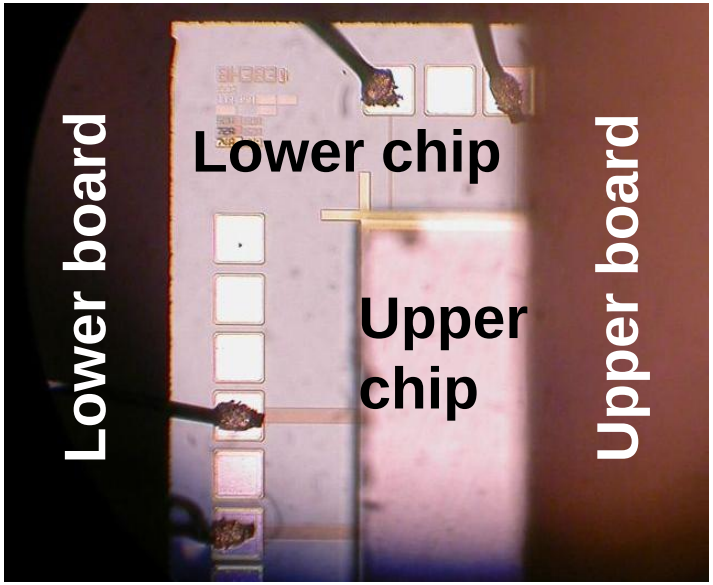


Upper chip
(Receiver)

L_2=9.3nH



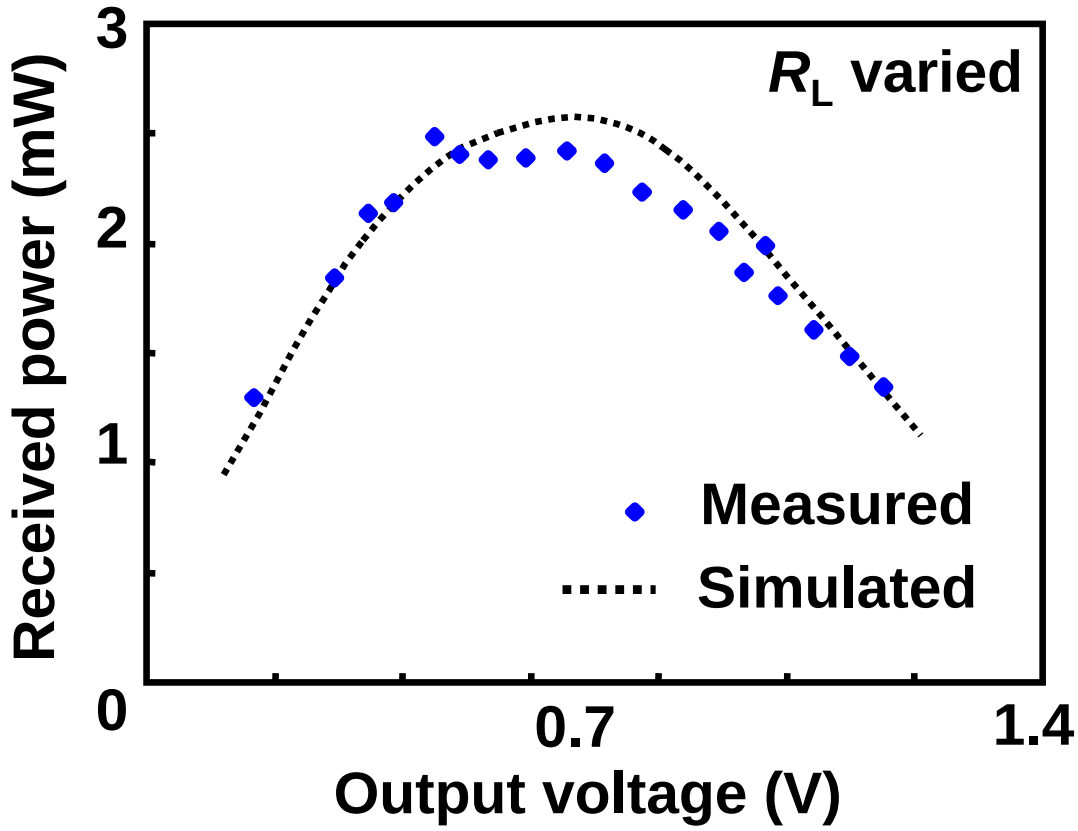
Whole setup



Close-up view

Measured results

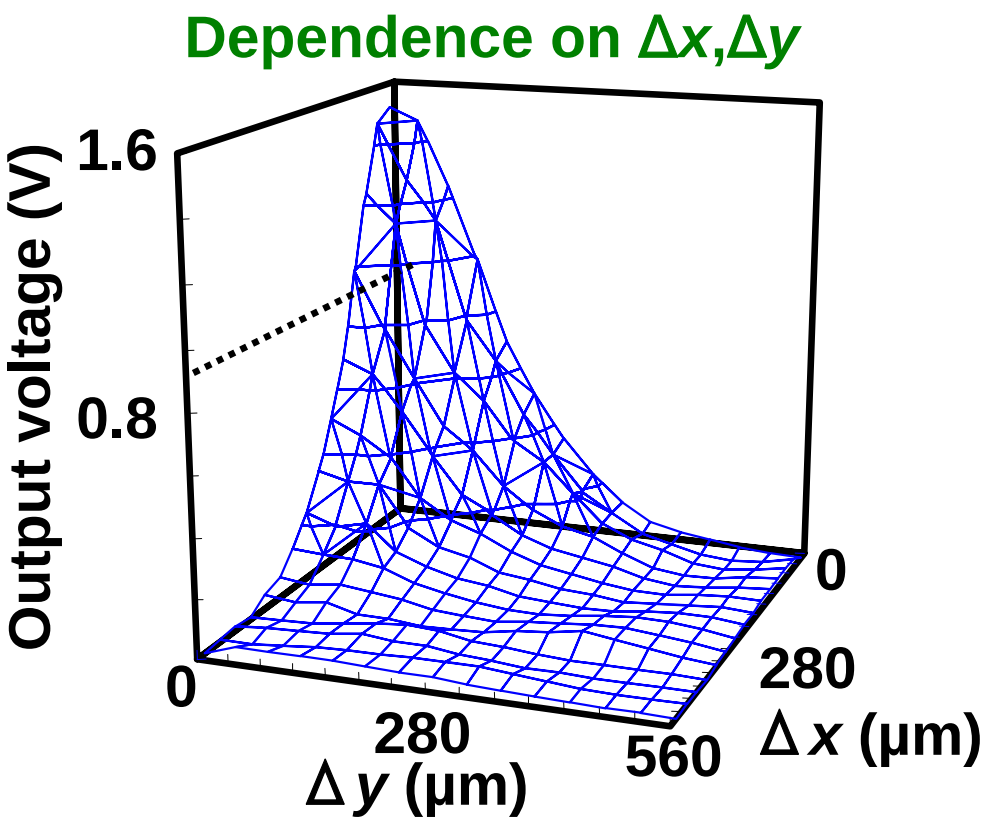
350nm 1P3M CMOS for TX/RX, f_{TX}=330MHz

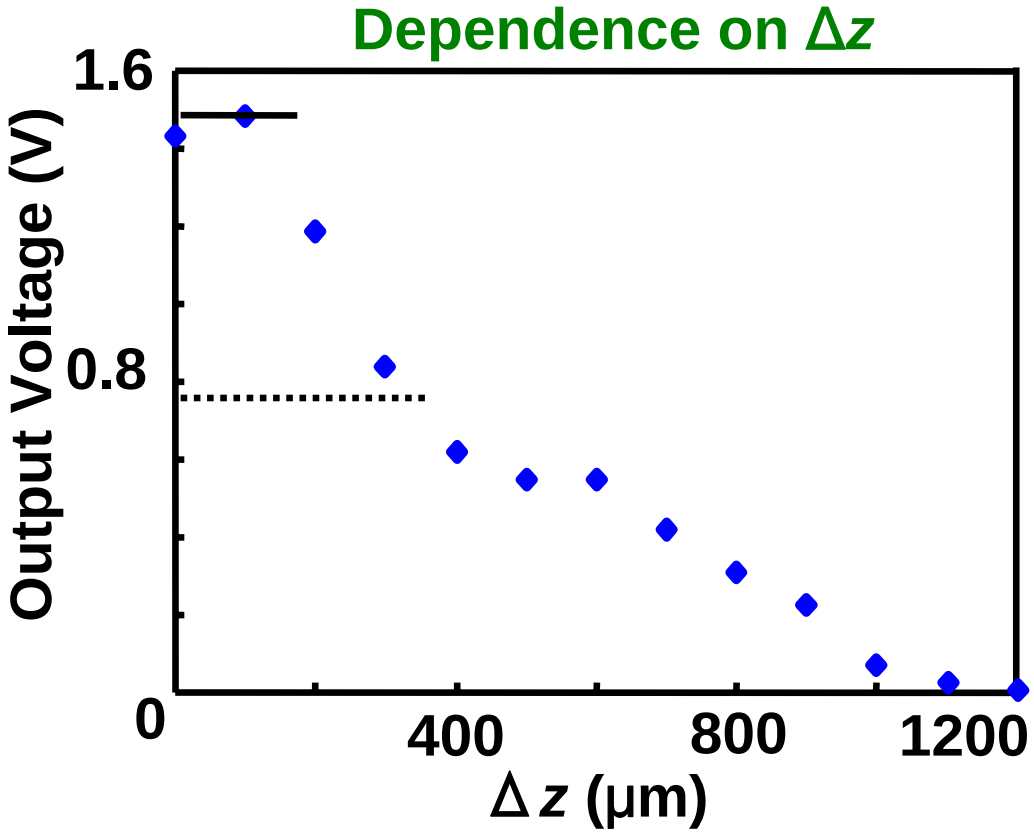


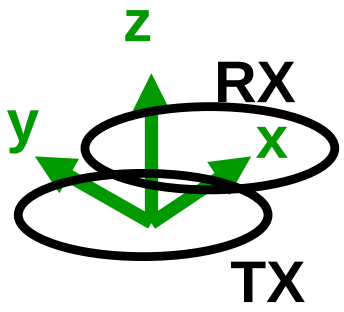
Maximum transmitted power: 2.5mW (5mW/mm²)

when V_{out}=0.5V, R_L=100, z=0

Alignment error tolerance





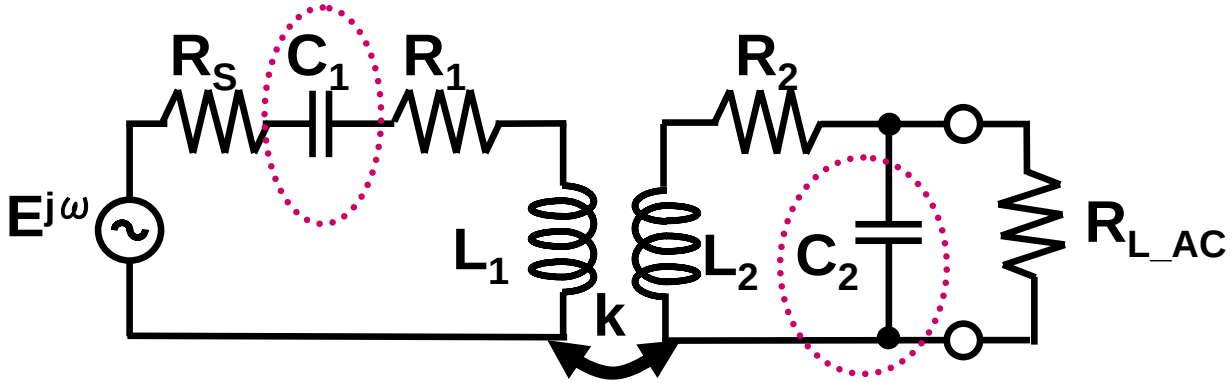


- Measurement results when $R_L=\infty$
- Half value breadth
  $\begin{cases} \Delta x, \Delta y < 200\mu m \\ \Delta z < 300\mu m \end{cases}$

[P5] K. Onizuka, H. Kawaguchi, M. Takamiya, and T. Sakurai, IEEE CICC, 2006.

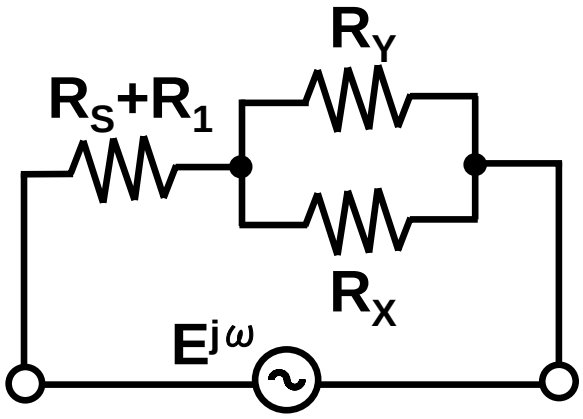
Introducing resonance capacitors

- For higher received power, transmission efficiency



C_1,C_2: Resonance capacitors
R_S,R_1,R_2: Parasitic resistances of transmitter, L_1 and L_2
R_{L_AC}: Equivalent load resistance including rectifier

Under resonance condition



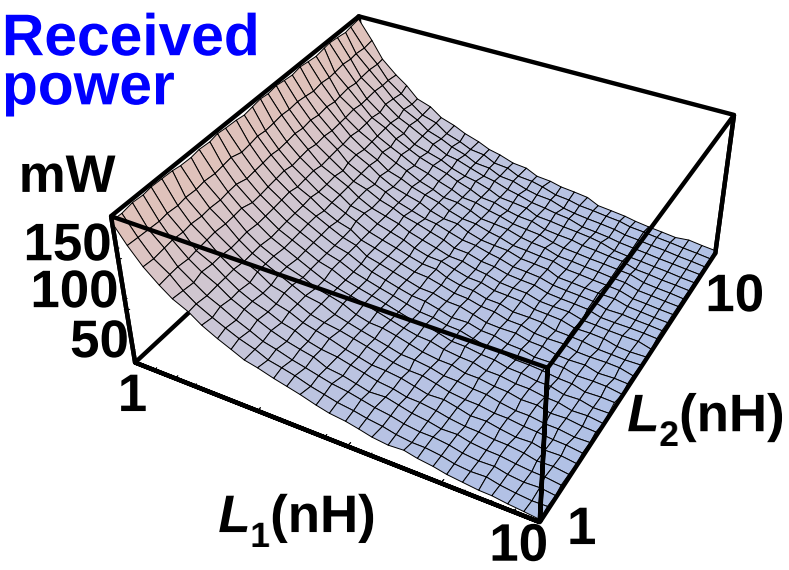
- R_X and R_Y: Functions of R_2 and R_{L_AC}
- When power efficiency maximized:

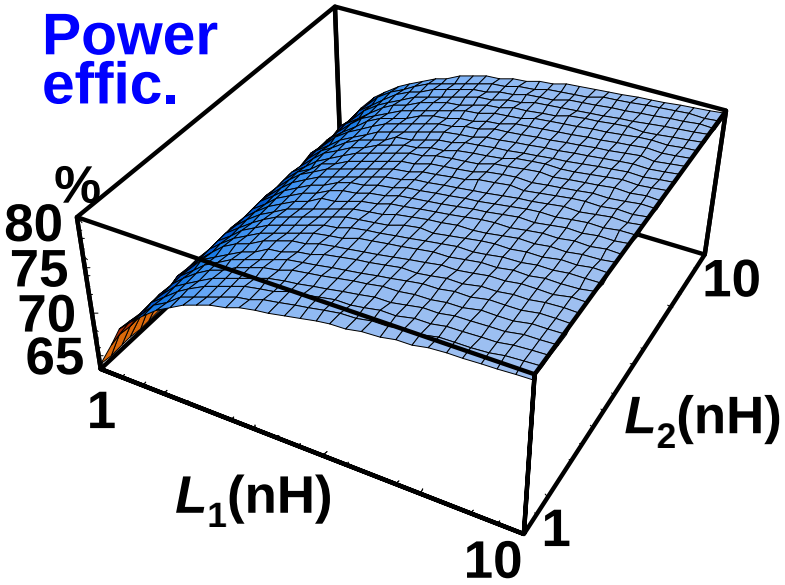
$$R_Y = R_X \sqrt{\frac{R_S + R_1}{R_S + R_1 + R_X}}\,.$$

[P6] K. Onizuka, H. Kawaguchi, M. Takamiya, and T. Sakurai, IEEE ICICDT, 2007(Invited).

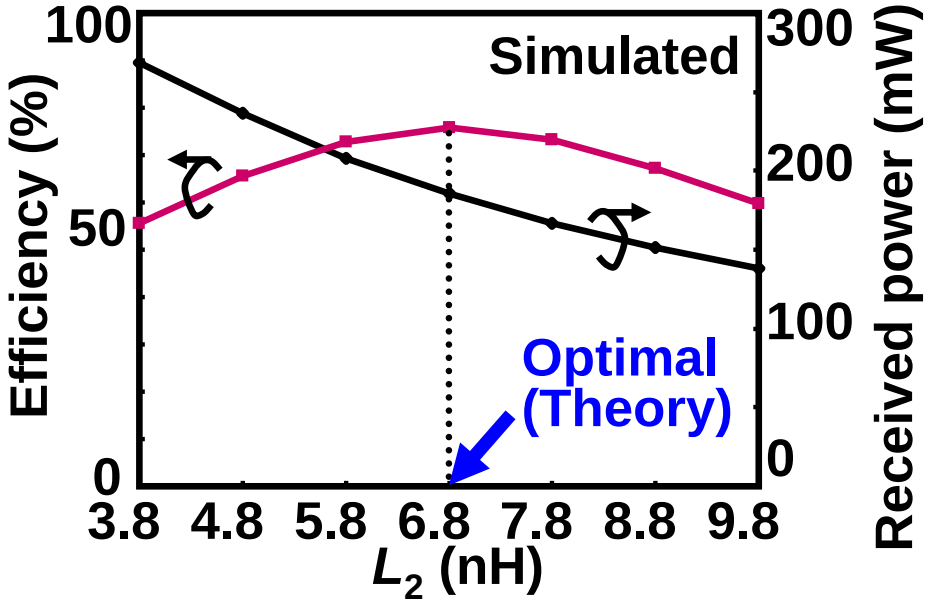
Optimization & verification

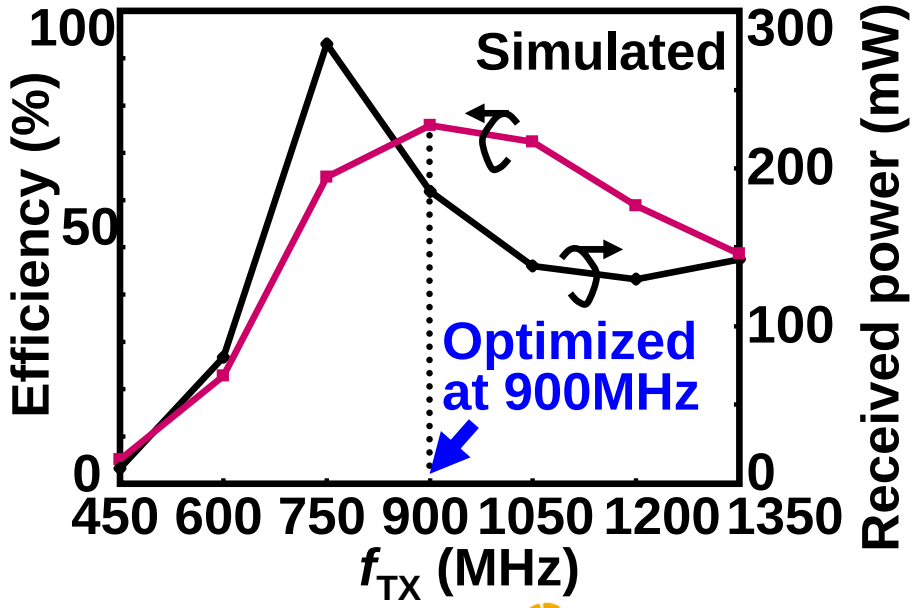
Theoretical calculation when
τ_L=2.6×10^{-9},
R_S=2.0,
V_{DD}=2.5V,
f_{TX}=900MHz,
k =0.75.





- L_1 ➔ Power and efficiency balancing, L_2 ➔ Voltage adjustment





Summary

- First-time wireless power transmission over chips
- Received power 2.5mW/0.5mm^2 measured
- Optimal design methodologies on power & efficiency derived
- Received power up to 100mW-order/mm^2 estimated