3D-Structured On-Chip Buck Converter for Distributed Power Supply System in SiPs

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***Abstract*— An on-chip buck converter with 3D chip stacking is proposed and the operation is experimentally verified. The manufactured converter achieves a maximum power efficiency of 62% for an output current of 70mA with a switching frequency of 200MHz and a 2x2mm on-chip LC output filter in 0.35μm CMOS. The use of glass epoxy interposer to increase the maximum power efficiency up to 71.3%, and the power efficiency dependence on the filter inductor are also discussed.**

I. INTRODUCTION

Recently System-on-a-Chip (SoC) and System-in-a-Package (SiP) are getting more and more interest as major integration technologies. They are often used to integrate various types of circuit blocks from processors and memories to analog circuits. Each block demonstrates a different optimum supply voltage (V_{DD}) and the difference tends to increase as the technology scales. For example, memory and analog circuits tend to prefer higher voltage compared with logic blocks. Fig.1 shows the V_{DD} trends for precision analog/RF, performance analog/RF, high performance logic and low-power logic with the design rule trends according to the International Technology Roadmap for Semiconductors (ITRS) 2006 Update [1]. Multiple-V_{DD} implementation is therefore required in low-power and high-performance systems. Moreover, supply voltage is sometimes tuned in time to achieve lower power consumption, which is called dynamic voltage scaling. The supply of many different and dynamically scaled voltages from outside the package gives rise to much overhead in area. The power line integrity, including IR drop and noise, becomes an issue as well. The distributed on-chip power supply circuits are useful for solving these problems. The concept of the distributed power supply is shown in Fig.2. High voltage is distributed by a main power grid and is then converted to the lower voltages at the vicinity of the target blocks by distributed on-chip voltage converters. This approach reduces cost and power integrity issues.

For DC-DC converters, linear regulator, buck converters and switched capacitor converter are well known circuits. A buck converter requires large passive elements of inductance and capacitance (LC) for an output filter but it shows a higher power efficiency than a linear regulator. A switched capacitor converter also needs large capacitors and one more drawback is that the output voltage levels are limited by the ratios of prepared capacitors. That is not very suitable for low-power dynamic voltage scaling systems.

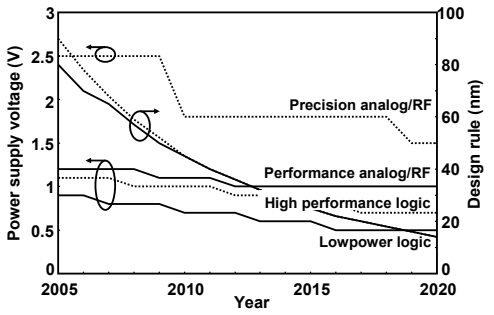

Fig. 1. Supply voltage trend with design rule trend according to ITRS.

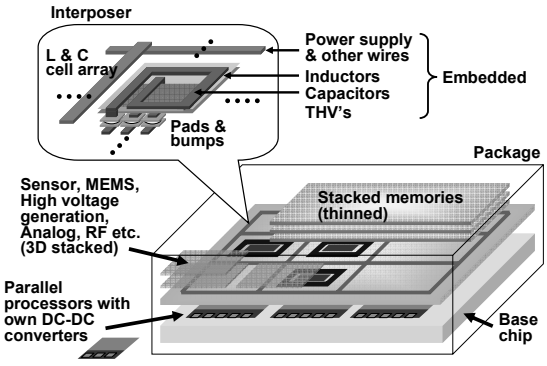

Fig. 2. Concept of distributed power supply system.

In case of the buck converter, high switching frequency is preferable for smaller L and C but the power efficiency is degraded by the dynamic power dissipated by switching transistors at high frequency. Low quality factor (Q) of air-core and on-chip inductors also degrades the power efficiency. High inductance is good for high Q but is not easy to obtain on a chip because of the area limitation and even if high magnetic permeability material is introduced on a chip, high-μ property is usually lost at high frequency. A couple of integrated buck converters have been reported in recent years however, they are to be sought through, focusing on cost issues and package friendliness.

II. POWER EFFICIENCY ANALYSIS

A. Circuit Model

In order to implement on-chip buck converters for on-chip power supply systems, the two following conditions should be met. First, all elements of the converter must be integrated at least in a package. Secondly, the implementation cost per one voltage domain must be minimized while maintaining high

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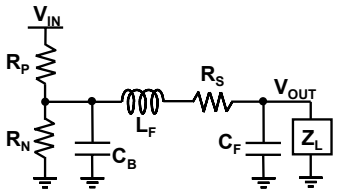

Fig. 3. Simple circuit model of buck converter including parasitic elements.

power efficiency. To maximize the power efficiency, the power loss must be minimized. The major components of power loss are classified into three parts: dynamic switching loss of the switching transistors, resistive loss of the switching transistors and the resistive loss of the inductor as shown in Fig.3 [2].

The theoretical maximum power efficiency is derived as formula (1) [3].

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} = \frac{V_{IN} D I_L}{V_{IN} D I_L + V_{IN} I_L^3 \sqrt{24 \frac{R_0 C_0}{\tau_L} D(1-D)}} = \frac{1}{1 + \alpha \tau_L^{-1/3}}. \quad (1)$$

where

$$R_0 C_0 = \left(\sqrt{D R_P C_P} + \sqrt{(1-D) R_N C_N} \right)^2, \quad (2)$$

$$\tau_L = \frac{L}{R_S}. \quad (3)$$

Here, P_{OUT} and P_{LOSS} represent the output power and the total power loss. D denotes the duty cycle which equals to V_{OUT}/V_{IN} where V_{IN} and V_{OUT} are input and output voltages. I_L signifies the load (output) current. α is a function of R_0C_0 and D, and can be a constant when the process technology and D are fixed. C_P, C_N, R_P, and R_N represent parasitic capacitances and parasitic series resistances per unit gate length of PMOS (high-side) and NMOS (low-side) switching transistors. τ_L is a figure of merit of the output filter inductor, L and R_S being whose inductance and parasitic series resistance.

B. Efficiency Dependence on Technology

As seen from (1), the smaller R_0C_0 and the larger τ_L are better for higher power efficiency. R_0C_0 is shown to be roughly proportional to the product of effective conduction resistance and effective switched capacitance per unit gate width of switching transistors. They reduce as the process technology scales down. Fig.4 shows the calculation results of the maximum power efficiency dependence on D and process technology (90, 130, 180, 350-nm CMOS) when τ_L=10ns which is a nominal value for on-chip planar inductors. It would be better to use the most scaled transistors for high conversion efficiency.

For planar inductors, the maximum τ_L is fixed and mainly determined by the metal thickness. The thicker the metal layer is, the larger the maximum τ_L is. Fig.5 shows the calculation results of the maximum power efficiency dependence on τ_L in several duty cycles assuming 90nm CMOS technology. Especially when D is small, it is valuable to use an inductor whose τ_L is large. In case of an on-chip inductor, the maximum value of τ_L is roughly 10ns independent of the process technology. On the other hand, the values of τ_L larger than 100ns are achievable by applying interposers with thick metal layers. Thus the inductor is not necessarily fabricated by using the most advanced technology which is expensive.

In addition to the inductor, fabrication cost of on-chip MOS capacitor per unit capacitance increases as technology scales.

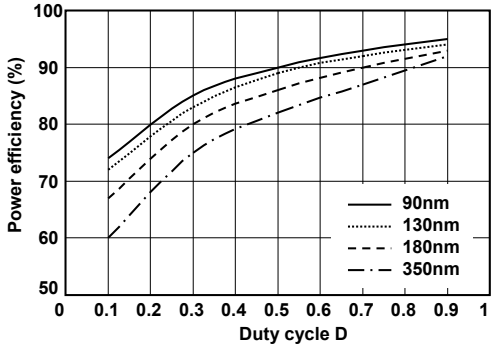

Fig. 4. Maximum power efficiency dependence on D and process technology.

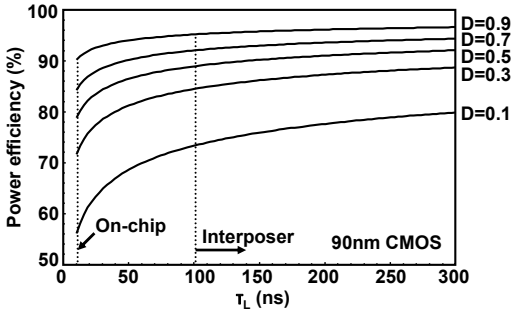

Fig. 5. Maximum power efficiency dependence on τ_L in several duty cycles.

III. Circuit Implementations

A. "Two Chips" Implementation

According to the discussions in the previous section, it is reasonable to implement active elements and output filter on separate die whose process technologies are different. By stacking two chips face-to-face and connecting them via metal bumps, a buck converter for on-chip distributed power supply systems can be fabricated in a well balanced manner for best cost and power tradeoff. To demonstrate the feasibility of the stacked-chip buck converter, an on-chip buck converter is designed in 0.35-μm CMOS for upper and lower chips. The lower chip could be manufactured by 90-nm or more advanced technology for the higher efficiency but this test chip is to show the feasibility of the stacked-chip approach. Fig.6 shows the circuit diagram of the test converter.

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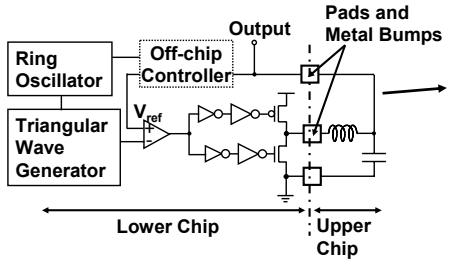


Fig. 6. Test circuit diagram of stacked-chip implementation of buck converter.

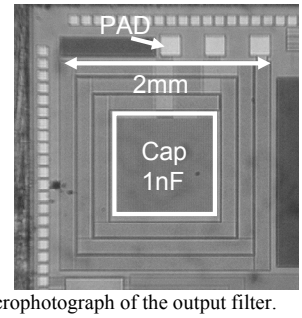
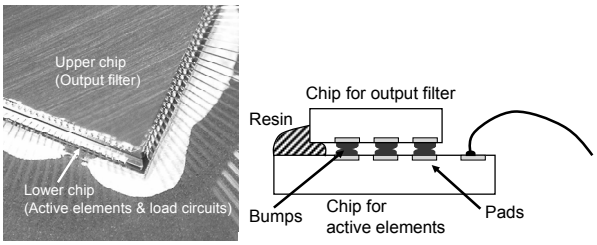


Fig. 7. Chip microphotograph of the output filter.



(a) (b)

Fig. 8. (a) 3D-structred buck converter and (b) its cross-sectional diagram.

The buck converter with the stacked-chip implementation was fabricated and measured. Fig.7 shows the chip microphotograph of the output filter on the upper chip. The outer diameter of the filter equals to that of the filter inductor d_{OUT}, which is set at 2x2mm by assuming that 10mm-square chip can have 25 voltage domains. 6.8x6.9mm chip with 7 voltage domains has already been presented [4].

The inductance is estimated by a simple formula from [5] and the calculated value in this work is 22nH when the sheet resistance is about 0.02Ω/□. The open space at the center of the inductor is filled with a MOS capacitor for the output filter. Area efficiency is more important than linearity for the filter capacitor, because the output voltage does not change dynamically in a normal operation. From that aspect, MOS capacitor is more suitable than any other types of on-chip capacitors like Metal-Insulator-Metal (MIM) capacitor or polysilicon capacitor. The obtained capacitance is about 1nF. Under those conditions, the switching frequency was chosen to 200MHz. The gate widths of the switching transistors were optimized at I_L=60mA.

Fig.8 shows the measurement setup and its cross-sectional diagram. The pad size and the effective bump diameter of this experimental setup are 200x200μm and 150μm, respectively. Micro bumps whose diameter is 30μm and whose resistance is as low as 14mΩ/bump have been realized in industry environments [6] and can be used instead for further smaller area.

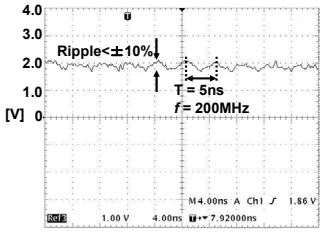


Fig. 9. Output voltage waveform for V_{OUT}=1.86V and I_L=60mA.

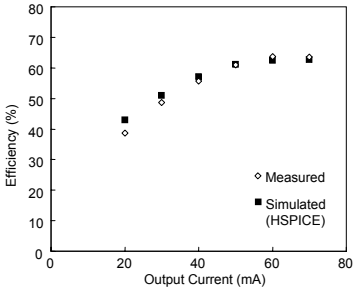


Fig. 10. Simulated and measured power efficiency for V_{OUT}=2.3V and f=200MHz.

The output waveform in Fig.9 shows V_{OUT}=1.86V at I_L=60mA. The measured voltage ripple is smaller than ±10%. Fig.10 shows the simulated and measured power efficiency with V_{OUT}=2.3V for an output current range from 20mA to 70mA. The maximum efficiency of 62% is achieved for 70mA output current. The measurement results compare well with the HSPICE simulation results. The simulation considers all the parasitic elements including the inductor parasitic resistance of 2.5Ω, and the inductor input-to-ground capacitance of 25pF.

B. "Two Chips + Interposer" Implementation

In order to further increase the efficiency, it is effective to use inductors whose τ_L is higher than that of the previous inductors. A thin-film inductor surrounded by magnetic core material as proposed in [7] can be a solution but is expensive. Implementing the inductor on a glass epoxy interposer is an effective yet inexpensive solution.

The structure shown in Fig.11 is assembled using a newly introduced interposer and the same lower and upper chips presented in the first half of this section. In this implementation, only a capacitor is used on the upper chip.

Fig.12 shows an inductor array on generic Flame Resistant 4 (FR-4) glass epoxy interposer with two metal layers. The circled inductor in the array, which achieved the minimum metal spacing in the trial manufacture, is used for the measurement. The metal thickness on the interposer is 30μm, the substrate thickness is 100μm, and the diameter of the through-hole via is 100μm. This implementation increases τ_L by 30 times compared with the case of an on-chip inductor. The outer diameter of the inductor is increased by 10% to achieve the same value of on-chip inductance because the minimum spacing of metal lands on glass epoxy is larger than that of on-chip interconnects. The permittivity of the glass epoxy is

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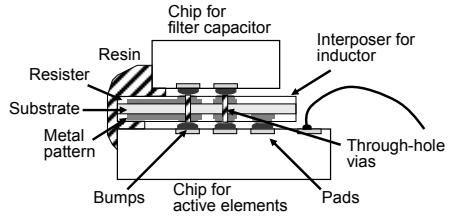

Fig. 11. Cross-sectional diagram of "two chips + interposer" implementation.

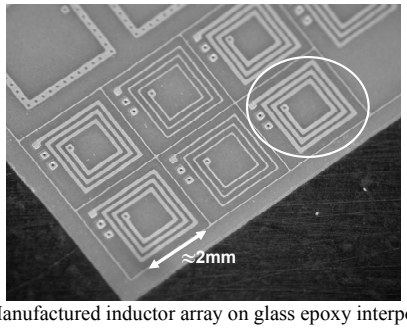

Fig. 12. Manufactured inductor array on glass epoxy interposer.

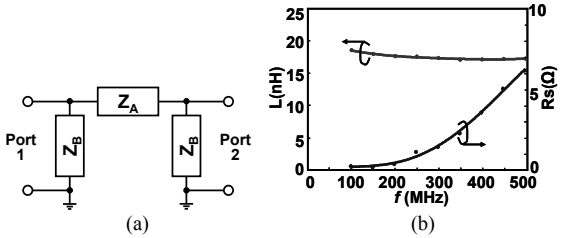

Fig. 13. (a) Equivalent model for inductance and resistance extraction (b) Measured inductance and resistance of fabricated inductor.

generally more than four times higher than SiO_2, however, the parasitic capacitance between both sides of the interposer can be negligible. That is because the substrate thickness is large enough compared with the line width. S-parameters of the fabricated inductor were measured using a test element group and a network analyzer. Fig. 13 (a) shows the equivalent model to extract the inductance and the parasitic series resistance of the inductor from the measured S-parameters. Fig.13 (b) shows the extracted characteristics of the inductor using formula (4).

$$Z_A = ReZ_A + j\,ImZ_A = R_S + j\omega L. \tag{4}$$

Measured inductance and τ_L were 18nH and 100ns at 200MHz, respectively. The value of τ_L at DC is more than 20 times larger than that of the previous on-chip inductor. The parasitic resistance increases rapidly because of skin effect in the high frequency region over 200MHz however, the characteristics below 200MHz are important in this application. The skin depth of the metal wire at 500MHz is assumed to be smaller than 3μm. The inductance decreases gradually as frequency increases, because of the current concentration caused by skin effect.

Fig.14 shows the comparison of measured power efficiency between two types of implementations of "two chips" and "two chips + interposer" for V_{IN}=3.3V and V_{OUT}=2.3V.

The power efficiency with the glass epoxy inductor is

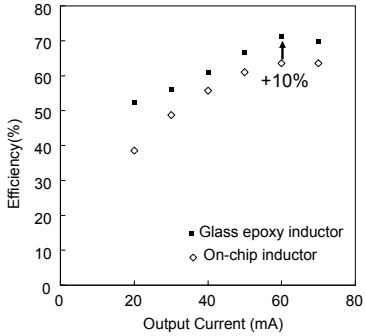

Fig. 14. Measured efficiency comparison between two types of implementations.

improved by 5-14% depending on the output current compared with the on-chip implementation. The maximum power efficiency of 71.3% is achieved at an output current of 60mA. The possible reason that the efficiency does not improve the most at 60mA, is that the switching transistors are not changed optimally according to the τ_L characteristic of newly implemented inductor.

IV. Conclusions

An on-chip buck converter with stacked-chip implementation which is suitable for low-cost low-power distributed power supply systems has been designed and fabricated for the first time. The switching frequency is optimized and chosen to be 200MHz. 62% power efficiency is measured for an output current of 70mA, which verifies the feasibility of this approach. By utilizing a glass epoxy interposer for a filter inductor, it is shown by experiment that the power efficiency can be increased to 71.3%.

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