A 100Mbps, 0.41mW, DC-960MHz Band Impulse UWB Transceiver in 90nm CMOS

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Abstract

A low power impulse ultra-wideband (UWB) transceiver for DC-960MHz band is proposed in this paper. It features a digital pulse-shaping transmitter, a DC power-free pulse discriminator and an error-recovery phase-frequency detector. The developed transceiver in 90nm CMOS achieves the lowest energy consumption of 2.2pJ/bit (TX) and 1.9pJ/bit (RX) at 100Mbps.

Introduction

UWB communication systems can be broadly classified as impulse UWB and multi-carrier UWB. For the impulse UWB, multi-user detectors (MUD) and hybrid RAKE/MUD-UWB transceivers for robust narrowband interference suppression are becoming popular. However, a simple, single clocked-correlator transceiver [1] or threshold detector [2] can also be used for short distance and high SNR environments.

In this paper a novel DC-960MHz impulse UWB transceiver [2, 3] is proposed for the low power ad-hoc wireless sensor networks. These ubiquitous networks require that the individual nodes are tiny, easily integratable into the environment, and have negligible cost. The proposed transceiver features a digital pulse-shaping transmitter, a DC power-free pulse discriminator and an error-recovery phase-frequency detector (PFD), thereby achieving extremely low power consumption at 100Mbps.

Digital Pulse-Shaping Transmitter

Digital pulse shaping in UWB transmitters (TX's) is a power efficient technique. All the previously reported digitally pulse shaped TX's [4-7], however, were developed for above-3GHz band and no TX for DC-960MHz band has been reported. Fig. 1(a) shows the proposed digital pulse-shaping TX. The TX generates the FCC-compliant first derivative Gaussian pulse with multi-drivers. Fig. 1(b) shows the operation principle of TX. Sequentially operated 8 drivers shape a pulse. The 32-tap delay line determines the timing for the drivers. Fig. 2 shows the reason why the pulse shaping with multi-drivers is required for the DC-960MHz band. The conventional TX's with a single driver per pulse do not pass the FCC mask, because the pulse width of the DC-960MHz band is long. In contrast, the developed pulse shaping with 8 drivers satisfies the FCC mask.

Receiver with DC Power-Free Pulse Discriminator

An ultra low-power solution for BPSK demodulation is leading edge detection (LED) technique [2]. The LED receiver (RX) sets a threshold at the receiver, and any incoming pulse that crosses the threshold is detected and demodulated. The proposed asynchronous threshold detector is shown in Fig. 3. It consists of four blocks: a front-end amplifier, a DC power-free pulse discriminator, an error-recovery PFD and a Reset-Set Flip-Flop (RSFF). The received signal is first amplified by the front-end amplifier and each BPSK symbol is split into two pulses V_0 and V_1 by the DC power-free pulse discriminator. Then the first incoming edge of the two pulses is detected by the PFD and the RSFF converts the detection result to the corresponding data bit.

Conventionally, an amplifier and a comparator can be used as the threshold detector. The major disadvantage of this topology is large DC power dissipation that occurs even for no AC input. In the transmitted BPSK signal, the circuit spends long periods of time with no AC signal. Power dissipated in these periods is wasted. The operation principle of the proposed DC power-free pulse discriminator is shown in Fig. 4(a). Two unbalanced inverter InvH and InvL are employed to detect the positive pulse and negative pulse respectively. To tune the threshold of the pulse discriminator, variable bias voltages V_L for the source input of the top inverter and V_H for the bottom inverter are used. As shown in Fig. 4(b), the proposed pulse discriminator has essentially zero power dissipation for no AC input.

A spurious-free PFD [8] is used to avoid simultaneous high input to the RSFF. One problem with this topology is that the bit error in the previous cycle due to signal distortion will be carried over to the subsequent cycles. To remove the error propagation, in the proposed error-recovery PFD shown in Fig.5, an additional RESET signal is fed back to the PFD input after certain time-delay in every cycle. Fig. 6 shows the simulation results for the data "10100" with and without the error-recovery circuit.

Experimental Results

Both TX and RX without the front-end amplifier were designed and fabricated in 90nm CMOS process. The micrograph is shown in Fig. 7. Fig. 8 shows the measured waveform and spectrum of TX output at 100Mbps, which satisfies the FCC mask. Fig. 9 shows the measured waveforms of RX. The potential error propagation due to distorted signal "1" is blocked by the error-recovery RESET signal. The measured BER and RX power dependence on data rate at different bias voltage are shown in Fig. 10. The bias voltage can tune the tradeoff between the sensitivity and power. DC power-free pulse discriminator enables the data rate dependent power. Table I summaries the performance of the whole chip. The developed transceiver consumes 220μW (TX) and 190μW (RX) at 100Mbps. Fig. 11 shows the comparison with the state-of-art UWB transceivers. Both TX and RX achieved the lowest energy per bit.

Conclusions

The transceiver in 90nm CMOS achieves the lowest energy consumption of 2.2pJ/bit (TX) and 1.9pJ/bit (RX without the front-end amplifier) at 100Mbps.

Acknowledgment

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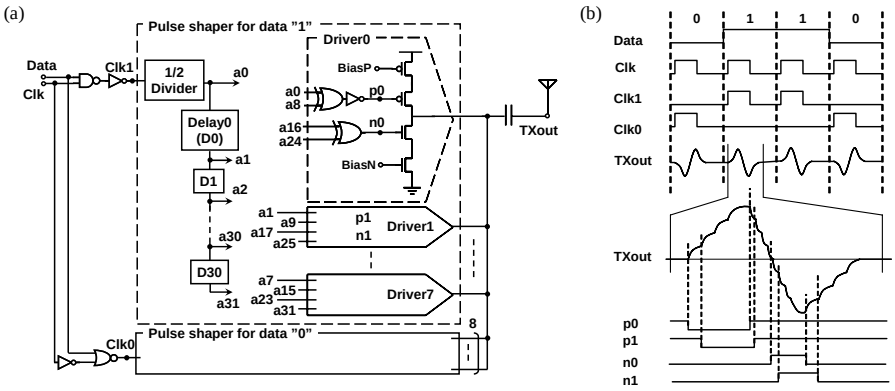


Fig. 1. Proposed digital pulse-shaping TX: (a) Architecture. (b) Timing chart.

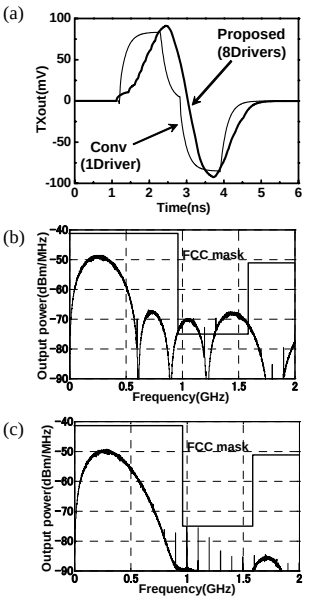


Fig. 2. Simulated TX output. (a) Waveforms. (b) Conv. TX with single driver. (c) Proposed TX with 8 drivers.

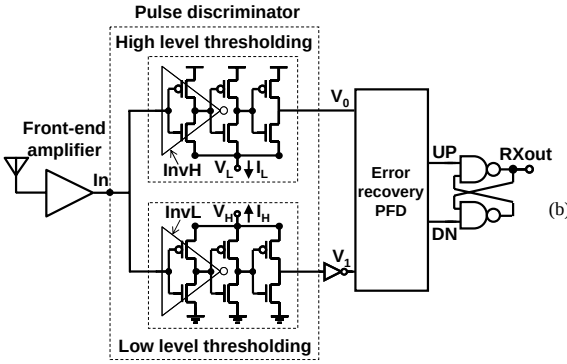


Fig. 3 Proposed RX with DC power-free pulse discriminator.

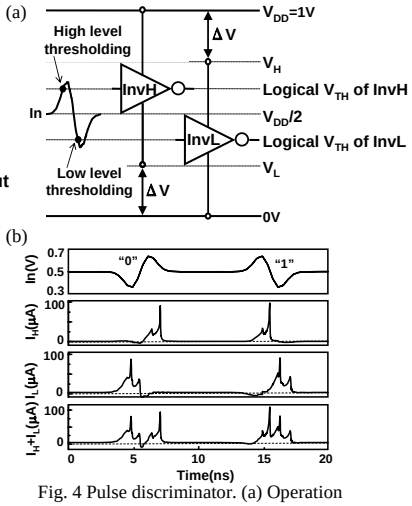


Fig. 4 Pulse discriminator. (a) Operation principle. (b) Simulated waveforms.

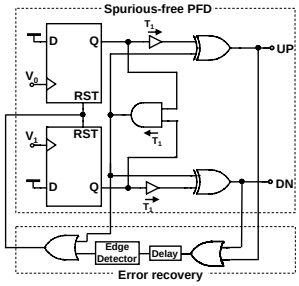


Fig. 5 Error-recovery PFD.

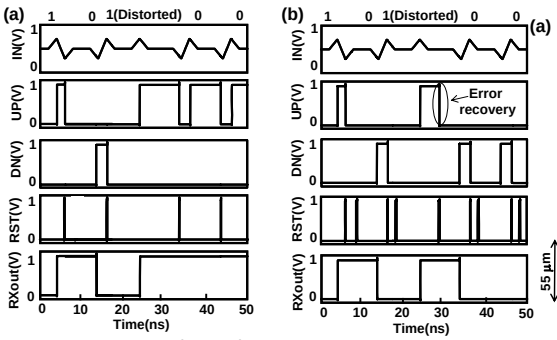
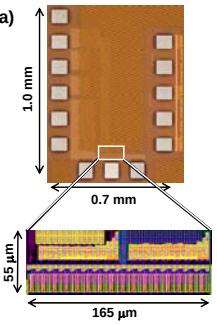


Fig. 6 Simulated waveforms of PFD. (a) Without error-recovery reset. (b) With error-recovery reset.



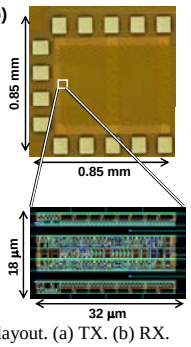


Fig. 7 Chip micrographs and layout. (a) TX. (b) RX.

Table. I Performance summary.

Technology		90nmCMOS
Supply Voltage		1.0V
Data Rate		100Mbps
Power@ 100Mbps	TX	220μW
	RX	190μW
Energy per bit	TX	2.2pJ/bit
	RX	1.9pJ/bit
Core Area	TX	55μm×165μm
	RX	18μm×32μm
Modulation		BPSK

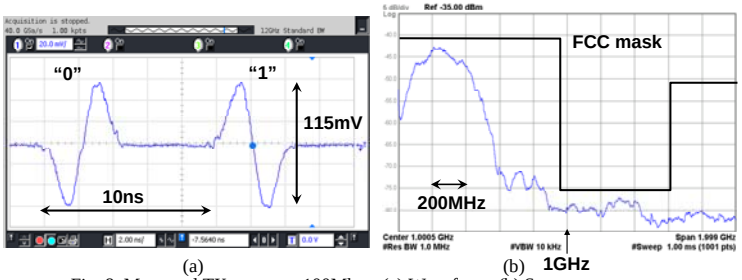


Fig. 8. Measured TX output at 100Mbps. (a) Waveform. (b) Spectrum.

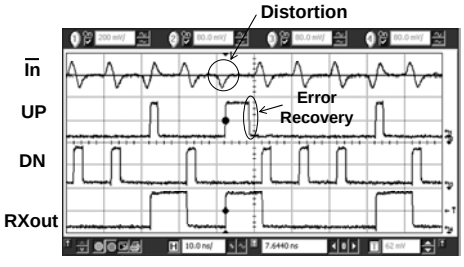


Fig. 9 Measured RX waveforms for distorted data "10100".

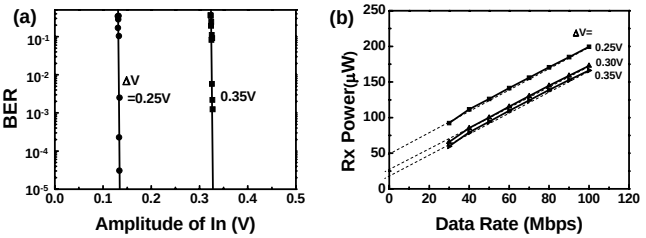


Fig. 10 Measured RX characteristics. (a) BER vs. In. (b) Power vs. data rate.

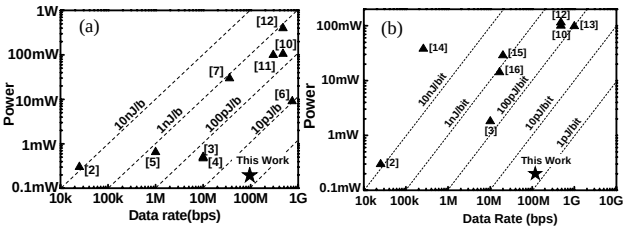


Fig. 11 Comparison with the published UWB transceivers. (a) TX. (b) RX.