Increasing Minimum Operating Voltage (V_{DDmin}) with Number of CMOS Logic Gates and Experimental Verification with up to 1Mega-Stage Ring Oscillators

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ABSTRACT
In order to explore the feasibility of the large scale subthreshold logic circuits and to clarify the lower limit of supply voltage (V_{DD}) for logic circuits, the dependence of minimum operating voltage (V_{DDmin}) of CMOS logic gates on the number of stages, gate types and gate width is systematically measured with 90-nm CMOS ring oscillators (RO's). The measured average V_{DDmin} of inverter RO's increased from 90 mV to 343 mV when the number of RO stages increased from 11 to 1Mega, which indicates the difficulty of the V_{DD} scaling in the large scale subthreshold logic circuits. The dependence of V_{DDmin} on the number of stages is calculated with the subthreshold current model with random threshold voltage (V_{TH}) variations and compared with the measured results, which confirm the tendency of the measurement.

Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]: General

General Terms
Measurement, Performance, Design, Reliability, Experimentation.

Keywords
Minimum operating voltage, subthreshold, logic, variations

1. INTRODUCTION
Very low voltage operation of VLSI's is effective in reducing both dynamic and leakage power and the maximum energy efficiency is achieved at low V_{DD} (e.g. 320mV [1]). Thus many works have been carried out on the subthreshold operation of logic circuits [1, 3-6] and SRAM's [2], where V_{DD} is less than V_{TH} of transistors. However, the number of transistors of the previously reported subthreshold circuits is small (e.g. 70k transistor logic circuits at V_{DD} of 230mV [1], a 32kbit SRAM at V_{DD} of 160mV [2], and a 1000 stage inverter chain at V_{DD} of 60mV [5]), and the possibility of the mega gate scale subthreshold circuits is not clear.

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V_{DDmin} is the minimum power supply voltage when the circuits operates without function errors. RO's are useful V_{DDmin} detectors [7], because RO's stop oscillation when the first function error in the logic circuits happens. Figure 1 shows simulated waveform of 5-stage CMOS inverter RO. V_{DD} is varied from 0.2V to 0V. At V_{DDmin} of 50mV, RO stops oscillation. In order to emulate the recent SoC's, the mega stage scale RO's are required, because the recent SoC's have 10M-100M logic gates. With the technology scaling and the increased number of transistors on a chip, V_{DDmin} will increase, because the more gates there are, the more likely it is that the worst-case condition will occur, and thus a higher V_{DD} will be required. However, the systematic measurements of the V_{DDmin} of the subthreshold logic circuits made with scaled devices have not been reported yet.

This paper reports the systematically measured dependence of V_{DDmin} of CMOS logic gates on the number of stages, gate types and gate width with 90-nm CMOS RO's for the first time in order to explore the feasibility of the large scale subthreshold logic circuits and to clarify the lower limit of V_{DD} for logic circuits.

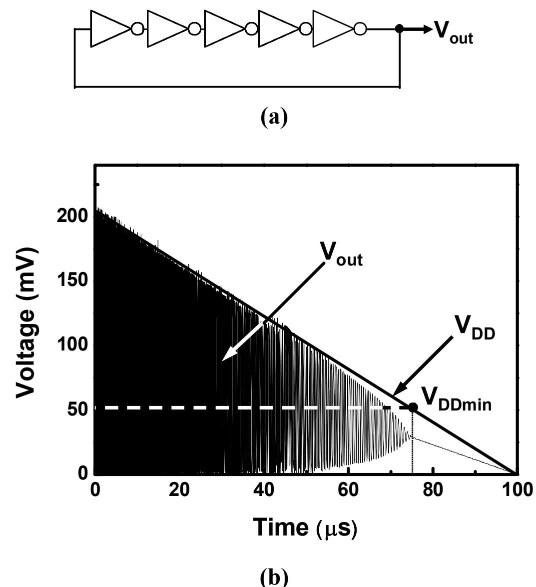


Figure 1. Simulated waveform of 5-stage CMOS inverter RO. Definition of V_{DDmin} is shown.

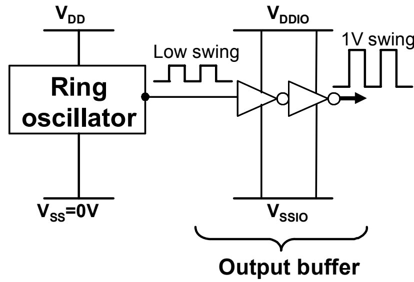


Figure 2. Proposed RO circuits to enable the V_{DDmin} measurement.

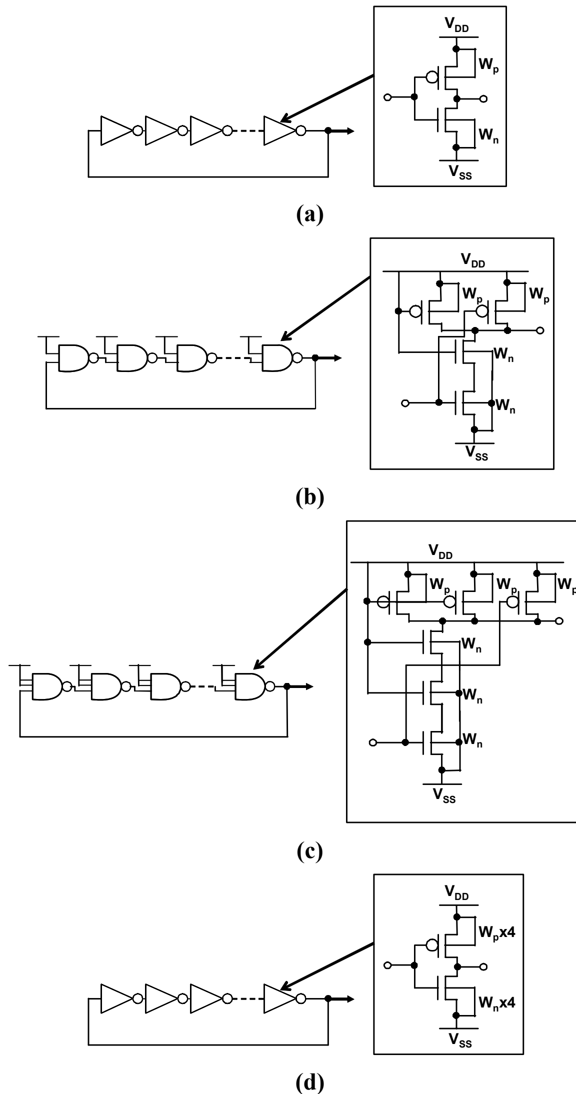


Figure 3. Fabricated RO circuits with varied number of stages. (a) Inverter RO, (b) 2NAND RO, (c) 3NAND RO, (d) x4 inverter RO.

Section 2 presents the design of CMOS RO's for V_{DDmin} measurement and the measured V_{DDmin}. Section 3 presents the analysis of the origin of V_{DDmin} with SPICE and MATLAB to explain the measured results.

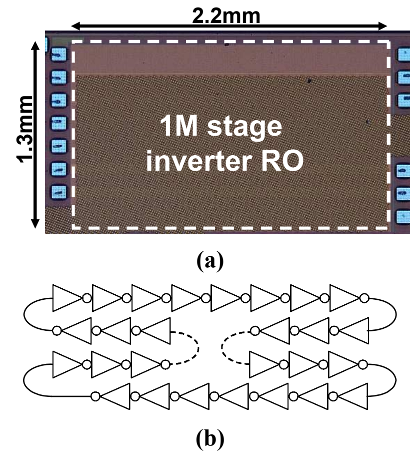


Figure 4. (a) Micrograph of a 1M-stage inverter RO. (b) Layout style of RO's.

2. MEASURED V_{DDmin} of 90-nm CMOS RO's

2.1 Design of CMOS RO's for V_{DDmin} Measurement

Figure 2 shows the schematic of the proposed RO circuits to enable the V_{DDmin} measurement. The low swing output of RO is amplified to 1-V swing by the output buffer, because both V_{DD} and V_{SS} of RO are separated from the V_{DDIO} and V_{SSIO} of the output buffer by the triple well and V_{SS} is manually tuned to the optimum input level for the output buffer in the measurement. V_{DDmin} is defined as the supply voltage (= V_{DD}−V_{SS}) when the RO's stop oscillation and no voltage transitions from the output buffer are observed, which corresponds to the function errors in logic LSI's.

Figure 3 shows the schematic of fabricated RO circuits with varied number of stages. RO's include three different logic gates (inverter, 2NAND and 3NAND) and two inverters with different gate width. The standard primitive cells are used for the logic gates and the P/N ratio was not optimized for the minimum V_{DD} operation. The gate length is the minimum in 90 nm CMOS process. The gate width of nMOS (W_n) and pMOS (W_p) are 0.54μm and 0.82μm respectively. RO's were fabricated with 1 V 90 nm CMOS process in three different lots. The first lot includes inverter RO's from 11-stage to 1Mega-stage to investigate the dependence of VDDmin on the number of stages. The second lot includes inverter RO's, 2NAND RO's and 3NAND RO's to investigate the gate type dependence. The third lot includes inverter RO's and x4 inverter RO's to investigate the gate width dependence.

Figure 4(a) shows the micrograph of a 1Mega-stage inverter RO in 90 nm CMOS. The core area is 2.2mm×1.3mm. Figure 4(b) shows the layout style of RO's. In order to remove the effect of the global variation on RO's, the interconnect length between the

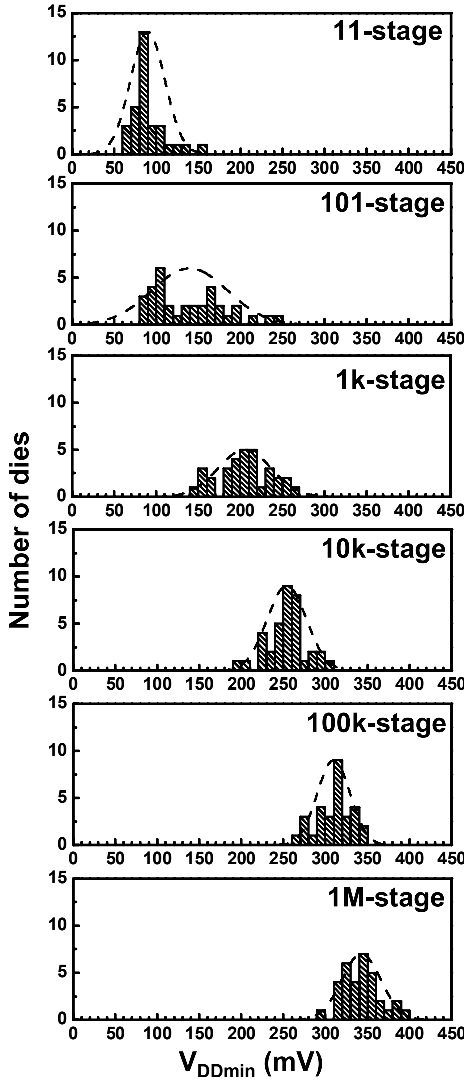


Figure 5. Die-to-die distribution of V_{DDmin} of inverter RO's with different number of stages from 11-stage to 1M-stage.

inverters is as short as possible and the maximum interconnect length in the 1Mega-stage inverter RO is 3.5μm.

2.2 Dependence of V_{DDmin} on Number of Stages

Figure 5 shows the measured die-to-die distribution of V_{DDmin} of inverter RO's with different number of stages from 11-stage to 1M-stage. Figure 6 shows the measured dependence of the average V_{DDmin} with ±1σ error bar of inverter RO's on the number of stages extracted from Figure 5. As the number of stages is increased, the average V_{DDmin} increase, because V_{DDmin} is determined by the worst inverter(s) in each RO. For example, the average V_{DDmin} increases from 90 mV to 343 mV when the number of RO stages increases from 11 to 1Mega. The 343 mV means above V_{TH} operation. The results indicate that V_{DDmin} for logic circuits depends on the scale of the circuits and large scale

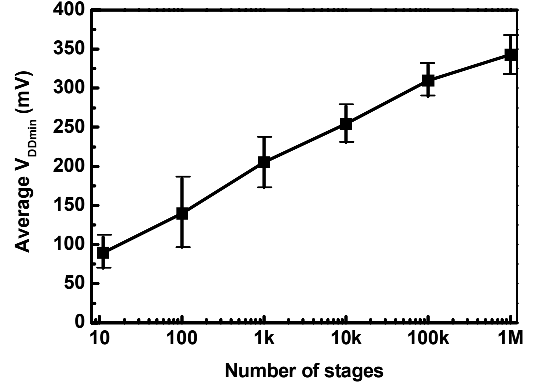


Figure 6. Measured dependence of the average V_{DDmin} of inverter RO's on the number of stages.

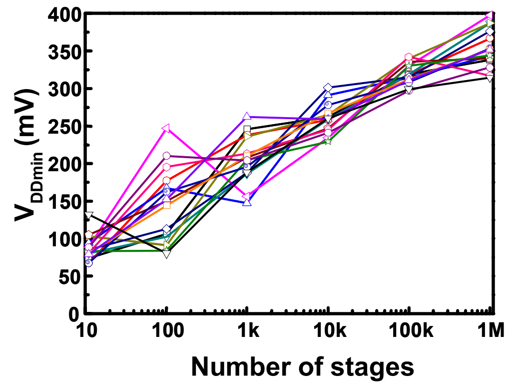


Figure 7. Measured dependence of V_{DDmin} of inverter RO's on the number of stages for 15 dies.

logic circuits have high V_{DDmin}. In order to analyze the die-to-die V_{DDmin} variations, Figure 7 shows the measured dependence of V_{DDmin} of inverter RO's on the number of stages for 15 dies. The die-to-die V_{DDmin} variations are not systematic but random.

2.3 Dependence of V_{DDmin} on Gate Types

Figure 8 shows the measured dependence of the average V_{DDmin} of inverter, 2NAND and 3NAND RO's on the number of stages from 11-stage to 1k-stage. The three lines have the similar gradient, but they have different offsets. The gradient is determined by the transistor variations and the offsets are determined by the unbalance between nMOS and pMOS. In this work, 3NAND RO's have the highest average V_{DDmin}, because both W_n and W_p are the same for the inverter, 2NAND and 3NAND RO's as shown Figures 3(a)-(c) and the 3NAND RO's have the largest unbalance between nMOS and pMOS. The unbalance, however, can be solved by tuning W_p /W_n ratio.

2.4 Dependence of V_{DDmin} on Gate Width

Die-to-die distribution of V_{DDmin} of inverter RO's and x4 inverter RO's with different number of stages from 11-stage to 1Mega-stage is measured. The lowest V_{DDmin} was 58 mV for the 11-stage RO's. Figure 9 shows the measured dependence of the average V_{DDmin} of inverter and x4 inverter RO's on the number of stages. The two lines have the similar offset, but they have different gradients. In theory, the gradient of the x4 inverter RO's is half of

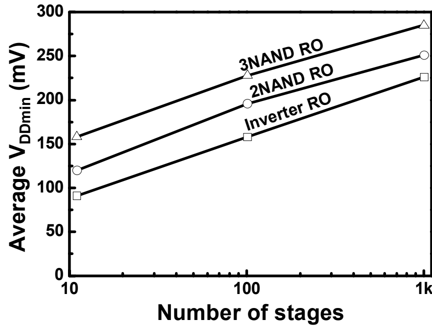


Figure 8. Measured dependence of the average V_{DDmin} of inverter, 2NAND and 3NAND RO's on the number of stages.

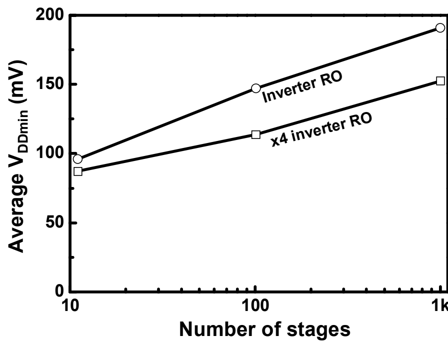


Figure 9. Measured dependence of the average V_{DDmin} of inverter and x4 inverter RO's on the number of stages.

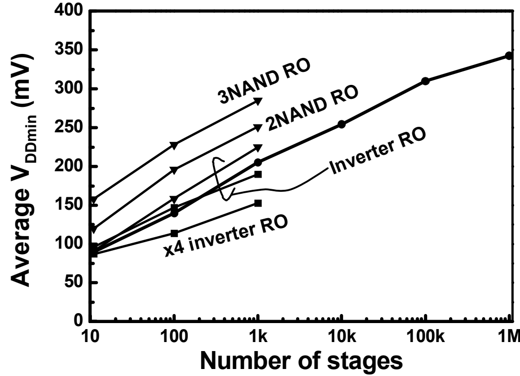
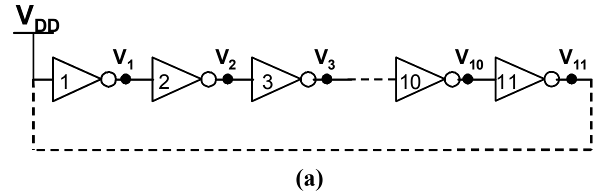


Figure 10. Summary the measured dependence of the average V_{DDmin} of all RO's lots on the number of stages.

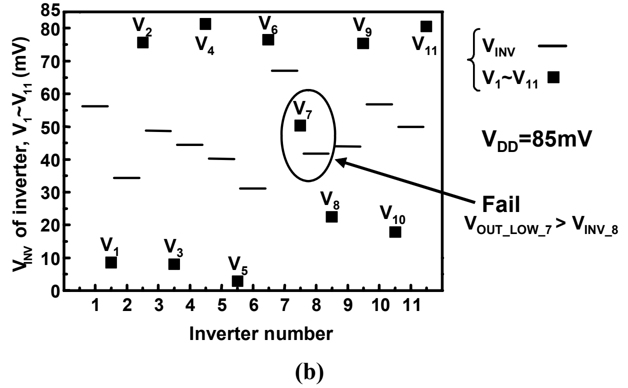
that of the inverter RO's, because the x4 gate width halves the V_{TH} variations. The measured gradient of the x4 inverter RO's, however, is 70% of that of the inverter RO's.

2.5 Summary of V_{DDmin} Measurement

Figure 10 summarizes the measured dependence of the average V_{DDmin} of all RO's lots on the number of stages extracted from Figures 6, 8 and 9. The three lines of the inverter RO's show the measured average V_{DDmin} in three different lots. While increasing the number of stages and the number of stacked transistors increases V_{DDmin}, the wide gate width decreases V_{DDmin}.



(a)



(b)

Figure 11. (a) Simulated 11-stage inverter chain where each transistor has random V_{TH}. (b) Node voltages (V_1−V_{11}) and inversion voltages (V_{INV}'s) of the inverters.

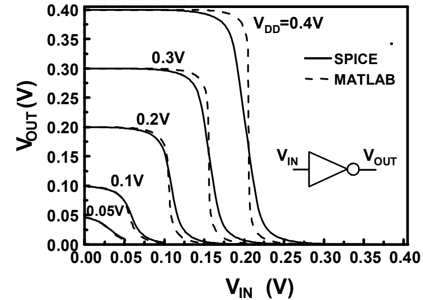


Figure 12. Comparison of the inverter characteristic of SPICE and Matlab.

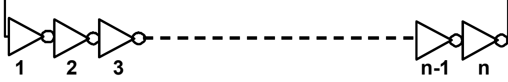
3. ANALYSIS OF V_{DDmin}

3.1 Analysis of V_{DDmin} with SPICE

The origin of the V_{DDmin} is analyzed with Monte Carlo SPICE simulations. Figure 11(a) shows the schematic of the simulated 11-stage RO's where each transistor has random V_{TH}. The inverter chain with the input of V_{DD} is simulated. Figure 11(b) shows the node voltages (V_1−V_{11}) and the inversion voltages (V_{INV}'s) of the inverters. Normally, the logical low of V_1−V_{11} is lower than V_{INV} and the logical high of V_1−V_{11} is higher than V_{IN}. The inverter chain, however, has a function error at #7 and #8 inverter, because #7 inverter has slow nMOS and fast pMOS, V_{INV} of #7 inverter is high, and the logical low of V_7 ($V_{OUT_LOW_7}$) is higher than V_{INV} of #8 inverter. The function error stops the RO oscillation.

3.2 Comparison of Measured and Calculated V_{DDmin}

In order to investigate the increasing average V_{DDmin} with the number of stages, the simulations of V_{DDmin} from 11-stage to 1Mega-stage RO's are required. However, the simulations of



(a)

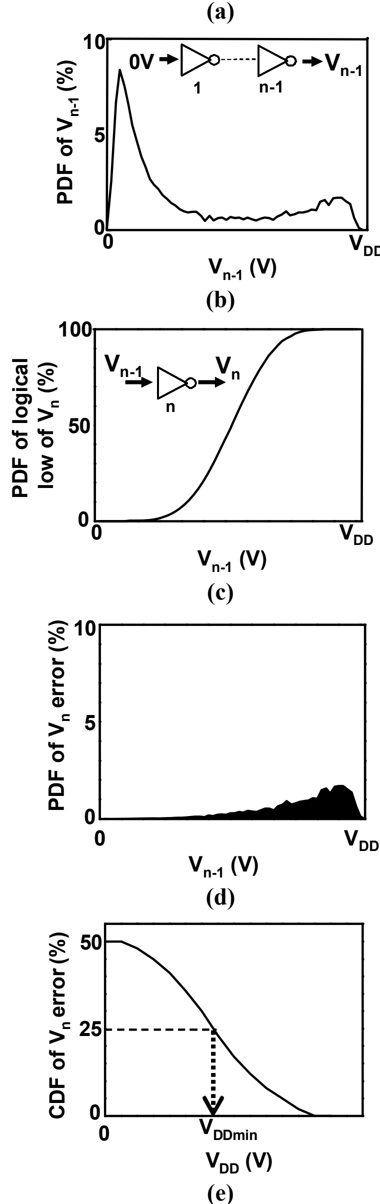


Figure 13. Calculation steps of V_{DDmin} of n-stage RO. (a) Calculated n-stage inverters. (b) PDF of the output of the (n−1)-stage inverter chain with the input of 0V. (c) PDF of the logical low (=error) of V_n. (d) PDF of V_n error. (e) CDF of V_n error.

V_{DDmin} of up to 1Mega-stage RO's with Monte Carlo SPICE take too long time and are not practical. Therefore, V_{DDmin} is calculated with the subthreshold current model with random V_{TH} variations and compared with the measured results. Equation (1) shows the drain current model of MOSFET in the subthreshold region.

$$I_D = C_1 e^{C_2(V_{GS}-V_{TH})}(1-e^{-C_3 V_{DS}}) \quad (1)$$

I_D is the drain current, V_{GS} is the gate-to-source voltage and V_{DS} is the drain-to-source voltage. C_1, C_2 and C_3 are constants. In the CMOS inverter, the input-output characteristic of the inverter is derived by equating I_D of nMOS and pMOS. Figure 12 shows the comparison of the inverter characteristic of SPICE and the calculation with Equation (1). MATLAB is used for the calculation. V_{DD} is varied from 50mV to 0.4V. The calculation is verified by comparing with SPICE. Below V_{DD} of 0.2V, the calculation error is small. In contrast, Above V_{DD} of 0.3V, the calculation error is large, because the calculation includes only the diffusion current (= subthreshold current) and neglects the drift current (= strong inversion current).

Figure 13 shows the calculation steps of V_{DDmin} of a n-stage RO, where n is an odd number. The transistors in the RO have random V_{TH} variations. First, the probability density function (PDF) of the output (V_{n-1}) of the (n−1)-stage inverter chain with the input of 0V is calculated by cascading the (n−1)-stage inverters as shown in Figure 13(b). Though the correct V_{n-1} is low, Figure 13(b) shows some incorrect high V_{n-1} due to the function error. Then, the PDF of the logical low (=error) of V_n by integrating the V_{INV} distribution is as shown in Figure 13(c). Figure 13(d) shows PDF of V_n error derived by multiplying Figure 13(b) by Figure 13(c). Finally, Figure 13(e) shows the cumulative distribution function (CDF) of V_n error derived by integrating Figure 13(d). Strictly speaking, CDF of V_n error of the n-stage inverter chain with the input of V_{DD} should also be calculated and added to Figure 13(e). However, the inputs of 0V or V_{DD} are symmetry. Therefore, V_{DDmin} is defined as V_{DD} when CDF of V_n error equals to 25% as shown in Figure 13(e).

Table I shows the 4 sets of σV_{TH}'s of nMOS and pMOS used in the calculation. σV_{TH}'s are originally determined by the Pelgrom plot, however, σV_{TH}'s are varied to fit the measured results. Figure 14 shows the comparison of measured and calculated dependence of the average V_{DDmin} of inverter RO's on the number of stages. The measured x4 inverter RO's are also plotted. The calculation shows the expected increasing gradients and offsets with increased σV_{TH}, which confirm the tendency of the measurement. The two reasons for the quantitative error between the measurement and MATLAB are; (1) Only V_{TH} variations are considered in the calculation and no other variations are not considered. (2) The inverter characteristic error increases with the increased V_{DD} as shown in Figure 12, because the model includes only the subthreshold current and neglects the strong inversion current.

Finally, the reason why the average V_{DDmin} increases with the number of RO stages is discussed. Generally, the largest value distributions $f_{max}(x,n)$ of n samples which have Gaussian distribution $f(x)$ are shown in Figure 15.

$$f(x) = \frac{1}{\sqrt{2}\sigma} e^{-\frac{(x-\bar{x})^2}{2\sigma^2}} \quad (2)$$

$$f_{max}(x,n) = \frac{d}{dx}\left\{\left(\int_{-\infty}^{x} \frac{1}{\sqrt{2}\sigma} e^{-\frac{(y-\bar{x})^2}{2\sigma^2}} dy\right)^n\right\} \quad (3)$$

Table I. Several sets of σV_{TH}'s of nMOS and pMOS used in the calculation.

Name	σV_{TH} (mV)		Remarks
	nMOS	pMOS	
Sim075	25.8	22.5	x0.75
Sim100	34.4	30.0	x1
Sim125	43.0	37.5	x1.25
Sim150	51.6	45.0	x1.5

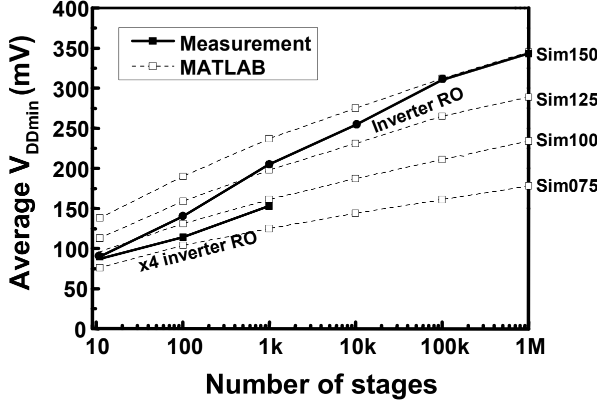


Figure 14. Comparison of measured and calculated dependence of the average V_{DDmin} of inverter RO's on the number of stages.

$\bar{x}$ is the average of x and σ is the standard variation of x. The x value ($\overline{x_{max}}$) where $f_{max}(x,n)$ has its peak is approximated as

$$\overline{x_{max}} \cong \bar{x} + 2\sqrt{\log_{10} n}\,\sigma \qquad (4)$$

Figure 16 shows the n dependence of $\overline{x_{max}}$, and compares the exact and approximated results. Equation (4) intuitively explains the reason why the average V_{DDmin} increases with the number of RO stages. The calculated dependence in Figure 14 is also approximated by Equation (4) and the error was negligible small.

4. CONCLUSIONS

The minimum operating voltage (V_{DDmin}) of 90-nm CMOS logic gates has been investigated with the ring oscillators. The measured average V_{DDmin} of inverter RO's increased from 90 mV to 343 mV when the number of RO stages increased from 11 to 1Mega, which indicates the difficulty of the V_{DD} scaling in the large scale subthreshold logic circuits. While increasing the number of stages and the number of stacked transistors increases V_{DDmin}, the wide gate width decreases V_{DDmin}. The dependence of V_{DDmin} on the number of stages is calculated with the subthreshold current model with random threshold voltage variations, which confirm the tendency of the measurement.

5. ACKNOWLEDGMENTS

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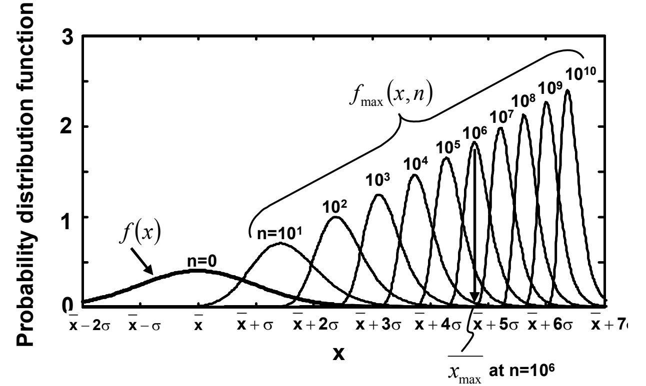

Figure 15. The largest value distributions $f_{max}(x,n)$ of n samples which have Gaussian distribution $f(x)$.

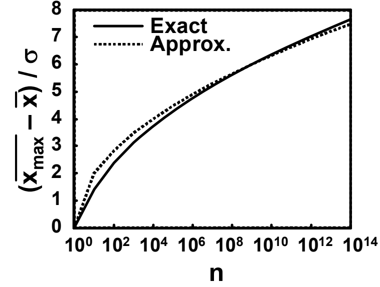

Figure 16. Comparison of exact and approximated results in n dependence of $\overline{x_{max}}$.

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