# Backgate Bias Accelerator for sub-100 ns Sleep-to-Active Modes Transition Time

David Levacq, *Member, IEEE*, Makoto Takamiya, *Member, IEEE*, and Takayasu Sakurai, *Fellow, IEEE*

***Abstract*—Backgate biasing is a promising technique for high speed systems. Leakage can be reduced during standby periods by reverse bias while adequate bias in active mode can balance process and temperature variations. This technique introduces no delay penalty in active mode but slow wake up time results in system performance degradation. In this paper, we demonstrate a circuit that provides fast charging of the backgate through a large MOSFET directly connected to the supply. A circuit based on a mirror delay is used to precisely turn off this MOSFET when the backgate voltage has reached the required bias voltage for active mode operation. A nonlinearity compensation operation is implemented to guarantee precise control of the timing despite a non-constant backgate charging rate during transition due to nonlinear backgate capacitance. A sleep-to-active mode transition on the order of 10 ns is demonstrated in a 90 nm CMOS technology. The accelerator occupies less than 2% of the total chip area, consumes 600 $\mu$W during the transitions and does not add any bias current during active and sleep modes.**

***Index Terms*—CMOS, backgate bias, body bias, low power, high speed, leakage reduction, static power reduction, sleep mode.**

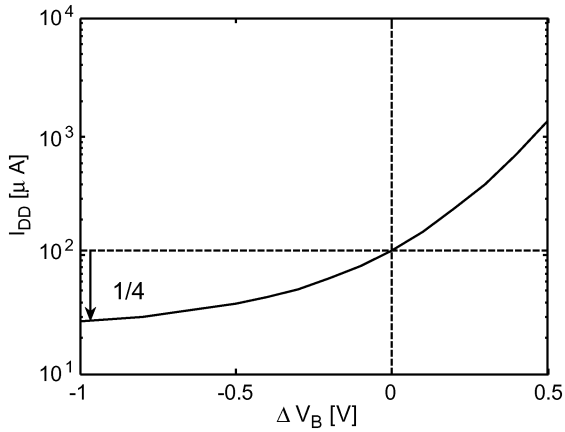


Fig. 1. Measured static current of 40 k NAND gates versus backgate bias ($V_{\rm DD} = 1$ V, $V_{\rm Backgate} = \Delta V_{\rm B}$ for NMOSFETs, $V_{\rm Backgate} = V_{\rm DD} - \Delta V_{\rm B}$ for PMOSFETs).

## I. Introduction

REDUCTION of static power dissipation during standby (or 'sleep') periods, i.e., when no data operation must be performed, is a major requirement for any VLSI chip today. Power gating technique, which introduces high threshold voltage $(V_{\rm th})$ sleep transistors to gate the power supplies of low $V_{\rm th}$ logic blocks during standby periods is widely used now [1] but suffers from some limitations for ultra-high speed applications. The insertion of sleep transistors results in a degradation of circuit speed and consumes silicon area. Their sizing can be a difficult task. The power supply noise induced by the switching of the sleep devices may affect the system reliability and the circuit state is lost when it is disconnected from power line, unless specific flip-flops with state retention capability during sleep modes or additional low standby power memory are used. In this last case, data saving and recovering operations increase the system latency.

An alternative to power gating is backgate/body bias: the $V_{\rm th}$ of the transistors is increased by reverse body bias during sleep mode, resulting in leakage power reduction. Backgate bias shows several advantages compared to power gating:

1) Unlike power gating, there is no data loss during standby mode, eliminating the requirement of specific storage elements.
2) Backgate bias can be used in active mode as well to balance process and temperature variations, and/or tune the circuit speed according to the computation requirements [2], [3].

A common criticism against backgate bias is that the efficiency of reverse body-biasing degrades as technology scales due to the higher contribution of other leakage mechanisms to the total static power dissipation: band-to-band-tunneling in reverse biased junctions, GIDL, gate leakage, etc. However, those leakage currents can be reduced by fabrication process improvements, and backgate bias can therefore still provide significant static power reduction in advanced technologies. Moreover, backgate bias is expected to get increased interest in a near future with the technological evolution towards double-gate devices that demonstrate very high backgate control efficiency, such as FinFETs or SOTBOX [4].

The circuits of this work have been implemented in a 90 nm CMOS technology in which the static power can be divided by 4 by applying $-1$ V reverse backgate bias as shown in Fig. 1. In active mode, backgate bias can tune the delay of logic cells by $\pm 30\%$ (Fig. 2) to balance process/temperature variations.

Backgate bias, possibly combined with variable $V_{\rm DD}$ [5], is therefore especially appropriate for high speed applications, like servers or super-computers, at the condition to provide fast transitions between sleep and active modes. In active mode, the backgate bias generator must provide adequate backgate bias

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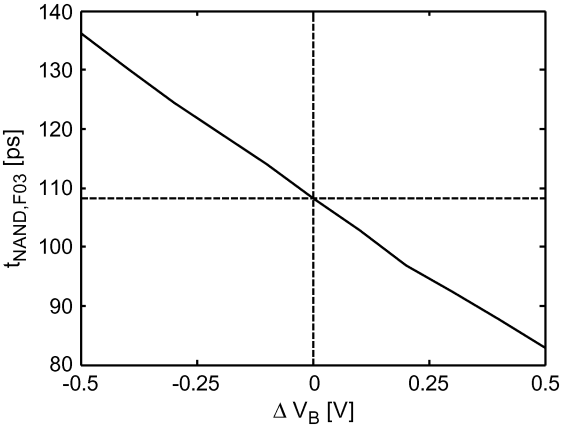


Fig. 2. Measured propagation delay of a 2NAND gate (fanout 3) versus backgate bias ($V_{\rm DD} = 1$ V, $V_{\rm Backgate} = \Delta V_{\rm B}$ for NMOSFETs, $V_{\rm Backgate} = V_{\rm DD} - \Delta V_{\rm B}$ for PMOSFETs).

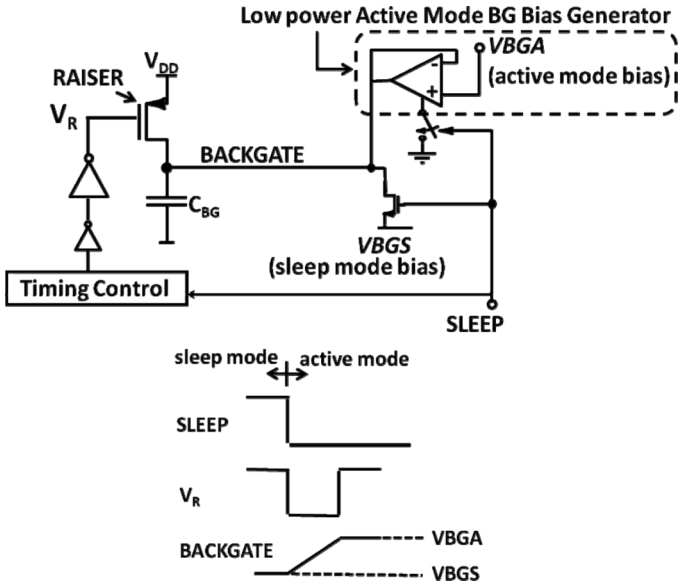


Fig. 3. Backgate bias accelerator principle.

voltage VBGA to balance process and temperature variations. Typically, this generator can be implemented as a voltage buffer with a simple source follower or an amplifier in a feedback loop [6]. It must dissipate minimum power, provided its output impedance is sufficiently low for not introducing additional noise onto the substrate. Considering this, a conventional backgate generator cannot provide fast charging of the large backgate capacitance to sweep its voltage from negative sleep backgate bias (VBGS) to VBGA in a short time.

In this paper, we present a Backgate Bias Accelerator (BBA) circuit that allows to strongly accelerate the charging of the backgate to have fast transition from sleep to active modes, with VBGA tuning capability. In Section II we describe the operation principle of the new accelerator. A description of the circuits is given in Section III. An experimental design on a 90 nm CMOS technology is presented in Section IV.

## II. Backgate Bias Accelerator Principle

Let consider the backgate bias technique in the case of NMOSFETs. Fig. 3 illustrates the principle of the proposed circuit to accelerate the sleep-to-active modes transition.

In sleep mode, the sleep control signal is HIGH and the backgate is tied to VBGS (e.g., $-1$ V). The active mode backgate bias generator is turned off and does not consume any DC bias current. Once the SLEEP control signal goes down, a large PMOS (the raiser) that is directly connected to the positive supply is turned on and quickly charges the backgate. The raiser is turned off once the backgate voltage has reached VBGA. This voltage is then maintained in active mode by the low power Active Mode Backgate Bias Generator. The raiser must be accurately controlled to avoid backgate charging above (if it is turned off too late) or below (if it is turned off too early) VBGA. If we turn off the raiser after that a comparator has detected that the backgate has reached VBGA, the delays of the comparator and the long raiser buffer chain introduce imprecision in final backgate voltage. In the next section we present a technique to predict the charging time of the backgate to turn off the raiser when the backgate voltage is precisely equal to VBGA.

## III. Control Circuits

In [7], we have proposed a circuit to predict the required ON time of the raiser that was based on the use of a mirror-delay [8]. Its operation can be explained with the timing diagram that is plotted in Fig. 4(a). In sleep mode (i.e., $\mathrm{Sleep} = \mathrm{HIGH}$), the backgate is reverse biased to VBGS. When the sleep signal goes low, the raiser is turned on and starts to charge the backgate. At the same time, a capacitor C1 is charged by a reference current $I_{\rm C}$.

After a time interval T1, when the backgate reaches half of its total variation (i.e., (VBGA-VBGS)/2), the charging of C1 is stopped, its voltage stored, and the same current $I_{\rm C}$ is used to charge a capacitor C2 identical to C1. The raiser is turned off when the voltage on C2 reaches the same voltage that is stored on C1, i.e., after a time $T1 + T2 = 2 \times T1$. If BG charging rate is reasonably constant during the transition, this circuit is sufficient to precisely control the raiser. However, a variation of the BG capacitance or of the raiser current during the transition can result in non linear charging. Typically, in a conventional bulk CMOS technology, the charging rate slows down as we move from reverse body-bias in sleep mode to zero or forward body-bias in active mode because junction capacitance increases and raiser current decreases due to Early effect. Consequently, T1 is shorter than T2 in Fig. 4(a). If this difference is significant, the raiser is turned off while the backgate has not reached VBGA yet. This error can be strongly reduced by the circuit shown in Fig. 5. Like in the circuit from [7], we start to charge a capacitor C1 by a current $I_{\rm C}$ as the raiser is turned on. But rather than dividing the charging in two parts to predict the raiser turn-off time (2-piece-wise prediction), it is divided in three (3-piece-wise prediction) to compensate nonlinearities. When the backgate reaches a quarter of its total variation (VBA-VBS)/4 (after a time T1), C1 is left floating and C2 is charged by the same current $I_{\rm C}$ until $V_{\rm BG}$ reaches three quarters of its total variation (after a time $T1 + T2$). C2 is then left floating and C1 is charged again until the voltages on C1 and

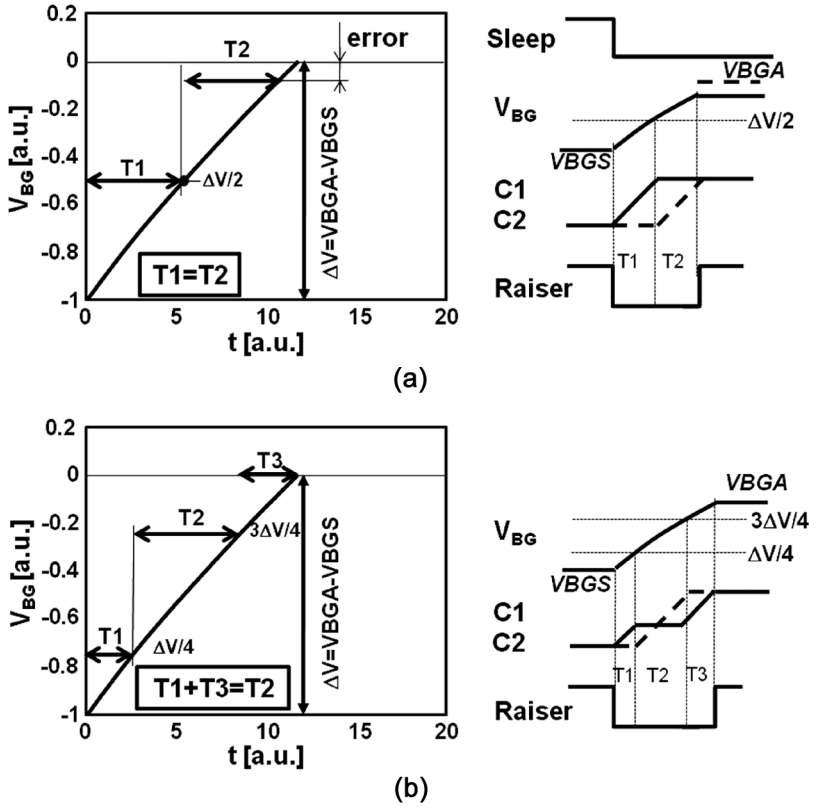


Fig. 4. Timing diagram of BBA: (a) 2-piece-wise prediction scheme; (b) 3-piece-wise prediction scheme with nonlinearity compensation.

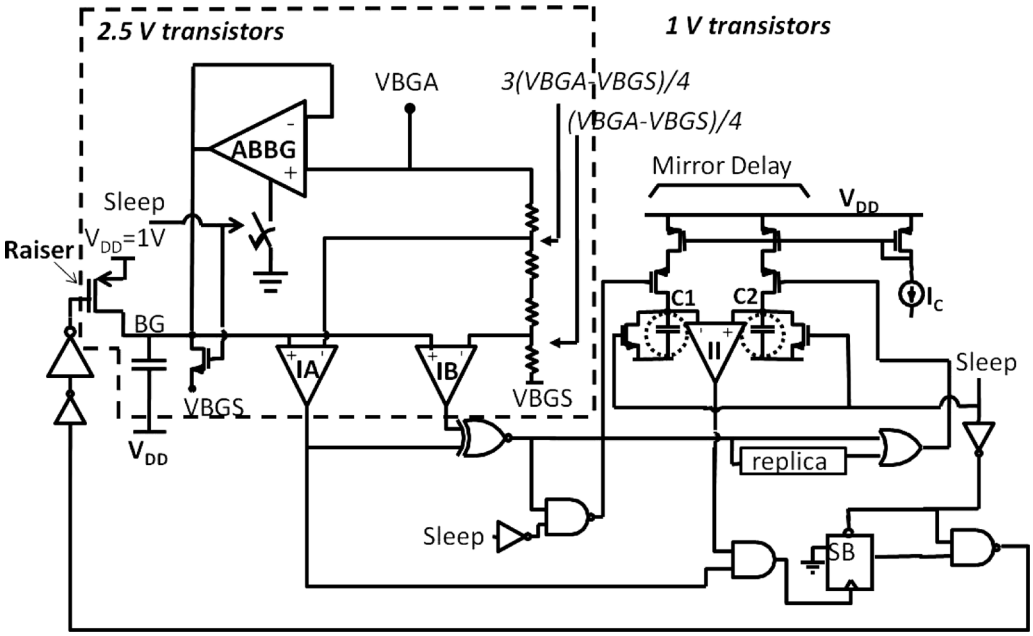


Fig. 5. Schematic of backgate bias accelerator.

C2 become equal. The raiser is then turned off, i.e., after a time $2\times T2$. If $T1 < T2 < T3$ due to slowdown of the charging, this technique results in a much better approximation of the charging time and a higher precision on the BG voltage when the raiser is turned off than with the previous proposal [Fig. 4(b)].

The comparators of the control circuit introduce delays in the control circuit that must be substracted in some way. A simple timing analysis shows that those can be cancelled out by delaying the charging of C2 by a time $t_{\rm repl}$ (see the Appendix):

$$t_{\rm repl} = 2(t_{\rm comp,IB} - t_{\rm comp,IA}) + t_{\rm comp,II} \approx t_{\rm comp,II} \qquad (1)$$

where $t_{\rm comp,IA}$, $t_{\rm comp,IB}$ and $t_{\rm comp,II}$ stand for the delays introduced by comparator IA, IB, and II respectively. This is done

by inserting a replica delay as shown in Fig. 5 that reproduces the propagation delay of comparator II.

## IV. Implementation on 90 nm Process

The proposed BBA has been implemented and measured on a triple-well 90 nm CMOS technology. The same circuit could be used in a double-gate technology [4]. As a test vehicle, the BBA is connected to the P-well of 40 k NAND gates. The circuits inside the dotted rectangle in Fig. 5 are supplied between $V_{\rm DD} = 1$ V and $V_{\rm SS} = {\rm VBGS} < 0$ V (e.g., $-1$ V). Their transistors must operate with drain-to-source voltage superior to the standard 1 V supply voltage. They were therefore implemented with 2.5 V I/O devices. The raiser has been implemented with a PMOSFET with minimum length $({\rm W} = 40 \times 10\ \mu{\rm m}$, ${\rm L} = 0.3\ \mu{\rm m})$.

The other circuits are conventionally supplied between $V_{\rm DD} = 1$ V and ground.

### A. Comparators

The voltage stored on C1 when the backgate has reached a quarter of its final value depends on VBGS, VBGA. By a proper choice of the capacitors C1 and C2 and of the current $I_{\rm C}$, we can ensure that it lies between 0 and $V_{\rm DD}$ for all possible (VBGA, VBGS) pairs. Comparator II must have a relatively constant delay for any stored voltage on C1. We therefore implemented a rail-to-rail comparator that combines operational transconductance amplifiers (OTAs) with NMOSFETs and PMOSFETs differential pairs.

Comparator I, which is supplied by $V_{\rm DD}$ and VBGS lines is an OTA made of 2.5 V transistors.

The DC bias of the comparators is controlled by the sleep signal to guarantee zero DC current during sleep mode.

### B. Active Mode Backgate Bias Generator

The active mode backgate bias generator (ABBG) consists of an OTA in voltage follower configuration (Fig. 5). It has been designed following a power constrained methodology. Its DC power dissipation must be strongly inferior to the active power dissipated by the logic. The power dissipation of a chip with an area equivalent to the 40 k NAND gates test vehicle has been estimated to 50 mW for a 1 GHz clock frequency. The maximum DC power of the ABBG has been fixed to 3% of the total chip power. A second constraint is that the output impedance of the ABBG must be minimized in order to reduce the noise impact on backgate voltage variations [6]. The maximum DC power fixes the maximum DC bias current of the differential pair of the OTA, and consequently determines the minimum achievable output impedance of the ABBG.

The designed ABBG provides 285 $\Omega$ output impedance. The OTA shows a 47 dB DC gain, its DC power dissipation is equal to 1.5 mW in active mode and 72 nW in sleep mode.

## V. Experimental Results

A picture of the test chip is shown in Fig. 6. The total area of the backgate bias accelerator represents less than 2% of the total area for the 40 k NAND gates. 40% of the area of the BBA is occupied by C1 and C2 that were implemented with MIM capacitors. The area overhead of the BBA could be therefore significantly reduced by the use of MOS capacitors since the mirror-delay does not require linear capacitances.

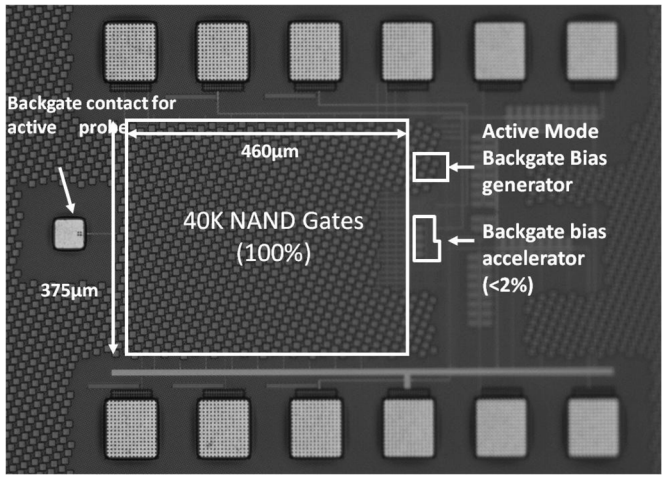


Fig. 6. Test chip microphotograph.

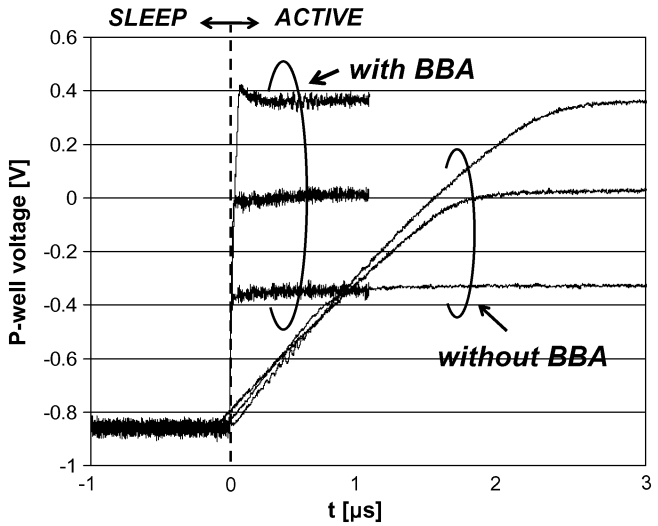


Fig. 7. Sleep-to-active voltage transitions of the backgate of 40K NAND gates with and without BBA.

The voltage of the p-well of the 40 k NAND gates is measured by a high frequency active probe. BBA and the pad for probing are located on different sides of the 40 k NAND block in order to take into account any RC-delay for the backgate bias.

Figs. 7 and 8 show the measured backgate bias during sleep-to active modes transitions. VBGS is fixed to $-0.85$ V, while VBGA is swept between $-0.4$ V and 0.4 V. The BBA efficiently control the ON time of the raiser according to the VBGA value, allowing on-chip tuning of both sleep and active backgate bias voltages. Without BBA, the active mode backgate bias generator alone takes up to 2 $\mu$s to charge the backgate. With the BBA, the transition time between sleep and active mode ranges from 12 ns to 70 ns, that is more than 28 times faster. Non linearity in backgate charging (charging rate sweeps from 27 ns/V to 94 ns/V during the transition from $-0.85$ V to 0.4 V, Fig. 9) is efficiently compensated by the proposed

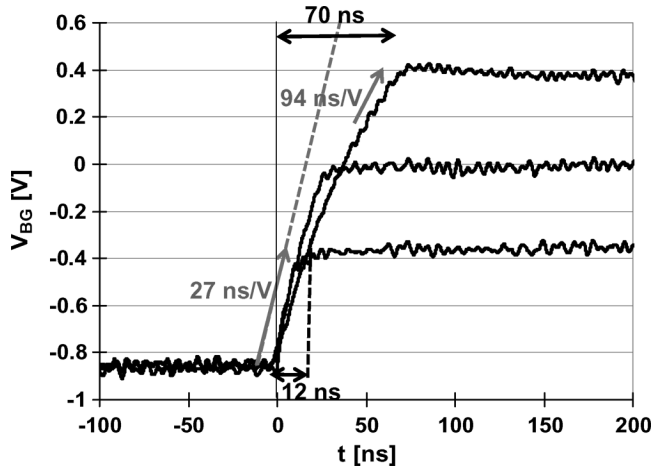


Fig. 8. Detail of sleep-to-active voltage transition with BBA ($\mathrm{VBGS} = -0.85$ V, $\mathrm{VBGA} = -0.4$, 0 and 0.4 V).

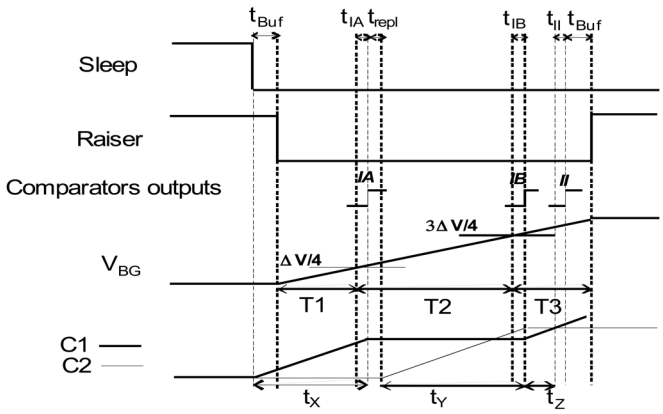


Fig. 9. Timing diagram of BBA signals, including the delays introduced by the comparators IA ($t_{\mathrm{IA}}$), IB ($t_{\mathrm{IB}}$), the replica ($t_{\mathrm{repl}}$) and the raiser buffer chain delays ($t_{\mathrm{BUF}}$).

3-piece-wise prediction scheme that provides precise control of the raiser ON time.

Simulations show that 5 ns rising time is possible by enlarging the raiser transistor without any modification to the rest of the circuit. Without mirror-delay to precisely predict the required ON time of the raiser, the delays of the comparator and the raiser buffer would introduce higher than 100 mV imprecision in final backgate voltage.

The total power dissipation of the BBA during the sleep-to-active mode transition is 600 $\mu$W. Once final voltage has been reached, it can be switched off and consumes negligible power (<100 nW).

## VI. Conclusion

A backgate bias accelerator that achieves fast transition between tunable sleep and active mode backgate voltages has been designed. Conventional active mode backgate bias generators have poor drivability, resulting in slow wake up time. The proposed circuit accelerates the charging of the backgate by using a large MOSFET that is directly connected to the positive supply. To precisely control this MOSFET in order to turn it off precisely when the backgate has reached its active mode bias voltage, a mirror-delay is used. A new operation scheme that divides the charging in three parts to predict the charging time has been proposed to compensate any nonlinearity in backgate charging. A prototype has been designed on a 90 nm CMOS technology. 0.45 V variation of backgate voltage in 12 ns and 1.25 V variation in 70 ns have been experimentally demonstrated. The accelerator occupies less than 2% of the chip area. It consumes 600 $\mu$W during sleep-to-active modes transitions.

## Appendix

The calculation of the required replica delay is illustrated by the timing diagram in Fig. 9 where the voltages of the the backgate and the mirror-delay capacitors are plotted considering the delays introduced by the comparators ($t_{\mathrm{IA}}, t_{\mathrm{IB}}, t_{\mathrm{II}}$), the raiser buffer chain ($t_{\mathrm{BUF}}$) and the replica ($t_{\mathrm{repl}}$). The different delays have been graphically increased for better clarity.

As explained in Section III, the control circuit aims to turn off the raiser after a time $2*$T2, T2 being the charging time of the backgate from $\mathrm{VBGS} + (\mathrm{VBGA} - \mathrm{VBGS})/4$ to $\mathrm{VBGS} + 3 * (\mathrm{VBGA} - \mathrm{VBGS})/4$. If T1 is the backgate charging time from VBGS to $\mathrm{VBGS} + (\mathrm{VBGA} - \mathrm{VBGS})/4$, this is equivalent to stop the raiser after a time $T1 + T2 + T3$ with $T3 = T2 - T1$.

The mirror-delay operation ensures that

$$t_X = t_Z - t_Y. \tag{2}$$

As illustrated in Fig. 9:

$$\begin{aligned} t_X &= t_{\mathrm{BUF}} + T1 + t_{IA} \\ t_Y &= T2 - t_{IA} - t_{\mathrm{repl}} + t_{\mathrm{IB}} \\ t_Z &= T3 - t_{\mathrm{IB}} - t_{\mathrm{II}} - t_{\mathrm{BUF}}. \end{aligned} \tag{3}$$

By combining (2) and (3) we get

$$\Rightarrow T3 = T2 - T1 - 2(t_{IA} - t_{\mathrm{IB}}) + t_{\mathrm{II}} - t_{\mathrm{repl}}.$$

If comparators IA, IB are identical, their delays are approximately equal:

$$\Rightarrow T3 = T2 - T1 + t_{\mathrm{II}} - t_{\mathrm{repl}}.$$

To have $T3 = T2 - T1$, and thereby turn off the raiser after a time $T1 + T2 + T3 = 2 * T2$ as wanted, the replica must be equal to

$$t_{\mathrm{repl}} = t_{\mathrm{II}}.$$

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