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500Mbps, 670μW/pin Capacitively Coupled Receiver with Self Reset Scheme for Wireless Connectors

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Abstract- **Using capacitively coupled signaling, the feasibility of implementing an electronic connector as short as 240μm in height is demonstrated for the first time using 0.18μm CMOS technology and 125μm FR4 printed circuit boards (PCB's). Maximum data rate of 500Mbps/pin and 3.6Gbps/mm^2 are measured with 670μW/pin of power consumption even with large parasitic capacitance associated with the FR4 board. Compared to the conventional circuits, the proposed self reset circuit can send signals 2.8x faster at the same parasitic capacitance or allow 6x more parasitic capacitance at the same data rate.**

Keywords: **Capacitive coupling, Low-profile connector and Proximity communication**

Introduction

There is a strong demand for low-profile components to reduce the thickness of recent portable electronic appliances such as mobile phones, laptop PC's, and PDA's. In this paper, using capacitively coupled signaling, the feasibility of implementing an electronic connector as short as 240μm in height is demonstrated for the first time using 0.18μm CMOS technology.

Recently, proximity communication technology has been investigated extensively mainly for the purpose of transferring data among stacked chips [1-5]. In order to realize a detachable connector, interconnections over organic FR4 printed circuit boards were used, which have orders of magnitude higher parasitic capacitance compared to interconnections on chips. This increases the technical difficulty of detachable connectors, compared to chip-to-chip communication.

Mechanical Connectors vs Wireless Connectors

Mechanical connectors need to scrape off residue and oxides of the surface of the connectors, and apply ~20g of pressure to maintain low resistances and stable connections. They are facing many problems for applying this pressure. The complex spring mechanism implemented in each pin for low profile connectors reduces the number of times the connector can be detached to as few as 5 times. To reduce the force needed to attach/detach a connector with many pins, Zero Insertion Force (ZIF) connectors which hold and release the connector pins with a lever, were developed which however consumes much space so cannot be used in space critical places.

Wireless connectors however, do not need pressure to reduce resistance nor do they need scraping mechanisms, thus simplifying the structure. They could reduce footprint and faulty connections. The capacitive coupling technique used here will also be useful in implementing a connector that has large number of pins. In a case where 10,000 pins are necessary and 20gf of pressure is needed for a stable mechanical connection, 200kgf is needed to press the connector, while in the case of wireless connectors, there is no need to put pressure on the pins.

Table I
Comparison of mechanical and wireless connector

	Conventional (mechanical)	Non-contacting
Pressure / pin	20g	~0g
Height	0.6 mm	~0.24 mm
Pin density	1pin / mm^2	10pins / mm^2
Reliability	△	○
Water proof	×	○

Table I compares the mechanical and wireless connectors.

Connectors vs Chip-to-chip Communications

For non-contacting chip to chip communication, there

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are two main approaches, using capacitive coupling and using inductive coupling. When implementing connectors on PCB's, the inductor or capacitor must be drawn on the PCB. Common technology for PCB's is 125µm line and space, so using inductors drawn on PCB's will require more area per pin compared to capacitively coupled connectors.

The wireless connector demonstrated here, and previously reported capacitively coupled chip to chip communication circuits share similar topologies but are completely different in that for the connector, the parasitic capacitance is very large (500fF~1pF) and differ between pin to pin because of parasitic capacitance on PCB boards which may vary according to the pattern on the PCB, and I/O diodes on the receiver chip which are excluded in chip to chip communication. Therefore, capacitively coupled technology was chosen over inductively coupled communication for the connector.

For capacitively coupled communication, the signal is always pulled back to a known DC level. The signal that propagates from the output of the TX (TXout) to the input RX (RXin) can be calculated using the coupling capacitance C_C, parasitic capacitance on the RX side C_{PR} and the resistance of the resistor or transistor which pulls the voltage of RXin to the DC level R_R, as shown in fig. 1.

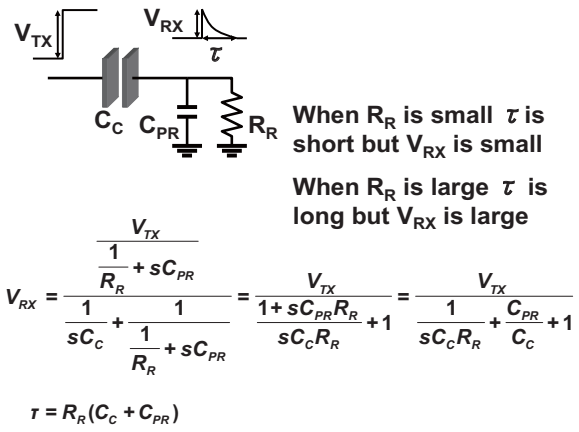

Fig. 1 Relationship between V_{RX}, R_R and τ

This shows that the resistance R_R causes a tradeoff between the input voltage at RXin V_{RX} and the time to reset the signal **τ**.

Proposed Capacitively Coupled Receiver

To overcome the problems shown above, a dual threshold, tri-band signal detection scheme and a self reset circuit are proposed. Fig. 2 shows the circuit schematic.

The dual threshold scheme consists of two sets of amplifiers and inverters to detect three regions, signal transition to high, signal transition to low, and no signal transition. Simulated waveforms are shown in fig.3.

As seen in the previous section, the selection of the resistor R_R is a tradeoff of input voltage and maximum

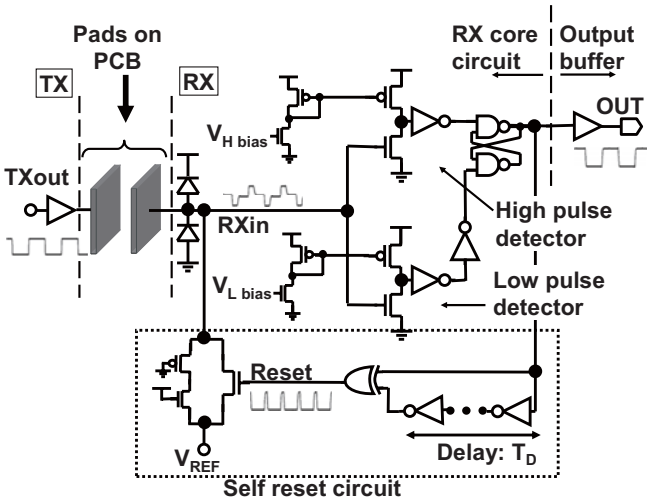

Fig. 2 Schematic of connector receiver circuit

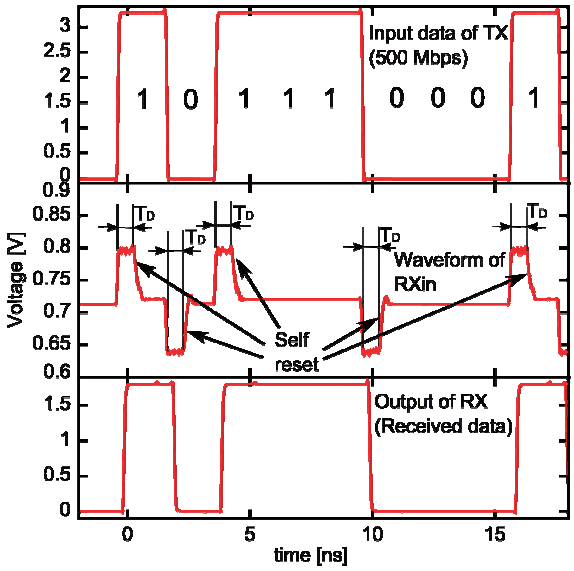

Fig. 3 Simulated waveforms of receiver circuit at 500Mbps

signal frequency. In the case of connectors, the parasitic capacitance and coupling capacitance both vary from pin to pin. To mitigate the tradeoff, when the receiver circuit waits for a signal, the reset transistor is turned off so that R_R is high, enabling large signal input, and when the signal is detected, it is pulled back by turning the reset transistor on to create a low resistance R_R. Fig. 4 shows the receiver circuit without the self reset circuit.

Fig. 5 shows through simulation, the maximum data rate of the receiver with a constant R_R and self reset circuit. The self reset circuit can send signals at the same data rate with 6x more parasitic capacitance, or 2.8x faster at the same parasitic capacitance compared to conventional circuits. For connectors, C_{PR}/C_C is about 5 to 10, making the self reset circuit, more important than chip to chip

connectors with low parasitic capacitances.

This receiver scheme enables the use of voltage level signaling for TX. This accounts for either increasing the pulse swing at the receiver by 2x compared to [1], increase the data rate of the signal by 2x compared to [3], reduce the number of pads needed for 1 channel by 1/2 thereby reducing power at the TX buffer by 1/2, and area of the pins by 1/2 compared to [5].

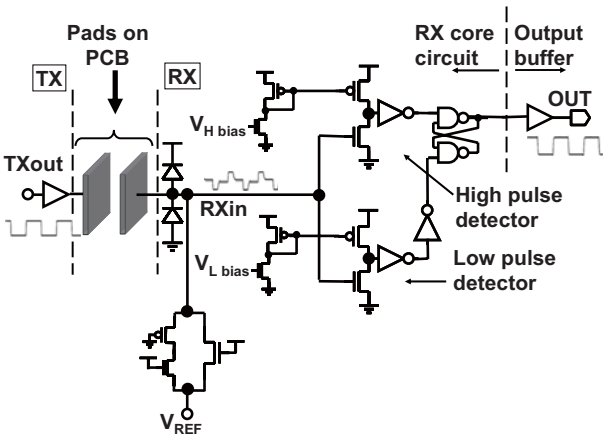

Fig. 4 Receiver circuit without self reset

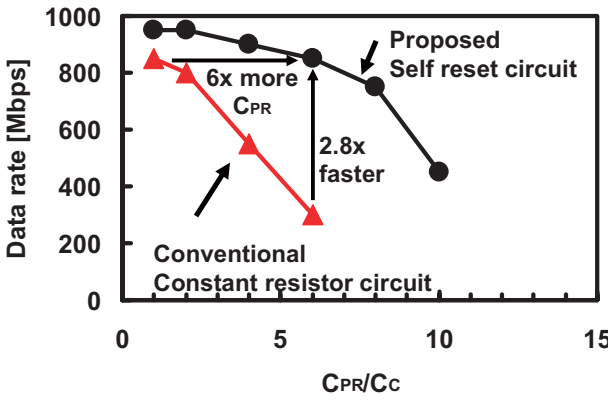

Fig. 5 Simulated dependence of the maximum data rate of conventional and proposed circuits on C_{PR}/C_C.

Measured Results

To prove the feasibility of this scheme, the receiver circuit was implemented in 0.18µm CMOS technology. The size of the core circuit of the receiver is 35µm by 65µm. The 250µm square non-contacting pads were made using 100µm thick FR4 boards with 125µm L/S technology. The connector is 240µm in height. To ensure insulation, 20µm thick solder masks were laminated on all connector pads. The measurement setup is illustrated in fig. 6.

Input and output waveforms at 500Mbps are shown in fig. 7. The data is 2^8-1 bit PRBS signals. The BER bathtub

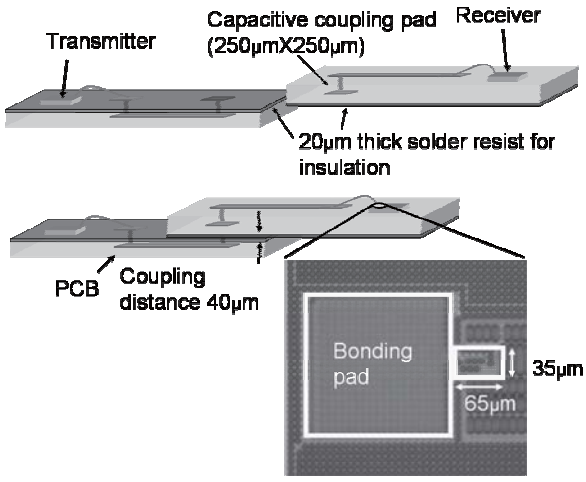

Fig. 6 Illustration of measurement setup and chip micrograph

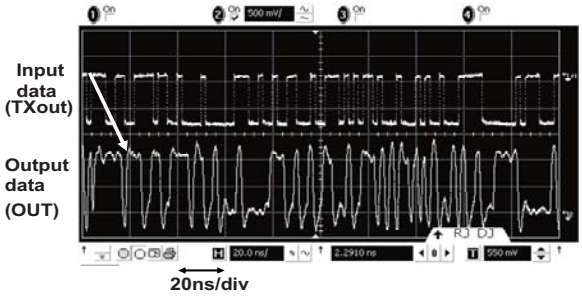

Fig. 7 Measured input and output waveforms at 500Mbps

is measured and drawn as shown in fig. 8. The timing

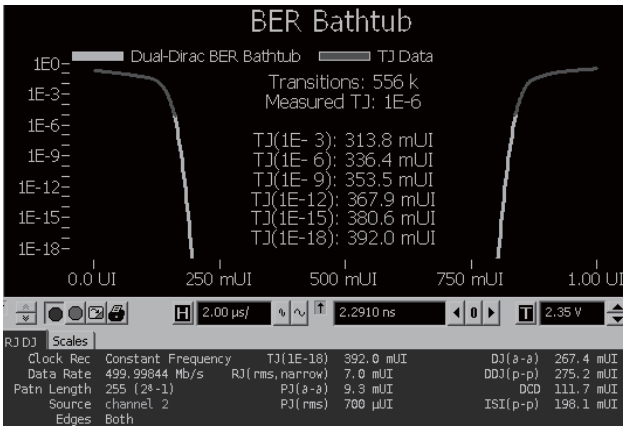

Fig. 8 BER Bathtub curve at 500Mbps.

tolerance is 0.6UI at BER of 10^{-18}.

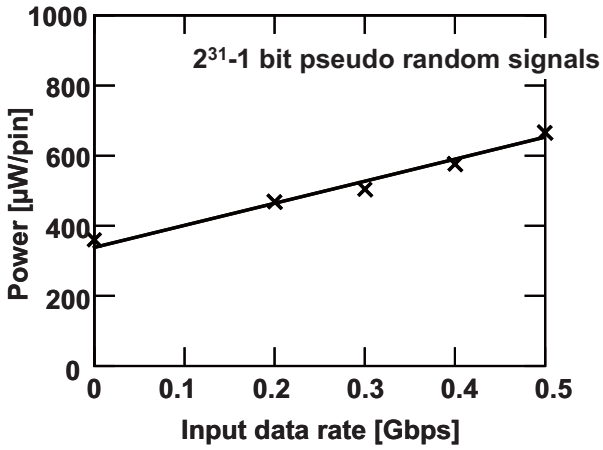

Fig. 9 Power versus input data rate

Power dissipation is shown in fig. 9. The core of the receiver circuit uses 360µW when there is no signal. Since the current mirror circuit for the bias can be shared by multiple receiver circuits, the static power of each circuit decreases when the number of RX circuits increase. At the maximum data rate, the measured power is 670µW/pin, excluding the power for the output buffer.

Table II summarizes the performance of the connector chip. Simulated results show the scalability of this circuit.

Conclusion

A capacitively coupled receiver circuit with a dual threshold tri-state signal detection and a self reset circuit is proposed for wireless connectors. A wireless connector using this topology was demonstrated using 0.18µm CMOS technology. Simulation showed that this self reset circuit enabled the circuit to work 2.8x faster at the same parasitic capacitance or with 6x parasitic capacitance at the same data rate compared to conventional circuits.

Table II
Performance summary of measured and simulated receiver

	Measured	Simulated
CMOS technology	0.18µm 6-Metal CMOS	65nm CMOS
Power supply	1.8V	1.0V
Receiver core size	65µm X 35µm	40µm X 20µm
Maximum data rate	500Mbps	2Gbps
Power @ max data rate	670µW/pin	760µW/pin
Board technology	125µm line/space on 100µm thick FR-4	Same as left
Board pad size	250µm X 250µm	Same as left
Distance between facing pads	40µm (pad metal covered by solder mask)	Same as left

The size of the core circuit of the receiver is 35µm by 65µm. 250µm square non-contacting pads were made using 100µm thick FR4 boards with 125µm L/S technology and demonstrated communication with the distance of 40µm. The connector was measured at a maximum data rate of 500Mbps and had 0.6 UI timing margin, while dissipating 670µW/pin.

Also, scalability of this scheme using 65nm CMOS was checked by simulation to operate at speeds up to 2Gbps while dissipating 760µW/pin.

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