A 100Mbps, 0.19mW Asynchronous Threshold Detector with DC Power-Free Pulse Discrimination for Impulse UWB Receiver

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Abstract - An asynchronous threshold detector for DC-960MHz band impulse ultra-wideband (UWB) receiver is proposed in this paper. It features a DC power-free pulse discriminator. The proposed architecture in 90nm CMOS achieves the lowest power consumption of 0.19mW and energy consumption of 1.9pJ/bit at 100Mbps in the UWB receiver.

I. Introduction

Receivers for impulse UWB can be broadly categorized as threshold or leading edge detectors, correlation detectors, and RAKE receivers. Multi-user detectors (MUD) and hybrid RAKE/MUD-UWB receivers for robust narrowband interference suppression are becoming popular. However, a single clocked-correlator receiver [1] or threshold detector [2] can also be used for short distance and high SNR environments.

In this paper a novel asynchronous threshold detector [3] is proposed for the ad-hoc wireless sensor networks. These ubiquitous networks require that the individual nodes are tiny, easily integratable into the environment, and have negligible cost. The proposed detector features a DC power-free pulse discriminator and an error-recovery phase-frequency detector (PFD), thereby achieving extremely low power consumption at 100Mb/s data-rate.

II. Asynchronous Threshold Detector

An ultra low-power solution for BPSK demodulation is leading edge detection (LED) technique [3]. The LED receiver sets a threshold at the receiver, and any incoming pulse that crosses the threshold is detected and demodulated. The proposed asynchronous threshold detector is shown in Fig. 1. It consists of four building blocks: a front-end amplifier, a DC power-free pulse discriminator, an error-recovery phase-frequency detector (PFD) and a Reset-Set Flip-Flop (RSFF).

The received signal is first amplified by the front-end amplifier and each BPSK symbol is split into two pulses by the proposed DC power-free pulse discriminator. Then the first incoming edge of the two pulses is detected by the PFD and the RSFF converts the detection result to the corresponding data bit.



Fig.1. Proposed UWB receiver with DC power-free pulse discrimination.

III. DC Power-Free Pulse Discriminator

Conventionally, an amplifier and a comparator can be used as the threshold detector. The major disadvantage of this topology is large DC power dissipation that occurs even for no AC input. In the transmitted BPSK signal, the circuit spends long periods of time with no AC signal. Power dissipated in these periods is wasted. The operation principle of the proposed DC power-free pulse discriminator is shown in Fig. 2. Two unbalanced inverter InvH and InvL are employed to detect the positive pulse and negative pulse respectively. To tune the threshold of the pulse discriminator, variable bias voltages V_L for the source input of the top inverter and V_H for the bottom inverter are used. As shown in Fig. 3, the proposed pulse discriminator has essentially zero power dissipation for no AC input.



Fig. 2. DC power-free pulse discriminator.



Fig.3. Simulated waveforms of pulse discriminator.

VI. Experimental Results

A test chip without the front-end amplifier was designed and fabricated in 90nm CMOS process and the micrograph is shown in Fig. 4. The measured receiver power dependence on data rate at different bias voltage is shown in Fig. 5. The tradeoff between power consumption and sensitivity can be tuned by the bias voltage ΔV in Fig.2. Fig. 6 shows the comparison with the state-of-art UWB receivers. The proposed architecture achieves the lowest power consumption of 0.19mW and energy consumption of 1.9pJ/bit at 100Mbps in the UWB receiver.

V. Conclusions

The proposed receiver without the front-end amplifier in 90nm CMOS achieves the lowest energy per bit in the UWB receiver.

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Fig. 5. Measured receiver power vs. data rate.



Fig. 6. Comparison with the published UWB receivers.

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