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An On-Chip Noise Canceller with High Voltage Supply Lines for Nanosecond-Range Power Supply Noise

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SUMMARY An on-chip power supply noise canceller with higher voltage supply and switching transistor is proposed and the effectiveness of the canceller is experimentally verified. The noise canceller is effective for nano-second order noise caused by circuit wakeup or step increase of frequency in frequency hopping. The principle of the noise canceller is to reduce the current flowing through the supply line of V_{DD} by injecting additional current from the higher voltage supply, so that the voltage drop across the V_{DD} supply line is reduced. As additional current flow from higher supply, switching transistor has to be turned off not to increase the power consumption. With turn-off time of $2L/R$, this current can be turned off without inducting another droop due to the increase of current flowing through the power supply line. The measurement shows the canceller reduces 68% of the noise with load circuit equivalent to 530 k logic gates in 90-nm CMOS with 9% wire overhead, 1.5% area overhead, and 3% power overhead at 50 k wake-ups/s. Compared to passive noise reduction, proposed noise canceller reduces power supply noise by 64% without wire overhead and to achieve same noise reduction with passive method, 77 times more C or 45 times less L is required. Too large switching transistor results in saturated noise reduction effect and higher power consumption. A rule-of-thumb is to set the on-resistance to supply 100% of load current when turned-on.

key words: *power integrity, power gating, wake-up, dynamic voltage and frequency scaling, noise canceller*

1. Introduction

System-on-a-Chip (SoC) and System-in-a-Package (SiP) have become major integration technologies in recent years. They have various types of circuit blocks like MPU, DRAM, SRAM, ROM, logic and analog circuits on a chip or in a package. These blocks often employ recent low power VLSI design such as power gating, clock gating, and dynamic voltage and frequency scaling (DVFS), which generate rapid and large change of the power supply current at the moment of the wake-up from the sleep mode to the active mode. This current induces noise on the power supply line which is larger than IR-drop at steady state [1]–[5].

Figure 1 shows a schematic figure of power supply line noise in power-gated circuit. Since there is inductance and resistance between external V_{DD} and V_{DD} of logic circuit and capacitance between internal V_{DD} and V_{SS}, when the power switch is turned on, sudden increase of current induces voltage noise. This voltage droop slows down the operation speed of logic circuits for 10 s to several 100 s of clock cycles. If there is only one power domain, this is not a problem because the logic circuit can be kept waiting until V_{DD} settles. Though, in more realistic configuration with multiple power domains as shown in Fig. 2, this noise becomes a problem. In this case, when an "aggressor" block wakes up, neighboring "victim" blocks suffer from reduced supply voltage and causes malfunction, which makes it difficult to effectively sleep/wake-up circuit blocks at high frequency.

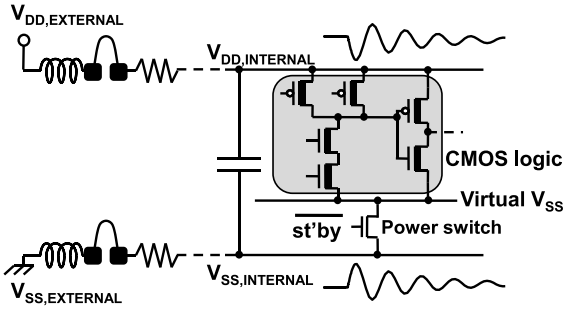

Fig. 1 Power gating and supply line noise.

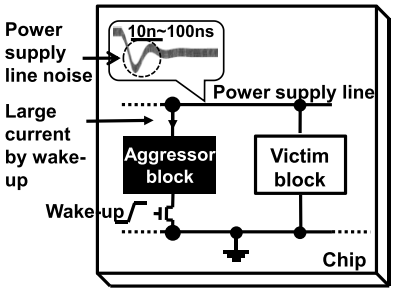

Fig. 2 Multiple blocks share same power supply.

To quantitatively analyze this noise, the power supply line can be approximated as R and L as shown in Fig. 3. C represents all the capacitance connected to the power supply node, including additional decoupling capacitor. I represents the load current. V_{DDINT} is the effective power supply voltage with which the logic circuit works. The load current at wake-up is modeled as a step current of I_0. This step current induces a transitional noise caused by L and C to V_{DDINT}. Assuming $R \ll 1\ \Omega$ and neglecting damping effect, the minimum voltage of V_{DDINT} can be approximated as

$$V_{DDINT\_min} \approx V_{DD} - RI_0 - \sqrt{\frac{L}{C}}\, I_0 \tag{1}$$

The third term, $-\sqrt{\frac{L}{C}}\, I_0$, is the most significant noise

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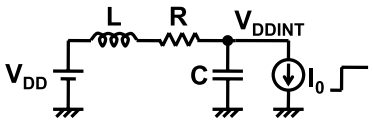

Fig. 3 Simple model of power supply noise.

when the circuit wakes up. From Eq. (1), less L, more C, or less I_0 can reduce this noise. Reducing L is equivalent to allocate more I/O pads for the power supply. This is difficult since 3 times more pads are required to reduce the noise to 50% and power supply already occupies large portion of the pads. Increasing C is also difficult since large decoupling capacitor is already added to the design, and adding more decoupling capacitor directly increase the chip cost. There are some techniques to increase virtual decoupling capacitance [6]–[8], though they are based on amplifier or comparator which consumes not negligible standby power. The final possibility, decreasing I_0 is to wake-up slowly dividing into several steps of I_0 [9]. Since it takes several intervals ($\sim 2\pi\sqrt{LC}$) for V_{DDINT} to settle, this approach results in slower wake-up.

In this paper, a technique to reduce the transition noise with the aid of higher voltage supply to reduce I_0 is proposed [10] and the effectiveness is verified through experiments. In Sect. 2, the basic concept of the noise canceller is introduced followed by the implementation of the noise canceller in Sect. 3. Sections 4 and 5 are dedicated for design considerations and conclusions.

2. Basic Concept of the Noise Canceller

Figure 4 shows the basic concept of the noise canceller. The transistor labeled M_{INJECT} and power supply V_{DDH} which are added to the V_{DDINT} node reduces power supply noise. The circuit configuration and schematic waveforms of V_{DDINT} and I with and without noise canceller are shown in Fig. 5. Neglecting the current supplied from $C_{\mathrm{DECOUPLING}}$, as shown in Fig. 5(a), without noise canceller all the load current I is supplied through the impedance of power supply lines, namely Z_{VDD} and Z_{VSS}. Step increase of I induces noise of $\left(R+\sqrt{\frac{L}{C}}\right) I_0$ as mentioned in Sect. 1. Fig. 5(b) shows the waveforms of V_{DDHINT}, V_{DDINT}, I_{VDD}, and I_{VDDH} with canceller. Detailed switch timing will be explained in Sect. 4. When the logic circuit wakes up, the PMOS switch between V_{DDHINT} and V_{DDINT} is also turned on to pull up V_{DDINT}. Since $I = I_{\mathrm{VDD}} + I_{\mathrm{VDDH}}$, $I_{\mathrm{VDD}} = I - I_{\mathrm{VDDH}}$ which means I_{VDD} is reduced as in the right figure of Fig. 5(b) and this reduces the noise $V_{\mathrm{DD}} - V_{\mathrm{DDINT}} = Z_{\mathrm{VDD}} \times I_{\mathrm{VDD}}$. Though V_{DDHINT} has a large noise, the capacitance between V_{DDHINT} and V_{DDINT} is much smaller (parasitic only) than $C_{\mathrm{DECOUPLING}}$, and consequently this noise does not affect V_{DDINT}.

The noise canceller requires an extra power supply line for V_{DDH}, though this line can be much smaller than the V_{DD} supply since the voltage drop across Z_{VDD} can be as large as $V_{\mathrm{DDH}} - V_{\mathrm{DD}} + V_{\mathrm{DS\_SW}}$, where $V_{\mathrm{DS\_SW}}$ is the minimum drain-source voltage of the M_{INJECT} transistor to supply I_{VDDH}.

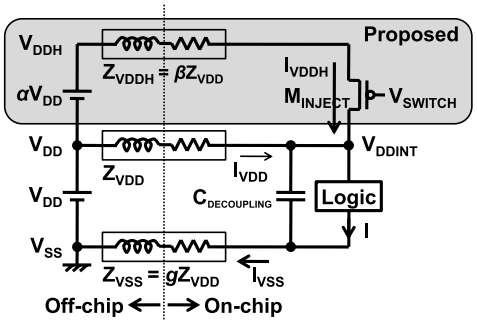

Fig. 4 Basic concept of the noise canceller.

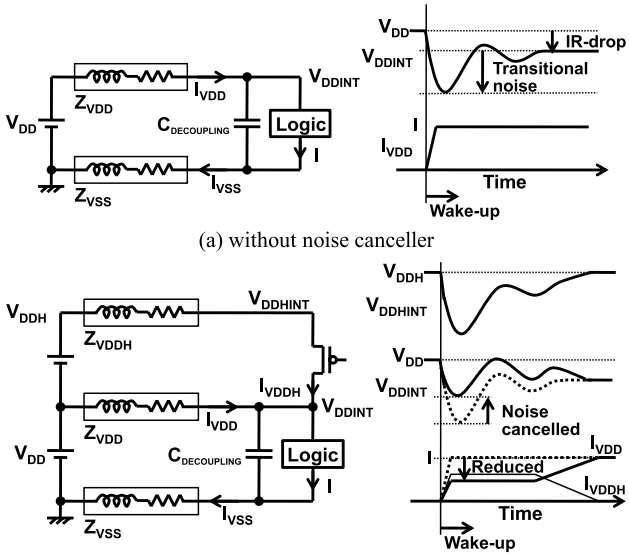

Fig. 5 Configuration and schematic waveform of with and without noise canceller.

In order to quantitatively discuss the noise reduction by the canceller, let us introduce the following four parameters: a high voltage factor α, a higher voltage supply impedance factor β, a ground impedance factor g, and a noise reduction factor γ. Figure 4 also shows parameters α, β, g.

The noise reduction factor γ is defined as:

$$\gamma = \frac{(V_{\mathrm{DD}} - V_{\mathrm{LOCAL\_min}})_{\mathrm{w\ canceller}}}{(V_{\mathrm{DD}} - V_{\mathrm{LOCAL\_min}})_{\mathrm{w/o\ canceller}}}$$
$$\text{where } V_{\mathrm{LOCAL}} = V_{\mathrm{DDINT}} - V_{\mathrm{SSINT}},$$
$$\text{and } V_{\mathrm{LOCAL\_min}} \text{ is the minimum of } V_{\mathrm{LOCAL}}. \quad (2)$$

Assuming $V_{\mathrm{min}} = V_{\mathrm{DD}} - (1+g) Z_{\mathrm{VDD}} I$ without canceller, with canceller I_{VDDH} and new I_{VDD}, namely I'_{VDD}, can be written as:

$$I_{\mathrm{VDDH}} = \frac{\alpha V_{\mathrm{DD}} + Z_{\mathrm{VDD}} I'_{\mathrm{VDD}}}{\beta Z_{\mathrm{VDD}}}, \quad (3)$$

$$I'_{\mathrm{VDD}} + I_{\mathrm{VDDH}} = I. \quad (4)$$

From Eqs. (3) and (4), I'_{VDD} is

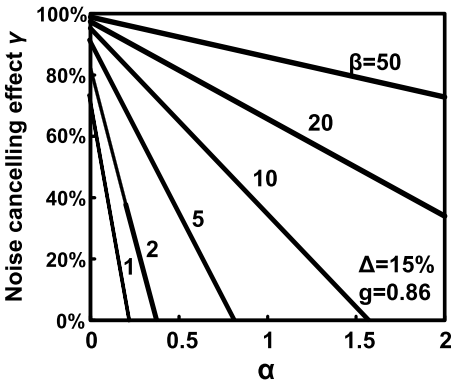

Fig. 6 High voltage factor vs noise cancelling effect.

$$I'_{\mathrm{VDD}} = \frac{\beta}{1+\beta} I - \frac{\alpha}{1+\beta} \frac{V_{\mathrm{DD}}}{Z_{\mathrm{VDD}}}.$$

Thus, $V_{\min} = \left(1 + \frac{\alpha}{1+\beta}\right) V_{\mathrm{DD}} - \left(\frac{\beta}{1+\beta} + g\right) Z_{\mathrm{VDD}} I$

$$\gamma = \frac{\left(\frac{\beta}{1+\beta} + g\right) Z_{\mathrm{VDD}} I - \frac{\alpha}{1+\beta} V_{\mathrm{DD}}}{(1+g) Z_{\mathrm{VDD}} I}$$

$$= \frac{g}{1+g} + \frac{\beta}{(1+g)(1+\beta)} - \frac{\alpha}{(1+g)(1+\beta)\Delta},$$

where

$\Delta = V_{\mathrm{DD}} - V_{\min}$ without noise canceller. (5)

Figure 6 shows the noise reduction factor for typical parameters ($g = 0.86, \Delta = 15\%$) with multiple α and β based on Eq.(5). If $\alpha = 1 (V_{\mathrm{DDH}} = 2V_{\mathrm{DD}})$, even if β is as large as 10, $\gamma \sim 40\%$, which is better cancelling effect than $\beta = 1$ without high voltage. This means large noise reduction can be achieved even with small overhead for additional V_{DDH} supply line.

3. Simulation and Measurement Results

3.1 Circuit Topology

To verify the effectiveness of the noise canceller, a test chip with 530 k-gate equivalent dummy load is designed and manufactured.

Figure 7 shows the measured circuit in 90-nm 1 V CMOS. It uses normal V_{DD} (1.0 V) and higher V_{DD}, namely V_{DDH} (2.0 V). To confirm the proposed canceller can reduce the noise with small wire overhead, only 1 I/O pad is allocated to V_{DDH} while 5 are allocated to V_{DD} and 6 are allocated to V_{SS}. This is $a = 1, b = 5$ configuration in Sect. 2.

As a noise source, NMOS switch M2 with on-current of 40 mA, and load capacitance and decoupling capacitance C_{circuit} of 2 nF are implemented to emulate 530 k-gate logic circuit. This noise source is driven by external wake-up signal (Wake-up).

As a noise canceller, a PMOS switch M3 which supplies 32 mA of current from V_{DDH} to V_{DD} at steady state is implemented. M3 is controlled by external control signal,

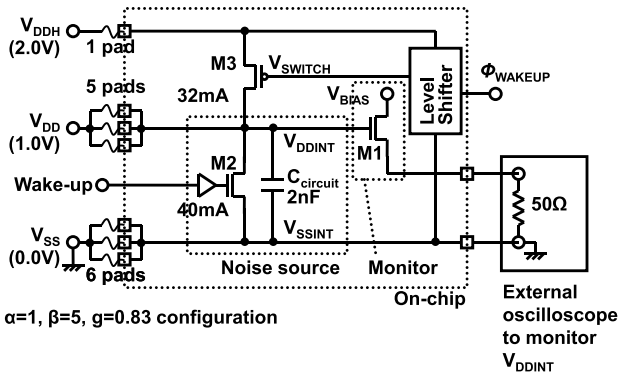

Fig. 7 Schematic of the test chip.

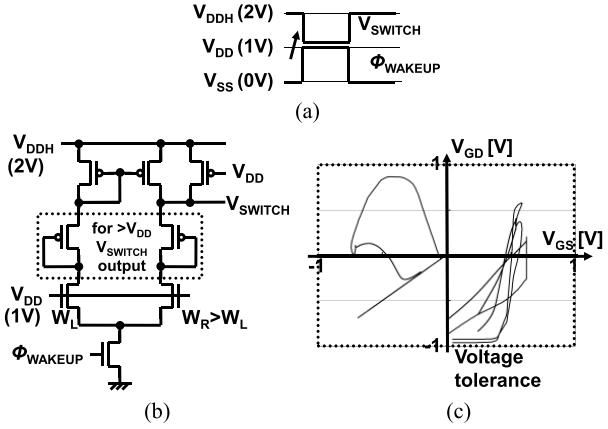

Fig. 8 V_{SS}-V_{DD} to V_{DDH}-V_{DD} level shifter.

namely Φ_{WAKEUP} to test various combinations with Wake-up signal. A V_{SS}-V_{DD} to V_{DD}-V_{DDH} level shifter is also used so that V_{SS} to V_{DD} level Wake-up signal can be also used for Φ_{WAKEUP}, or the control signal can be generated on-chip without higher-V_{DD} tolerant transistors.

On-chip V_{DD} is monitored through source follower M1 with external oscilloscope.

All the transistors here are normal-V_{DD} tolerant transistors.

The level shifter implemented here is shown in Fig. 8. As shown in Fig. 8(a), this level shifter converts V_{SS} to V_{DD} level signal into V_{DDH} to V_{DD} level signal to control M_{INJECT}. Figure 8(b) shows the schematic. The tail transistor is switched by the input signal and since the right-side transistor has larger width than the left-side one, V_{SWITCH} is pulled down to near V_{DD} to turn on the cancelling transistor. V_{SWITCH} is weakly pulled up to V_{DDH} to completely turn off the cancelling transistor when the tail transistor is off. V_{TH} drops of the two diode-connected PMOS are used to avoid below-V_{DD} V_{SWITCH} output. Figure 8(c) shows the gate-source and gate-drain voltage trajectories of the level shifter when 0 to 1.0 V pulse is applied to Φ_{WAKEUP}. This shows that all the transistors operate within their gate oxide tolerance.

3.2 Measurement Results

Figure 9 shows the measured waveforms of the power supply line with and without the noise canceller. Without noise canceller, the minimum voltage of V_{DDINT}-V_{SSINT} during wake-up is about 0.84 V where the steady state voltage with IR-drop is 0.92 V. On the other hand, with proposed noise canceller, the minimum voltage is improved to about 0.89 V, which is 68% noise reduction and $\gamma = (1 - 0.89)/(1 - 0.84) = 0.69$.

A chip microphotograph of the fabricated test chip is shown in Fig. 10. Table 1 shows the specification of the test chip. The noise canceller area is 0.022 mm^2, while the noise source area is 0.21 mm^2. Since this noise source emulates logic circuits with NMOS switch, this current consumption is equivalent to 1.5 mm^2 of 2NAND. Thus the area overhead of the noise canceller can be as small as 1.5% of the load circuit.

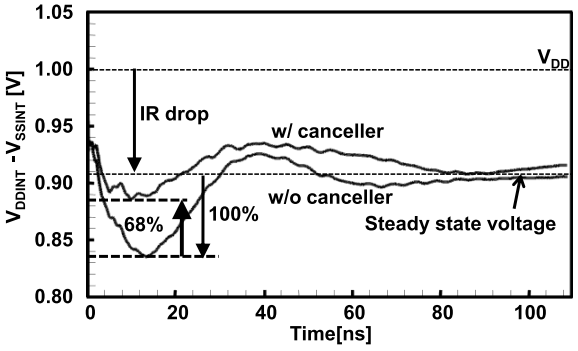

Fig. 9 Measured noise waveform with and without noise canceller.

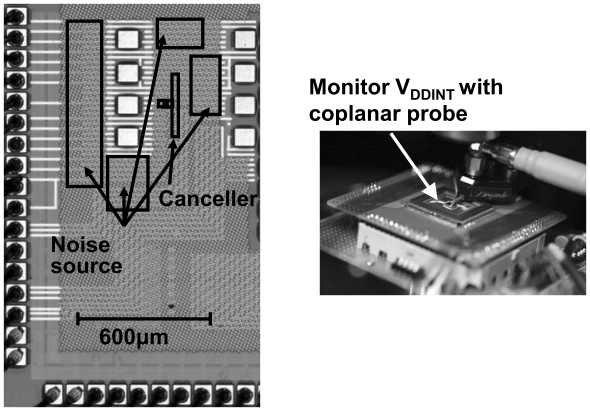

Fig. 10 Chip micrograph and test setup.

Table 1 Specification of the test chip.

Technology	90nm 1V CMOS
Area	Canceller 0.022mm^2 Noise source 0.21mm^2 ~1.5mm^2 * (2NAND equivalent)
Area overhead	1.5% *

4. Design Consideration

Improved control methodologies for proposed canceller are discussed in this section.

4.1 Turn-On Control

One straightforward method to control the cancelling transistor M_{INJECT} is to compare V_{DDINT} with a reference voltage V_{REF} and turns on if $V_{\mathrm{DDINT}} < V_{\mathrm{REF}}$. This method has several problems. One is its stability. If V_{DDINT} exceeds V_{REF} τ_d seconds after turning-on M_{INJECT}, this circuit will oscillate with the period of τ_d. To avoid this oscillation, hysteresis with $V_{\mathrm{REF\_ON}}$ and $V_{\mathrm{REF\_OFF}}$ can be used.

Another problem is the detection delay. Since the noise is relatively fast, turn-on delay of the canceller has a large impact on noise reduction. Figure 11 shows the simulated relationship between turn-on delay and noise cancelling effect, or $1-\gamma$. Cancelling effect goes down to zero with 10 ns of delay. To turn-off the cancelling transistor, V_{REF} must be lower than the steady state voltage, V_{DD}-RI, whose delay is also shown in Fig. 11 as "Steady state voltage." Here, noise cancelling effect is approximately 2/3 of that without delay, and if dual V_{REF} is used, the effect is further reduced.

To solve these problems, the transistor is turned on as soon as the circuit wakes up. In other words, in order to achieve the quickest turn-on, the transition of V_{SWITCH} from H to L should be as sharp as possible. This method does not require a comparator, and is practical since the noise canceller can know when the circuit wakes up.

4.2 Turn-Off Control

After the first droop is cancelled by the proposed canceller, how should it be turned off? In a configuration where $I_{\mathrm{VDDH}} = I$ and $I_{\mathrm{VDD}} = 0$, if M_{INJECT} is turned off as a step function, I_{VDD} results in step increase of I, which induces same amount of noise without canceller. Thus, M_{INJECT} has to be turned off slowly enough not to induce another noise.

Figure 12 shows the measured waveforms of V_{DDINT}-V_{SSINT} for several turnoff slopes. t_{OFF} is the time to turn

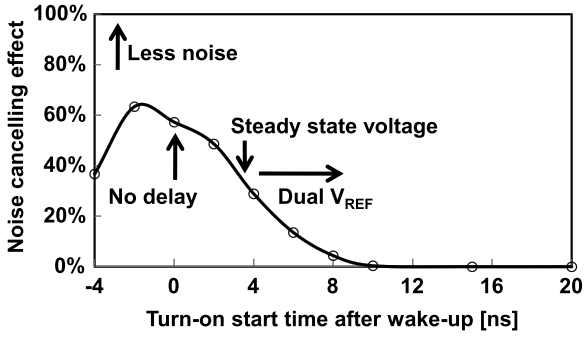

Fig. 11 Turn-on delay vs noise cancelling effect.

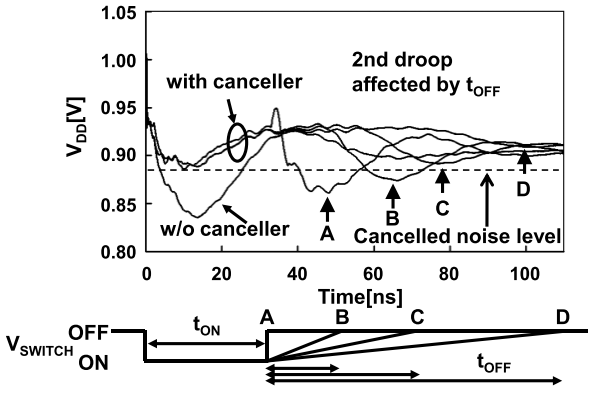

Fig. 12 Measured turn-off time vs noise.

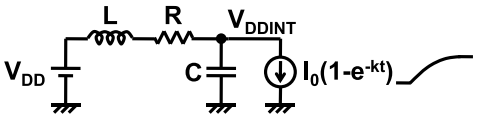

Fig. 13 A simple model to evaluate turn-off time.

off M_{INJECT}. A, B, C and D have t_{OFF} of 0 ns, 20 ns, 40 ns, and 80 ns, respectively. A and B have 2nd noise which is larger than the cancelled noise, on the other hand, C and D has smaller 2nd noise. From this, it is shown that slower turn-off is necessary not to abandon cancelling effect.

To quantitatively analyze t_{OFF}, let us think of a simple model shown in Fig. 13. All power supply impedance is approximated as L and R, and all circuit and decoupling capacitance is approximated as C. Because decrease of I_{VDDH} is equivalent to increase of I_{VDD}, turn-off of M_{INJECT} is modeled as increase of I. For simplicity, current of $I = I_0\left(1 - e^{-kt}\right)$ is used. In this model, the condition that transitional noise is smaller than IR-drop, or $V_{\mathrm{DDINT\_MIN}} \geq V_{\mathrm{DD}} - RI_0$ is achieved when

$$k \leq \frac{R}{2L}.$$

Assuming the noise is determined by largest dI/dt, this condition can be written as

$$t_{\mathrm{OFF}} \geq \frac{2L}{R}. \tag{6}$$

In the measured circuit, this value is around 60 ns. Figure 14 shows the measured V_{min} for various t_{OFF} and t_{ON}. As mentioned before, with t_{OFF} of 0 ns, 2nd droop is larger than the cancelled noise in any t_{ON}. With t_{OFF} of 40 ns and 80 ns, 2nd droop is smaller than the cancelled noise and if $t_{\mathrm{ON}} > 10$ ns, noise reduction rate remains constant. From this, design of $t_{\mathrm{OFF}} = \frac{2L}{R}$ does not induce 2nd droop and still has margin not to induce it. Since the canceller is not susceptible to t_{ON}, turning off after the 1st droop ($t_{\mathrm{ON}} \sim \pi\sqrt{LC}$) is preferred because too large t_{ON} results in higher power consumption and too small t_{ON} suffers from side-effects.

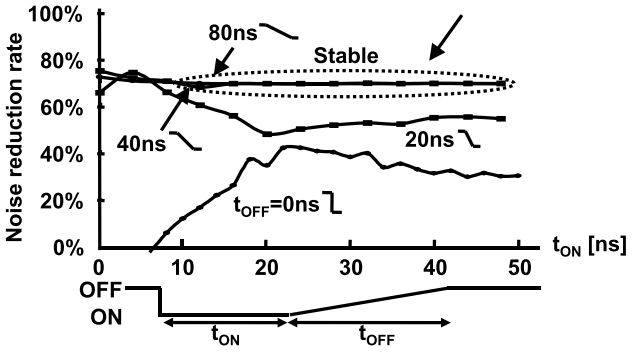

Fig. 14 Turn-off start time vs noise reduction effect.

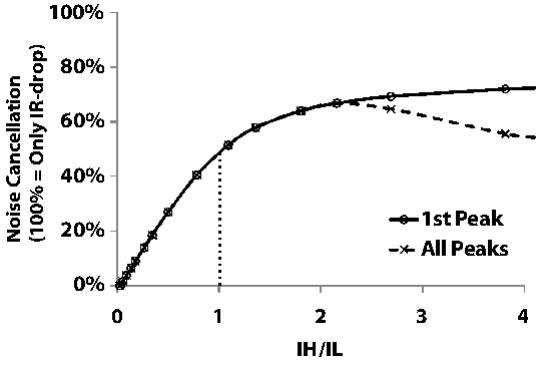

Fig. 15 On-resistance of M_{INJECT} vs noise cancelling effect.

4.3 On-Resistance of the Switching Transistor

In the model of Sect. 2, on-resistance of M_{INJECT} was treated as zero. However, such a transistor tends to be very large and not practical. On-resistance of M_{INJECT} affects the peak I_{VDDH}, which is

$$I_{\mathrm{VDDH}} = \frac{(\alpha + \Delta)\ V_{\mathrm{DD}}}{(1+\beta)R + R_{\mathrm{ON}}}. \tag{7}$$

Figure 15 shows simulated noise R_{ON} vs noise cancellation where IH/IL means $I_{\mathrm{VDDH}}/I_{\mathrm{VDD}}$. As $I_{\mathrm{VDDH}}/I_{\mathrm{VDD}}$ increases, noise cancelling effect linearly increase up to $I_{\mathrm{VDDH}}/I_{\mathrm{VDD}} = 1$. After that point, cancellation effect saturates and 2nd droop becomes significant because long t_{OFF} is required. Furthermore, total power consumption when M_{INJECT} is turned on is

$$V_{\mathrm{DD}} I_{\mathrm{VDD}} + (\alpha + 1)\, V_{\mathrm{DD}} I_{\mathrm{VDDH}} \tag{8}$$

From Eqs. (4), (8) is equal to

$$V_{\mathrm{DD}} I + \alpha\, V_{\mathrm{DD}} I_{\mathrm{VDDH}}. \tag{9}$$

From this, large I_{VDDH} means large power consumption, $I_{\mathrm{VDDH}} = I_{\mathrm{VDD}}$ is a optimum point for setting R_{ON} of M_{INJECT}.

4.4 Power and Area Overhead

Figure 16 shows the measured and calculated power overhead of the proposed noise canceller. Power overhead was

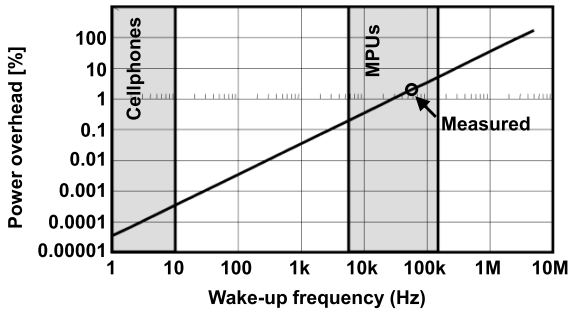

Fig. 16 Wake-up frequency vs power overhead.

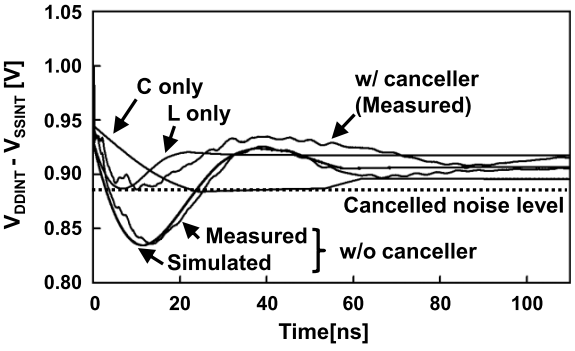

Fig. 17 Noise waveform of passive noise canceller.

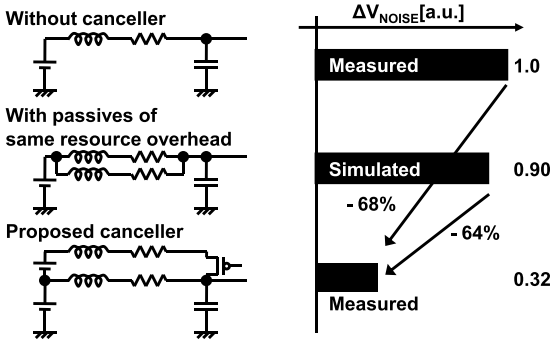

Fig. 18 Noise cancelling effect comparison regarding wire overhead.

about 3% in 50 k wake-ups/s. Since the charge injected from V_{DDH} to V_{DDINT} is constant, power overhead depends on the frequency of sleep/wake-up. In the measured case, maximum frequency under power overhead of 5% is around 100 kHz, which is the upper bound frequency of practical noise cancelling with the proposed canceller.

Comparison with passive countermeasures is shown in Fig. 17. Measured noise waveforms with and without proposed noise canceller and simulated waveforms which are fit to the cancelled noise level with increasing C or decreasing L are shown. To obtain same noise reduction, 77 times as much C or 45 times as small L is required, whose overhead is to large to implement.

Comparison with same overhead is shown in Fig. 18. Normalized to noise without canceller, if Z_{VDDH} is also used for Z_{VDD}, noise is reduced to 90%. This configuration has the same wire overhead as the proposed noise canceller, while the proposed canceller reduces noise to 32%, which is 64% noise reduction from same wire overhead.

5. Conclusions

A power supply noise canceller for transitional noise at power gating or frequency hopping wake-up is proposed and 68% noise reduction is experimentally verified for load current and capacitance equivalent to 530 k NAND gates. This enables the power consumption reduction in power gating systems by frequent wake-ups without affecting neighboring blocks' operation. To confirm the effectiveness of the proposed canceller, general design methodologies are shown.

Acknowledgments

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