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A 100 Mbps, 4.1 pJ/bit Threshold Detection-Based Impulse Radio UWB Transceiver in 90 nm CMOS

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SUMMARY A novel DC-to-960 MHz impulse radio ultra-wideband (IR-UWB) transceiver based on threshold detection technique is developed. It features a digital pulse-shaping transmitter, a DC power-free pulse discriminator and an error-recovery phase-frequency detector. The developed transceiver in 90 nm CMOS achieves the lowest energy consumption of 2.2 pJ/bit transmitter and 1.9 pJ/bit receiver at 100 Mbps in the UWB transceivers.

key words: *impulse radio ultra-wideband (IR-UWB), digital pulse-shaping, pulse discriminator, error-recovery phase-frequency detector*

1. Introduction

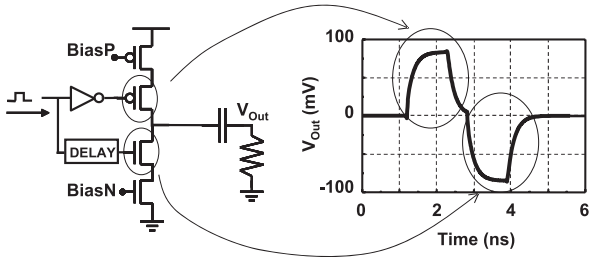
UWB communication systems can be broadly classified as impulse radio UWB (IR-UWB) and multi-carrier UWB. For IR-UWB, multi-user detectors (MUD) and hybrid RAKE/MUD-UWB transceivers for robust narrowband interference suppression are becoming popular [1]. However, a simple, single clocked-correlator transceiver or threshold detector can also be used for short distance and high SNR environments [2], [3].

In this paper a novel DC-960 MHz impulse radio UWB (IR-UWB) transceiver is proposed for the low power ad-hoc wireless sensor networks [4], [5]. These ubiquitous networks require that the individual nodes are tiny, easily integratable into the environment, and have negligible cost. The proposed transceiver features a digital pulse-shaping transmitter, a DC power-free pulse discriminator and an error-recovery phase-frequency detector (PFD), thereby achieving extremely low power consumption at 100 Mbps.

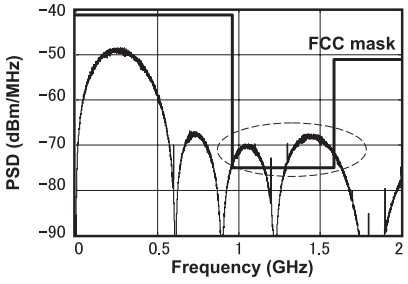
2. Digital Pulse-Shaping Transmitter

Gaussian first derivative or second derivative pulse is often used as IR-UWB pulse signals. In this work, a novel digital pulse-shaping technique is proposed to generate BPSK modulated Gaussian first derivative pulse. The first-order derivative Gaussian impulse can be expressed as

$$G_1(t) = -A\frac{t}{\sigma}\exp\left(-\frac{t^2}{2\sigma^2}\right) \quad (1)$$



(a)



(b)

Fig. 1 (a) Conventional UWB pulse generator. (b) Modulated transmit spectrum.

where A is the pulse amplitude, t is time, and σ is time constant.

Digital pulse shaping in UWB transmitters (TX's) is a power efficient technique [6]. All the previously reported digital pulse-shaping TX's, however, were developed for above-3 GHz band and no TX for DC-960 MHz band has been reported [7]–[10]. Figure 1(a) shows the simplified topology of the conventional digital pulse-shaping TX. It consists of a triangular pulse generator and an output stage driving 50 Ω load. The input signal and the inverted input generate the upper and the lower pulses respectively.

The simulated transmit spectrum of the conventional UWB pulse generator is shown in Fig. 1(b). The spectrum can not satisfy the FCC EIRP spectrum mask above 1-GHz frequency. To suppress the spectrum above 1-GHz frequency, sequentially operated eight drivers are proposed to shape one pulse. As shown in Fig. 2, the upper and the lower pulses are divided to eight parts respectively and every part is shaped by different drivers. For example, the first part of the upper pulse is only shaped by the driver 0 while the second part is shaped by the driver 0 and driver 1 simulta-

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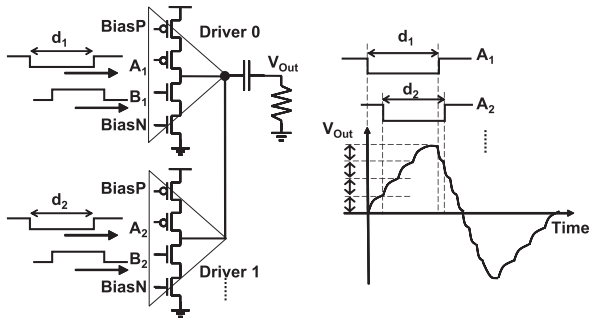
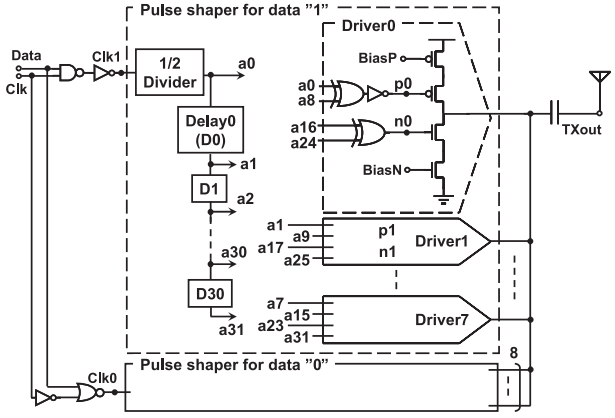
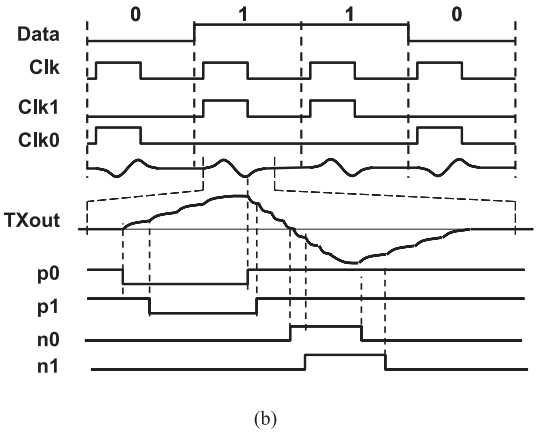


(a) (b)

Fig. 2 (a) Proposed UWB pulse generator. (b) Digital pulse-shaping waveforms.



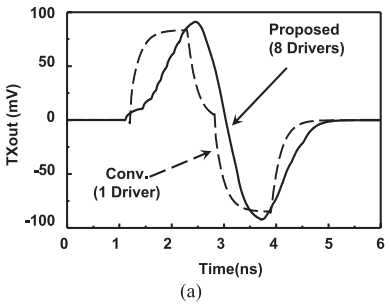
(a)



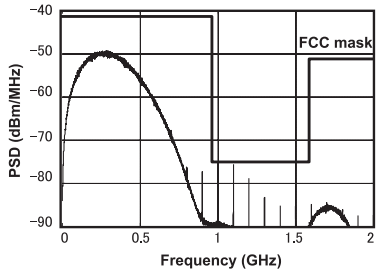
(b)

Fig. 3 (a) Overall view of the proposed digital pulse-shaping transmitter. (b) Timing chart.

neously. Figure 3(a) shows the overall view of the proposed digital transmitter. It consists of two pulse shapers for data "1" and data "0" respectively and each shaper is composed of eight drivers. The timing of the drivers is determined by the 32-tap delay line. The timing chart of the whole transmitter is shown in Fig. 3(b). The transmitted data serves as the selection signal for the input clock. For the transmitted data "1" and "0," the input clock can pass to the upper



(a)



(b)

Fig. 4 (a) Waveform comparison between conventional and proposed TX. (b) Modulated transmit spectrum of the proposed TX.

shaper and lower shaper respectively.

Figure 4(a) shows the waveform comparison between the conventional TX in Fig. 1(a) and the proposed TX in Fig. 3(a). Simulated transmit spectrum is shown in Fig. 4(b). The developed digital pulse-shaping transmitter with eight drivers can satisfy the FCC mask. With the increased number of the pulse-shaping drivers, the transmit spectrum above 1-GHz frequency can be further suppressed but the power consumption will be increased. Compared to the eight-driver pulse shaper, the four-driver pulse shaper can't satisfy the FCC mask and therefore in this work eight drivers are used to shape the pulse.

3. Receiver with DC Power-Free Pulse Discriminator

An ultra low-power solution for BPSK demodulation is leading edge detection (LED) technique. The LED receiver (RX) is also known as threshold detection-based receiver [2]. The threshold receiver consists of a circuit fast enough to detect the presence of the IR-UWB pulse, and some type of pulse stretcher circuit that outputs a pulse which is long enough for slower logic or analog circuits to process. Figure 5 is the basic block diagram of threshold detection-based receiver. The receiver sets a threshold at the receiver, and any incoming pulse that crosses the threshold is detected and demodulated.

The proposed asynchronous threshold detection-based receiver is shown in Fig. 6(a). It consists of four blocks: a front-end amplifier, a DC power-free pulse discriminator, an error-recovery phase-frequency detector (PFD) and a Reset-Set Flip-Flop (RSFF). Figure 6(b) shows the timing chart of the proposed receiver. The received signal is first amplified by the front-end amplifier and each BPSK symbol is split

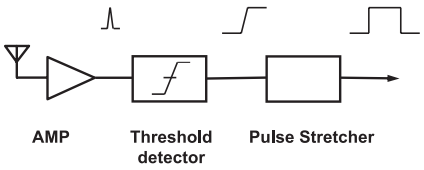


Fig. 5 Block diagram of threshold detection-based UWB receiver.

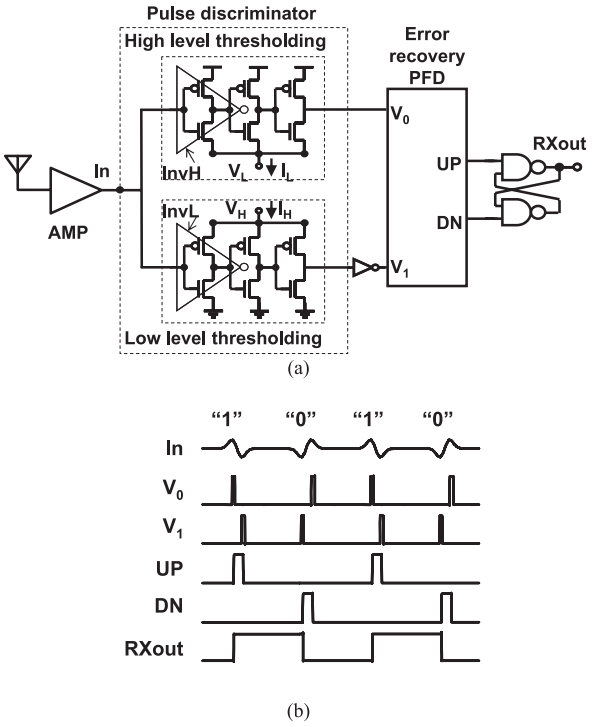


Fig. 6 (a) Circuit schematics of proposed threshold detection-based receiver. (b) Timing chart.

into two pulses V_0 and V_1 by the DC power-free pulse discriminator. Then the first incoming edge of the two pulses is detected by the PFD and the RSFF converts the detection result to the corresponding data bit.

3.1 DC Power-Free Pulse Discriminator

Conventionally, an amplifier and a comparator are combined as a threshold detector. The major disadvantage of this topology is large DC power dissipation that occurs even for no AC input. In the transmitted BPSK signal, the circuit spends long periods of time with no AC signal. Power dissipated in these periods is wasted. In this study, a novel DC power-free pulse discriminator is proposed to discriminate the received signal.

The proposed pulse discriminator is based on the conventional CMOS inverter. As shown in Fig. 7(a), two inverters InvH and InvL are employed to detect the positive pulse and negative pulse respectively. The source of the inverter InvH is biased to V_L (=ΔV) while the drain of the inverter InvL is biased to V_H (=$V_{DD} - \Delta V$). The gate inputs of the two inverters are both biased to V_{DD} /2. The logical

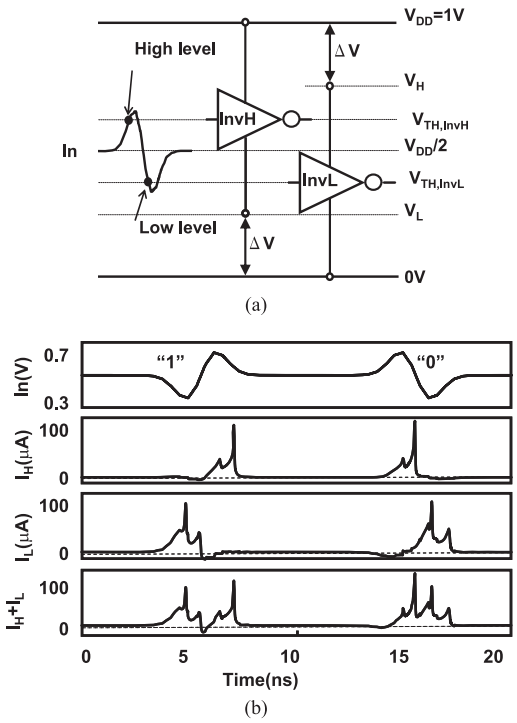


Fig. 7 DC power free pulse discriminator. (a) Operation principle. (b) Simulated waveforms.

thresholds of the two inverters are labeled as $V_{TH,InvH}$ and $V_{TH,InvH}$ respectively. When the amplitude of the received signal is larger than $V_{TH,InvH}$ or less than $V_{TH,InvL}$, the pulse is detected and the power is only consumed on this period. The simulated waveforms of the received signal and power supply current of the two inverters are shown in Fig. 7(b). The proposed DC power free pulse discriminator consumes essentially zero power dissipation for no AC input.

3.2 Error-Recovery Phase-Frequency Detector

The received signal can be demodulated by detecting the first incoming edge of the two pulses V_0 and V_1. Figure 8 (a) shows the conventional PFD implementation to detect the first incoming edge of the discriminator output. It consists of two edge-triggered D flip-flops with D input tied to logical ONE. The output of the pulse discriminator, V_0 and V_1, serves as the clocks of the flip-flops. As shown in Fig. 8(b), if the PFD output UP and DN are low and V_0 goes high, the signal UP rises. If this is followed by a rising transition on V_1, the signal DN will go high and the AND gate will reset both flip-flops. In other words, to generate the reset signal RST, UP and DN are simultaneously high for a short time which should be avoided as the input signal for the following RSFF. To eliminate the simultaneous high output, two delay cells with delay time t_0, placed on the XOR gate inputs, are used to compensate the time delay of the AND gate [11].

The conventional PFD employs sequential logic to create three-status and respond to the rising edges of the two

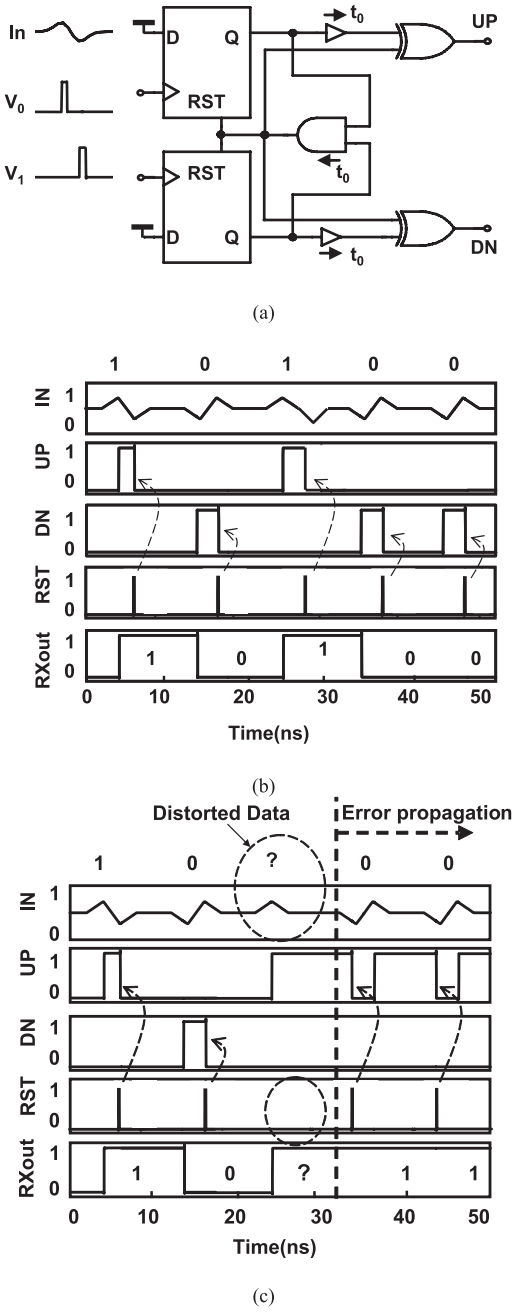


Fig. 8 Conventional PFD. (a) Circuit schematics. (b) Normal operation (RXout is shown in Fig. 6). (c) Error propagation due to distorted signal.

inputs. The output of sequential circuits depends not only on the current inputs, but also on the previous values. The bit error in the previous cycle will be carried over to the subsequent cycles. Figure 8(c) shows the bit error propagation due to distorted signal. At the third data bit, the AND gate of the PFD is failed to generate the reset signal because V_1 is missed by the pulse discriminator due to the distorted signal "1." The reset signal RST generated by the following rising edge of V_1 in the next period changes the time sequence of the PFD and causes bit error.

To avoid the bit-error propagation due to the distorted

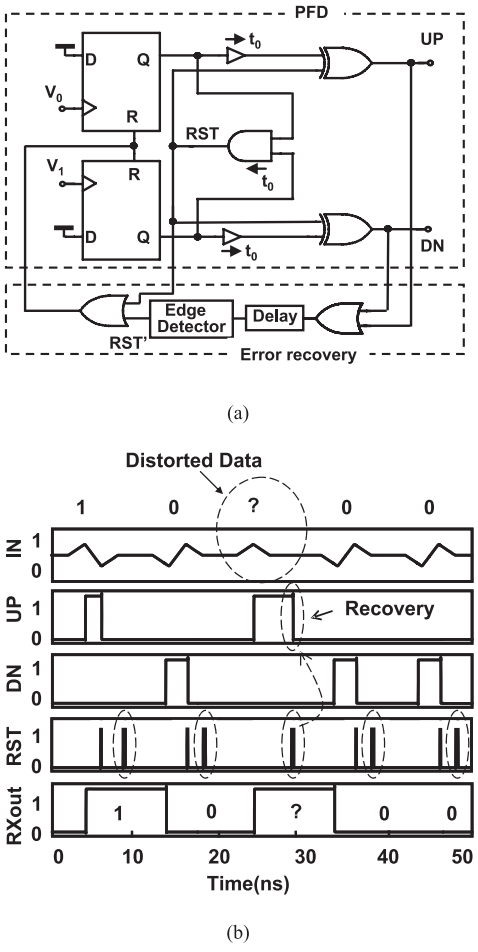


Fig. 9 Proposed error-recovery phase-frequency detector. (a) Circuit schematics. (b) Error-recovery operation (RXout is shown in Fig. 6).

received signal, an auxiliary reset signal RST′, as shown in Fig. 9(a), is fed back to the PFD input to force the reset operation in every period. The error-recovery circuits consist of a delay cell, an edge detector and two OR gates. The auxiliary reset signal RST′ is generated by combing the delayed rising edges of the output UP and DN. In this design, since the pulse width is 4 ns and the pulse period is 10 ns, the delay time of the delay cell should be larger than 4 ns and less than 10 ns. Figure 9(b) shows the simulated waveforms for the distorted data "10100." Compared to Fig. 8(c), two rest signals are employed to reset the flip-flops for the normal data bit in every period. For the distorted data bit "1," the primary reset signal RST is missed by the pulse discriminator but the auxiliary reset signal RST′ resets the PFD output to zero and blocks the potential bit-error propagation. However, if V_0 is missed by the pulse discriminator due to the distorted signal, the PFD output UP will keep low and it cannot set the output of the following RS-latch to high level. In this case, one bit error will occur but the potential bit error propagation can still be blocked by the auxiliary reset signal.

4. Experimental Results

The proposed digital pulse-shaping transmitter and the DC power-free receiver without front-end amplifier were designed and fabricated in 90 nm CMOS process. Figure 10 shows the micrograph and the layout of the transceiver. The core area of the transmitter and the receiver are 9075 μm^2 and 576 μm^2 respectively.

Figure 11(a) shows the measured waveform of the transmitter. The measured pulse amplitude is 115 mV and the pulse period is 10 ns. The measured BPSK modulated transmit spectrum is shown in Fig. 11(b). It can be seen that the proposed digital pulse-shaping transmitter can suppress the spectrum above 1 GHz and satisfy the FCC EIRP spectrum mask. Figure 12 shows the measured waveform of the receiver. To verify the error-recovery PFD, the fifth bit of the input data is distorted intentionally. As indicated in Fig. 9(b), the potential error propagation due to distorted signal "1" is blocked by the auxiliary error-recovery reset

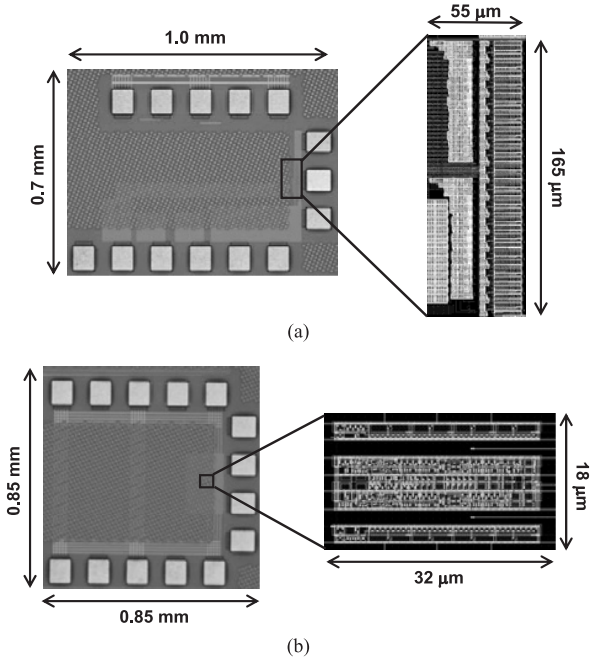


Fig. 10 Chip micrographs and layout. (a) Transmitter. (b) Receiver without front-end amplifier.

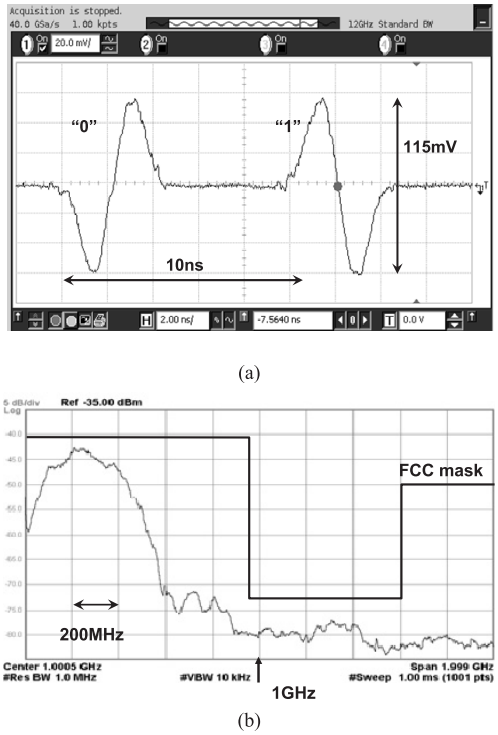


Fig. 11 Measured transmitter output at 100 Mbps. (a) Waveform. (b) Spectrum.

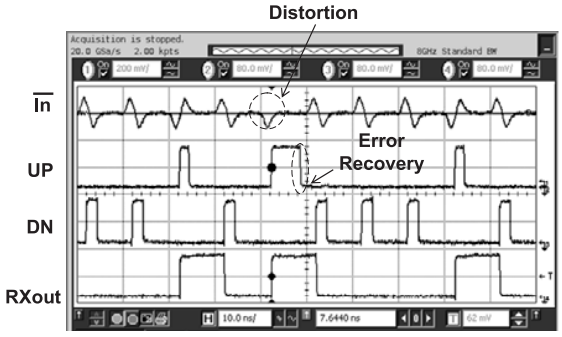


Fig. 12 Measured receiver waveforms for distorted data "10100."

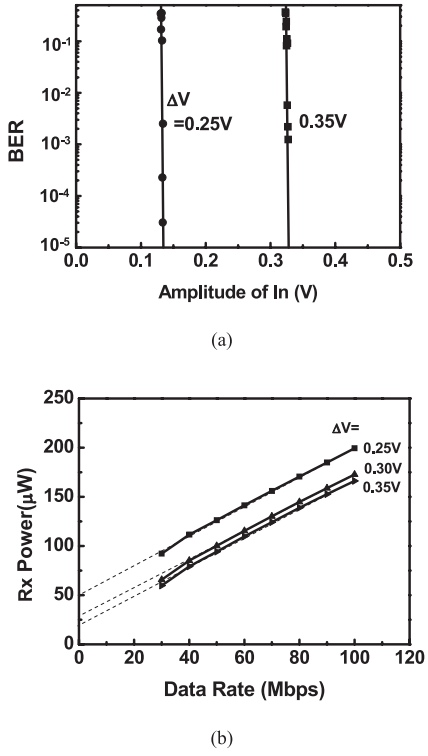
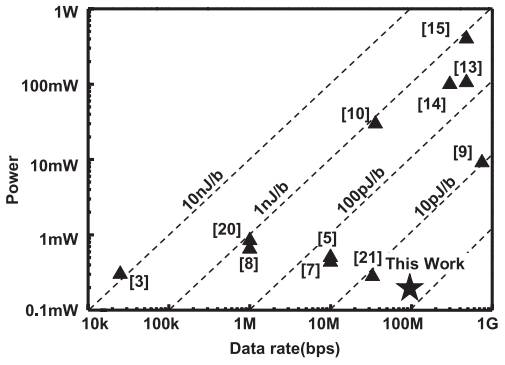


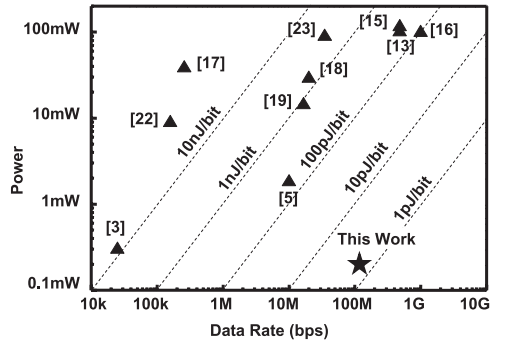
Fig. 13 Measured receiver characteristics. (a) BER vs. Amp. (b) Power vs. data rate.

Table 1 Performance summary.

Technology		90nm CMOS
Supply Voltage		1.0V
Data Rate		100Mbps
Power@ 100Mb/s	TX	220μW
	RX	190μW
Energy per bit	TX	2.2pJ/bit
	RX	1.9pJ/bit
Core Area	TX	55μm × 165μm
	RX	18μm × 32μm
Modulation		BPSK



(a)



(b)

Fig. 14 Comparison with the state-of-the-art UWB transceivers. (a) Transmitter. (b) Receiver.

signal. The measured BER at different threshold of pulse discriminator are shown in Fig. 13(a). Figure 13(b) shows the measured RX power dependence on data rate at different threshold of pulse discriminator. The tradeoff relationship between the receiver sensitivity and the power consumption is tuned by ΔV. To increase the sensitivity of the receiver, the bias voltage ΔV should be reduced but the power consumption will be increased. However, since the worst-case power consumption is only $220\,\mu$W and it is not a dominating factor in the real application, a simplified constant bias voltage generator for the proposed pulse discriminator can also be used. The proposed DC power-free pulse discriminator enables data rate dependent power. The measured transceiver performance is summarized in Table 1.

Figure 14 shows energy and power comparison with state-of-the-art UWB transceivers. The proposed digital pulse-shaping transmitter and the DC power-free receiver achieves the lowest energy consumption of 2.2 J/bit and 1.9 pJ/bit respectively at 100 Mb/s, and potentially a promising technology for low-complexity wireless communications.

5. Conclusions

A novel DC-to-960 MHz impulse radio UWB (IR-UWB) transceiver with digital pulse-shaping transmitter, DC power-free pulse discriminator and error-recovery phase-frequency detector is proposed for ad-hoc wireless sensor networks. The digital pulse-shaping transmitter shapes one pulse with eight sequentially operated drivers to suppress the spectrum above 1 GHz. The proposed pulse discriminator has essentially zero power dissipation for no AC input and the error-recovery phase-frequency detector can block the error propagation due to distorted received signal. Therefore, the transceiver in 90 nm CMOS achieves the lowest energy consumption of 2.2 J/bit TX and 1.9 pJ/bit RX (without front-end amplifier) in the state-of-the-art UWB transceivers at 100 Mbps, and potentially a promising technology for low-complexity wireless communications.

Acknowledgments

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