A 1.28mW 100Mb/s Impulse UWB Receiver with Charge-Domain Correlator and Embedded Sliding Scheme for Data Synchronization

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Abstract

A 1.8V 1.28mW 100Mb/s impulse UWB receiver in 0.18μm CMOS for DC-960MHz band is developed. The proposed receiver features a DC power-free charge-domain sampling correlator and an embedded sliding scheme for data synchronization, thereby achieving the lowest energy of 12.8pJ/bit in the state-of-the-art correlation-based UWB receivers.

Introduction

Impulse radio ultra-wideband (IR-UWB) receiver can be classified as threshold-detection based receiver [1, 2] and correlation based receiver [3]-[5]. Performance comparison of different topologies is shown in Fig.1. Figs. 1(a) and (b) show the simulated UWB environments with narrowband interference and band-limited white noise in frequency domain and time domain, respectively. The simulated BER of various topologies is shown in Fig.1 (c). When the amplitude of the interference and the noise are much larger than the received UWB pulse as shown in Fig. 1(b), threshold-detection based receiver can't work at all. In contrast, correlation based UWB receiver can still attain superior BER due to the correlation between the received signal and the template signal of the correlator.

To achieve the correlation operation, the template of the correlator must be synchronized with the received signal. Conventionally, synchronization circuits are implemented with PLL or DLL at the expense of increased circuit complexity and increased power consumption [5]. In this paper, low power correlation based receiver with a charge-domain correlator and an embedded sliding circuits for data synchronization is proposed.

Receiver Architecture

The proposed topology of the receiver is shown in Fig. 2. The received signal is first amplified by the front-end amplifier and then correlated with the discrete template of the charge-domain correlator. Correlation results are detected by the following comparators and SR latch convert the comparison results to the corresponding data bit. If the amplitude of the correlator output V_{cor} is not large enough to trigger the comparators, data synchronization process will be activated. The proposed sliding scheme can slide the phases of sampling clocks until synchronization is achieved.

DC Power-Free Charge-Domain Correlator

One low-power solution for analog design is discrete-time charge-domain technique. In the literature [6] and [7], addition-based charge-domain technique is introduced to the design of mixer and filter. In this work, a novel charge-domain correlator based on both addition and subtraction is proposed. Fig. 3(a) shows the operation of the correlator. The received DC-960MHz band Gaussian first-order derivative pulse is sampled at 2GSa/s and correlated with the discrete template determined by the capacitor value in the correlator. Since the pulse is odd symmetric and the pulse width is 4ns, only six sampling points are non-zero and six capacitance values C_1, C_2, C_3, $-C_3$, $-C_2$ and $-C_1$ can be used to represent the discrete template for 100Mb/s date rate correlation. As shown in Fig. 3(b), sampling operation is implemented by turning on the switches controlled by clocks ϕ_1, $\phi_2 \ldots \phi_7$ sequentially and sampling results are stored in the capacitors as V_1, $V_2 \ldots V_7$ respectively. In Fig. 3(c), the stored voltages are weighted summed and averaged by turning on all the ϕ_r controlled switches. Subtraction operation is implemented by exchanging the two plate connections of the capacitors. After summing and averaging, the correlator output is reset to $V_{DD}/2$ by clock ϕ_r .

Sliding Scheme for Data Synchronization

Unlike the data synchronization by using the tapped delay-lines [3] or the digital baseband [5], the proposed sliding scheme enables the data synchronization with simple circuits by utilizing the 2GHz clock for the sampling correlator. The circuits and the timing chart of the proposed sliding scheme are shown in Fig.4 and Fig.5 respectively. Before the synchronization is achieved, V_{cor} is small and is not detected by the DC-power free comparators [1]. In this case, neither UP nor DN is generated and the clock removal signal (RM) is generated to increase the period of ϕ_0 from 10ns to 10.5ns. The sliding scheme finishes the synchronization process within 19 slides, because the period of input signal is equals to 10ns and differs with ϕ_0 by 0.5ns. After the synchronization is achieved, V_{cor} is large and is detected by the comparators. In this case, either UP or DN is generated and RM is not generated, which keeps the ϕ_0 period 10ns. The 20-phase clock is generated by combining the output edges of the divide-by-5 divider and the divide-by-4 divider.

Experimental Results

The proposed receiver without front-end amplifier was designed and fabricated in 0.18μm CMOS process. The micrograph is shown in Fig. 6 and the performance is summarized in Table I. Fig. 7 shows the measured waveforms at 100Mb/s with synchronization circuits disabled and enabled respectively. As indicated in Fig. 5, with and without synchronization circuits, the sampling clock (ϕ_3) period varies from 10ns to 10.5ns. The measured power dependence on data rate and the measured BER dependence on the amplitude of V_{in} at different bias voltage ΔV are shown in Fig. 8(a) and Fig. 8(b) respectively. Small ΔV achieves high sensitivity at the expense of high power consumption. Fig. 9 shows energy and power comparison with the state-of-the-art correlation based UWB receivers. The proposed UWB receiver with charge-domain correlator and embedded sliding scheme for data synchronization achieves the lowest energy consumption of 12.8pJ/bit at 100Mb/s.

Conclusions

The receiver in 0.18μm CMOS achieves the lowest energy consumption of 12.8pJ/bit at 100Mbps in the state-of-the-art correlation-based UWB receivers.

Acknowledgment

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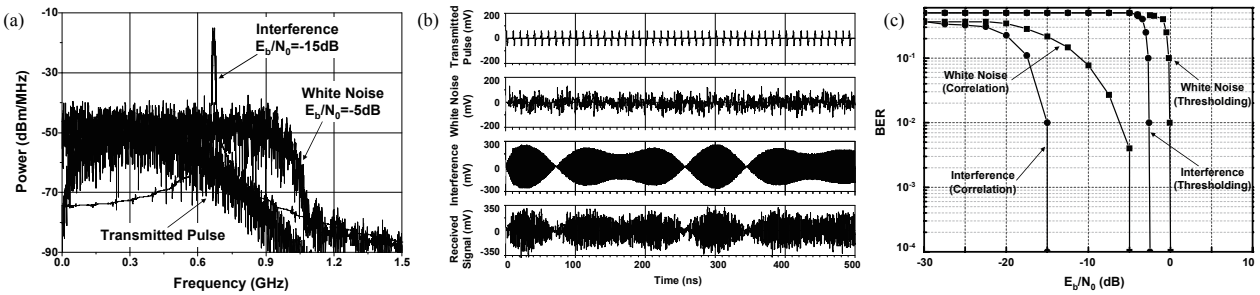


Fig. 1. Simulated UWB environments with narrowband interference and white noise. (a) Frequency domain. (b) Time domain. (c) BER vs. E_b/N_0.

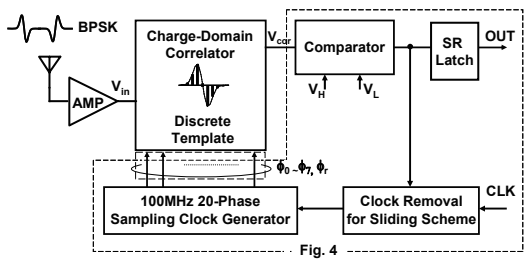


Fig. 2. Impulse UWB receiver with charge-domain correlator and sliding scheme.

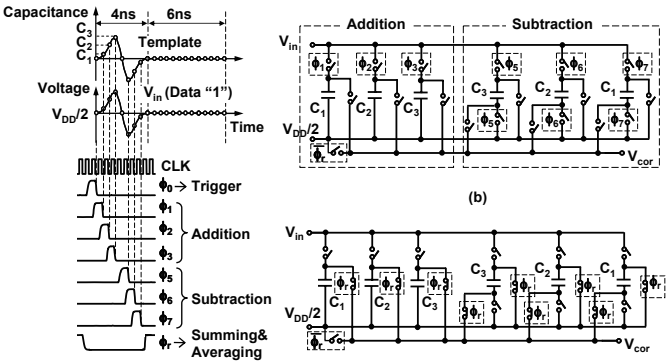


Fig. 3. Charge-domain correlator. (a) Timing chart. (b&c) Circuit schematics in (b) sampling operation and (c) summing and averaging operation.

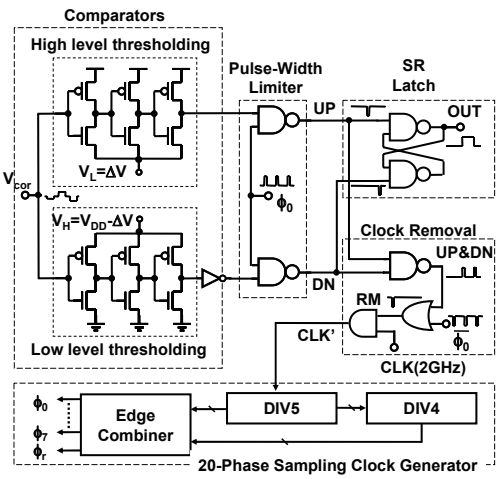


Fig. 4. Circuits for sliding scheme.

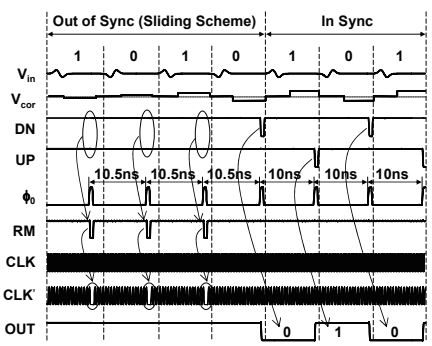


Fig. 5. Timing chart of sliding scheme.

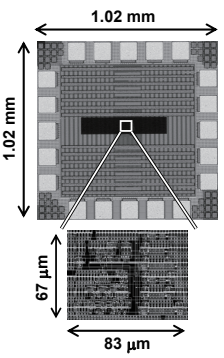


Fig. 6. Micrograph and layout.

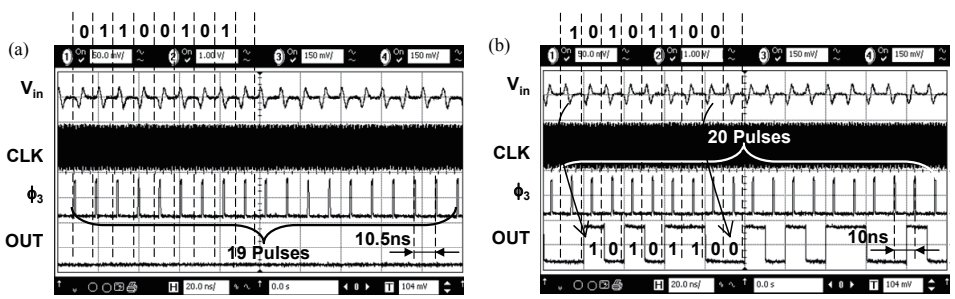
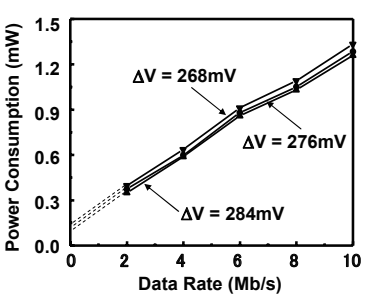


Fig. 7. Measurement results at 100Mb/s. (a) Without sliding scheme. (b) With sliding scheme.

Table. I Performance summary.

Technology		0.18μm CMOS
Supply Voltage		1.8V
Data Rate		100Mbps
Clock Frequency		2GHz
Modulation		BPSK
Power	Correlator & Synchronization	0.63mW
	Clock Generator	0.53mW
	Comparator	0.12mW
	Total	1.28mW
Energy per bit		12.8pJ/bit
Core Area		5561μm²



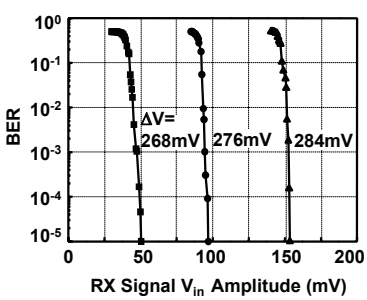


Fig. 8. Measurement results. (a) Power vs. data rate. (b) BER vs. amplitude of Vin.（ΔV is defined in Fig. 4.）

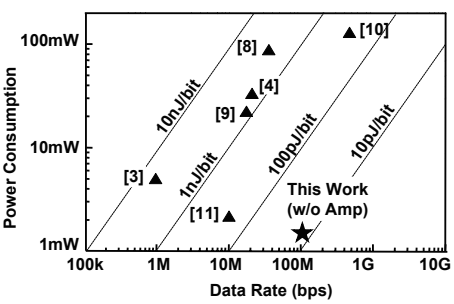


Fig. 9. Comparison with correlation based UWB receivers.