Inductor Design of 20-V Boost Converter for Low Power 3D Solid State Drive with NAND Flash Memories

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ABSTRACT
A 3D-integrated Solid State Drive (SSD) with the boost converter can achieve both the low power and the fast write-operation at the small die area of the NAND flash memory. The performance of the boost converter, however, is critically affected by the inductor, because the output voltage of the boost converter, the rising time, and the energy consumption during the boost are determined by the inductor. Therefore, this paper proposes a spiral inductor design of the boost converter for the 3D SSD. By using the boost converter with the optimized inductor, the energy during write-operation of the proposed 1.8-V 3D-SSD is decreased by 68% compared with the conventional 3.3-V 3D-SSD with the charge pump.

Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]: General

General Terms
Measurement, Performance, Design, Experimentation, Theory.

Keywords
SSD, boost converter, charge pump, inductor design

1. INTRODUCTION
One of the serious design issues of Solid State Drive (SSD) is the increasing power consumption. Figure 1 shows a device architecture of a conventional SSD. A typical SSD consists of more than 16 NAND flash memories, DRAM's and a NAND controller. In SSD, each NAND flash chip has a charge pump circuit to generate the program voltage of 20V. Figure 2 shows a schematic and issues of the charge pump to generate the program voltage (V_{OUT}). 5 to 10 % area of each NAND flash chip is occupied by the charge pump due to its large capacitance, which raises the cost of SSD. Unacceptably large current (e.g. 800mA)

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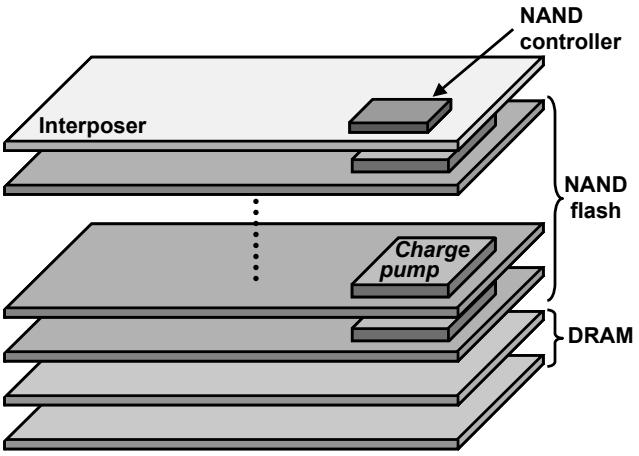

Figure 1. Conventional SSD with charge pump.

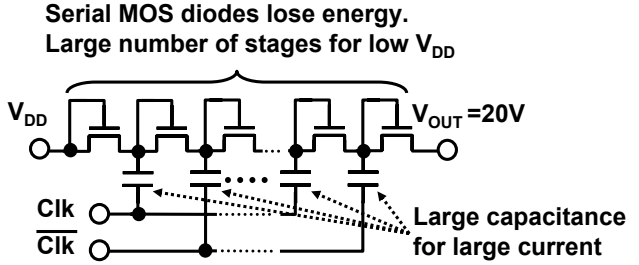

Figure 2. Schematic and issues of the charge pump.

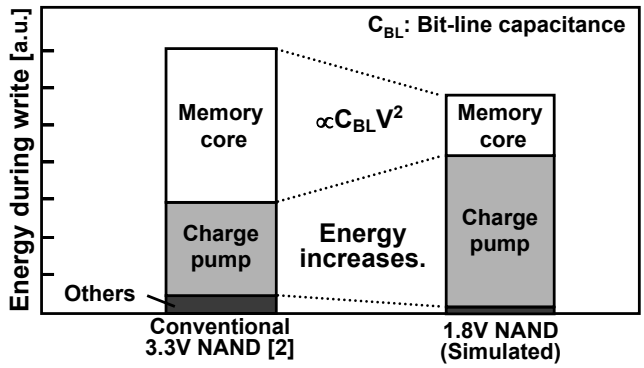

Figure 3. Energy consumption of NAND flash memories during write-operation at V_{DD} of 3.3V and 1.8V.

will flow to charge huge bit-line capacitance of NAND flash memories in a sub-30nm SSD [1], when 8 or more NAND chips operate in parallel, because the bit-line capacitance drastically increases with the device scaling. A good strategy to decrease the power is lowering the power supply voltage (V_{DD}) from 3.3V to 1.8V. Figure 3 compares the energy consumption of NAND flash memories during a write-operation at V_{DD} of 3.3V [2] and 1.8V (simulated). When V_{DD} is decreased from 3.3V to 1.8V, even though the energy of the memory core decreases, the total energy decreases by only 18%, because the energy of the charge pump increases. This is because the number of capacitance stages increases to generate 20V from reduced V_{DD} and the energy loss at the NMOS diodes increases as shown in Figure 2.

The poor output current drivability of the charge pump is also the problem, because 8 or more NAND flash chips in SSD need to be simultaneously programmed in order to achieve the 100-MByte/sec write speed of the hard disk drive, because the write speed of the NAND flash memory is only 10MByte/sec [2][3].

In this way, the charge pump prevents the area reduction, the V_{DD} scaling, and the fast write-operation of the NAND flash memory. Therefore, a new alternative high voltage generation circuit is strongly required to reduce the area, the power, and the write-time of the NAND flash memory.

Figure 4 shows a 3D-integrated SSD proposed in [4]. The NAND flash memories, DRAM's, the NAND controller, and a boost converter are integrated in SiP. Figure 5 shows a schematic diagram of the boost converter which consists of two high-voltage nMOS transistors and an inductor. In the proposed 3D SSD, both the low power and the fast write-operation are achieved, because both the voltage conversion efficiency and the output current drivability of the boost converter are higher than those of the charge pump. The die area of the NAND flash memory is also reduced, because the charge pumps on each flash memory are merged into the boost converter on an interposer. In the conventional NAND flash memory, the implementation of the inductor for the boost converter was difficult, because an on-chip inductor occupies the large die area and raises the cost. In contrast, in the proposed 3D SSD, the inductor is implemented on the blank space of the original interposer, which does not raise the cost for the inductor. The area penalty of high voltage MOS of the boost converter on the interposer is negligible, because the area is just 15% of the conventional charge pump. Thus, the proposed 3D-integrated SSD with the boost converter can achieve both the low power and the fast write-operation at the small die area of the NAND flash memory.

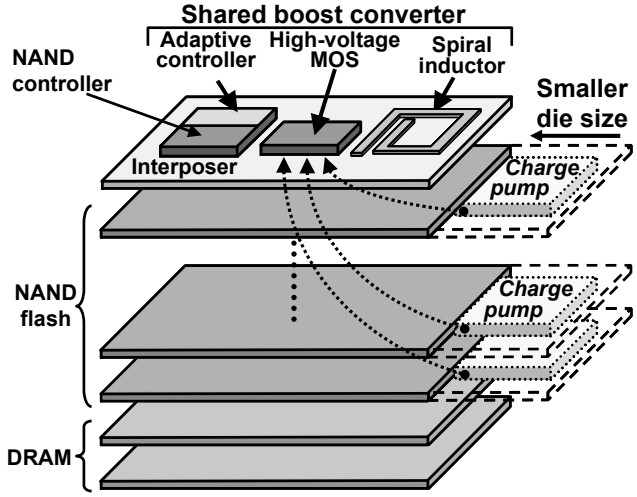

Figure 4. Proposed 3D-SSD with boost converter.

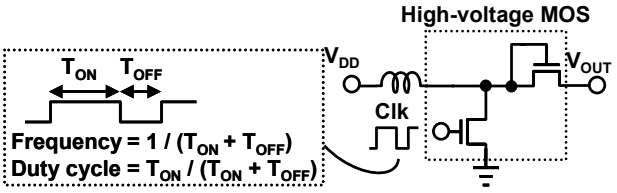

Figure 5. Circuit diagram of boost converter.

The performance of the boost converter, however, is critically affected by the inductor, because the output voltage of the boost converter, the rising time from an initial voltage to a target voltage (V_{OUT}), and the energy consumption during the boost are determined by the inductor. Therefore, the inductor design of the boost converter for the 3D SSD is very important. A spiral inductor design, however, is not clear and has not been published yet, because the output load of the boost converter of the NAND flash memory is different from that of a widely-used boost converter. Normally, the output load of the boost converter is resistive and the boost converter including that for a NOR flash memory [5] operates in a continuous conduction mode and the steady-state analysis is important and well understood. In contrast, the output load of the boost converter of the NAND flash memory is capacitive, and the boost converter operates in a discontinuous conduction mode. As shown in [4], the transient analysis during the boosting is important in this application. Although analytical equations of the discontinuous conduction mode have been developed in [6-7], their output load is resistive (less than tens of ohms). Therefore, the analytical equations cannot be used in this paper. Hence, this paper proposes a spiral inductor design of the boost converter for the 3D SSD with the NAND flash memories using SPICE circuit simulation.

2. Spiral inductor design for boost converter

In this chapter, the spiral inductor design of the boost converter for the 3D SSD is investigated. In order to implement the inductor in the 3D SSD, three types of inductors including an on-chip inductor (L), an on-interposer inductor, and an on-board inductor are compared. Figure 6 shows design parameters of the inductor. A square-shaped inductor is assumed. Table.1 shows the parameters of the three types of inductors used in this chapter. The inductance of the inductors is calculated by equations (1)-(4) [8].

$$L \approx \frac{\mu_0 n^2 d_{avg} c_1}{2}\left[\ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2\right] \quad (1)$$

$$d_{avg} = \frac{d_{out} + d_{in}}{2} \quad (2)$$

$$\rho \equiv \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \quad (3)$$

$$c_1 = 1.27,\ c_2 = 2.07,\ c_3 = 0.18,\ c_4 = 0.13 \quad (4)$$

L shows the inductance, μ_0 shows the vacuum permeability, n shows the number of turns, d_{out} shows the outer diameter, d_{in} shows the inner diameter, and c_1-c_4 are constants. d_{in} / d_{out} = 1/3 is assumed in this study to increase the quality factor of the inductor.

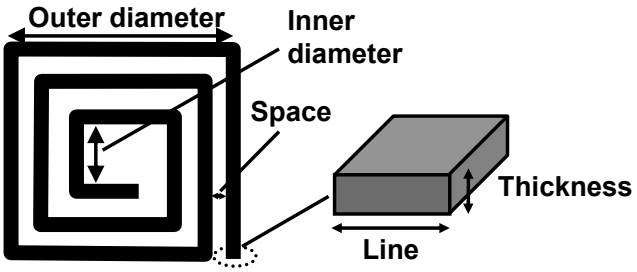

Figure 6. Design parameters of inductor.

Table 1. Parameters of three types of inductors.

	Line / Space	Thickness	Metal material
On-chip inductor	10μm / 10μm	2μm	Al
On-interposer inductor	25μm / 25μm	15μm	Cu
On-board inductor	100μm / 100μm	35μm	Cu

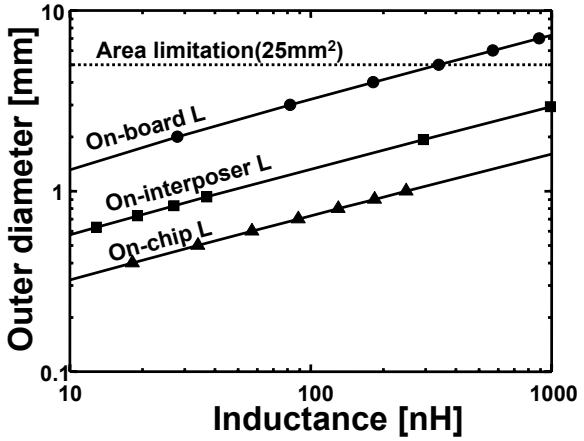

Figure 7. Calculated inductance dependence of outer diameter of three types of inductors.

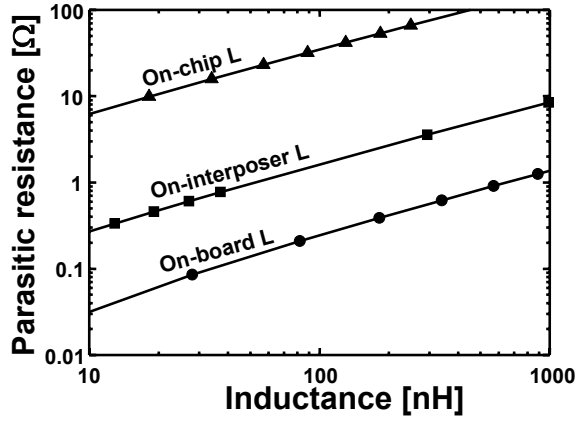

Figure 8. Calculated inductance dependence of parasitic resistance of three types of inductors.

As a first step of the inductor design, the range of the inductance is calculated with an area constraint.

Figure 7 shows the calculated inductance dependence of the outer diameter of the three types of inductors. Area limitation of 25mm^2 for the inductor is assumed, because the die area of a typical flash memory is 150mm^2 - 200mm^2 and the 15% of the area can be used for the inductor. Figure 8 shows the inductance dependence of the parasitic resistance of the three types of inductors calculated from total length of inductor. The on-chip inductor has the small area and the large parasitic resistance, because the line and space is narrow and the metal thickness is thin. In contrast, the on-board inductor has the large area and the small parasitic resistance, because the line and space is wide and the metal thickness is thick. In the on-board inductor, 330nH is the maximum inductance with the 25mm^2-area constraint.

The various inductors shown in Figures 7 and 8 are adopted in the boost converter and the best design of the inductor is investigated. Figure 9 shows the equivalent circuit of the simulated boost converter. Input voltage (V_{DD}) is 1.8V, and target output voltage (V_{OUT}) is 20V. A NAND flash chip as the output load of the boost converter is emulated by the load resistance (1MΩ) and capacitance (160pF). Parasitic resistance of the interconnects (R_1-R_5) and the inductor (R_L) are also included. Switching frequency (or period) and duty cycle are 18.2MHz (55ns) and 80% respectively, and the amplitude of the switching transistor is 3.6V. Inductance dependence of key performances of the boost converter including the output voltage, the rising time, and the energy consumption are simulated with this circuit.

Figure 10 shows the simulated dependence of the output voltage on the inductance in the three types of inductors. The boost converter with the on-chip inductor cannot boost the voltage above 4V, because the parasitic resistance of the on-chip inductor is very large. In contrast, both the on-interposer and the on-board

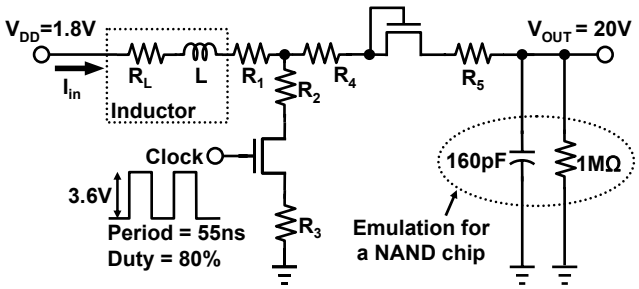

Figure 9. Equivalent circuit of simulated boost converter.

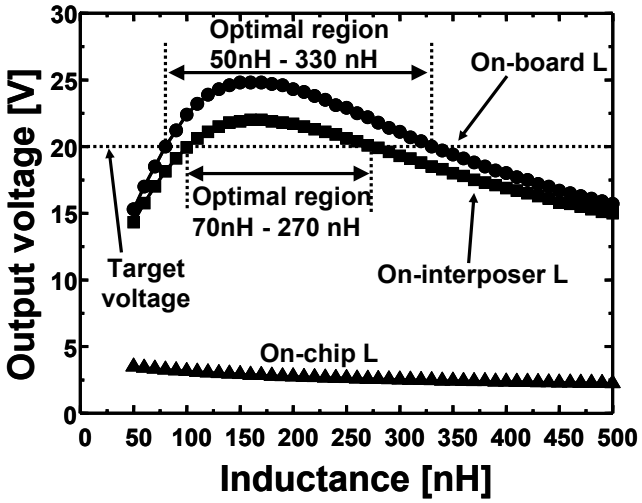

Figure 10. Simulated dependence of output voltage on inductance in three types of inductors.

inductors can boost the voltage above 20V. In order to boost the output voltage above 20V, a 50-nH to 330-nH on-board inductor and a 70-nH to 270-nH on-interposer inductor are needed. Too large or too small inductance cannot be used, because of the tradeoff between the inductance and the parasitic resistance. When the inductance is too small, the inductor cannot store enough energy to boost the voltage. When the inductance is too large, on the other hand, the inductor also cannot store enough energy because of the large parasitic resistance.

Figure 11 shows the simulated dependence of the rising time (t_{rise}) on the inductance in the two types of inductors. Figure 12 shows the simulated waveforms of the boost converter. t_{rise} is defined as the time to boost V_{out} from 0V to 15V as shown in Figure 12. The graph in Figure 11 is not smooth, because V_{out} of 15V is achieved by several pulses as shown in Figure 12. To realize short t_{rise}, the range of inductance is limited by 130nH to 260nH for the on-interposer inductor, and 110nH to 330nH for the on-board inductor. The reason for the optimum inductance region is similar to the previous discussion.

Figure 13 shows the simulated inductance dependence of energy consumption (E_{loss}) during boosting in the two types of inductors. E_{loss} is calculated from equation (5) using V_{DD}, the input current

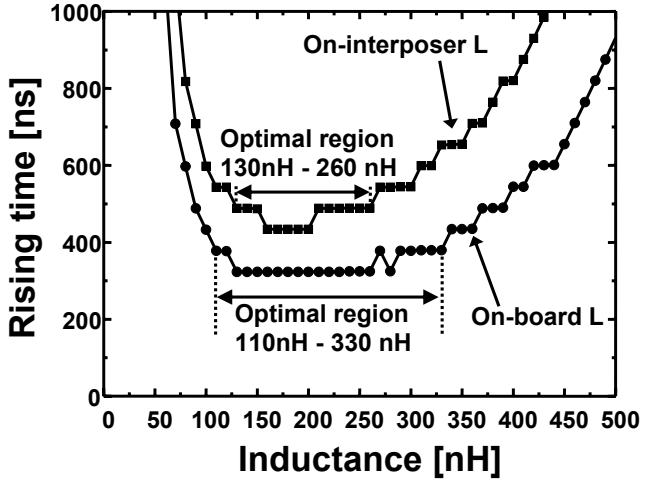

Figure 11. Simulated dependence of rising time on inductance in two types of inductors.

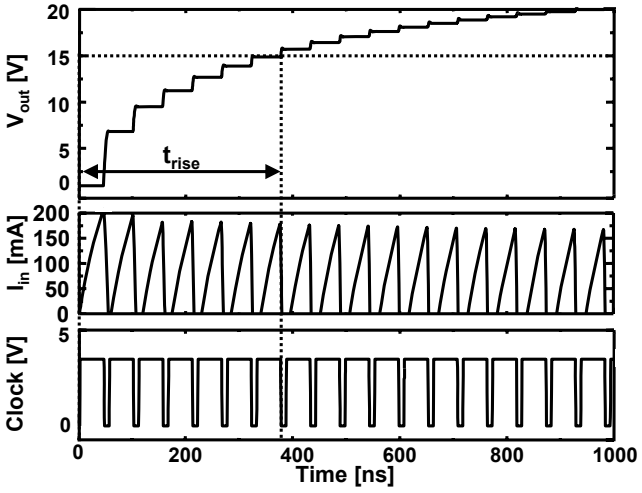

Figure 12. Simulated waveforms of boost converter.

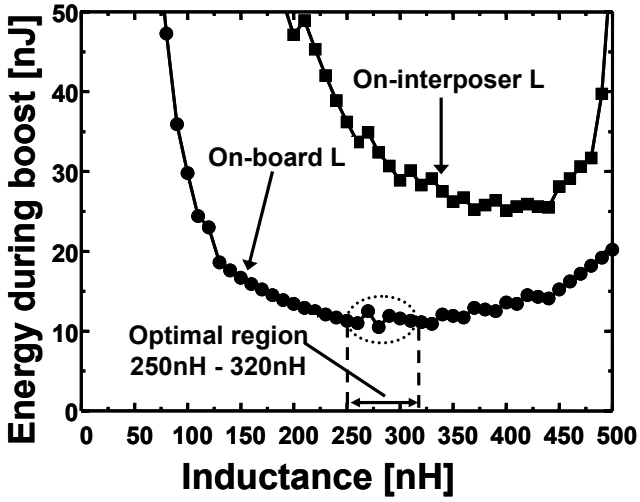

Figure 13. Simulated inductance dependence of energy consumption during boosting in two types of inductors.

(I_{in}), and t_{rise} shown in Figure 9.

$$E_{loss} = \int_0^{t_{rise}} V_{DD} \cdot I_{in} dt \quad (5)$$

When the on-interposer inductor is used, E_{loss} is minimum at around 400nH. This optimal range, however, does not match the range shown in Figures 10 and 11. In contrast, the inductance range from 250nH to 320nH is optimal with the on-board inductor. This is the best design point which meets all requirements including the high output voltage, the fast rising time, the low energy consumption, and the area limitation of 25mm^2, because this range is also within optimal region as shown in Figures 10 and 11. If the thicker metal is available in the on-interposer inductor, the boost converter with the on-interposer inductor will also achieve the similar performance as that with the on-board inductor.

3. Measurement results

To demonstrate the performance of the boost converter with the optimized inductor in the chapter 2, the boost converter with the 270-nH on-board inductor shown Table1 is fabricated and measured. Figure 14 shows the microphotographs of the on-board spiral inductor and the fabricated boost converter LSI where the high voltage MOSFET's are integrated. The area of the inductor is 5mm by 5mm, and the area of the boost converter LSI is

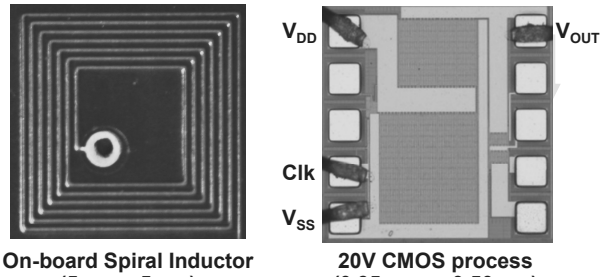

Figure 14. Microphotographs of on-board spiral inductor and fabricated boost converter LSI where high voltage MOSFET's are integrated.

Table 2. Summary of key features of proposed boost converter and conventional charge pump.

	Proposed boost converter (Measured)	Conventional charge pump (Simulated)
Supply voltage	1.8V	←
Chip area	0.175mm² (15%)	1.19mm² (100%)
Rising time (0➔15V)	0.92μs (27%)	3.45μs (100%)
Energy during boost (0➔15V)	30nJ (12%)	253nJ (100%)

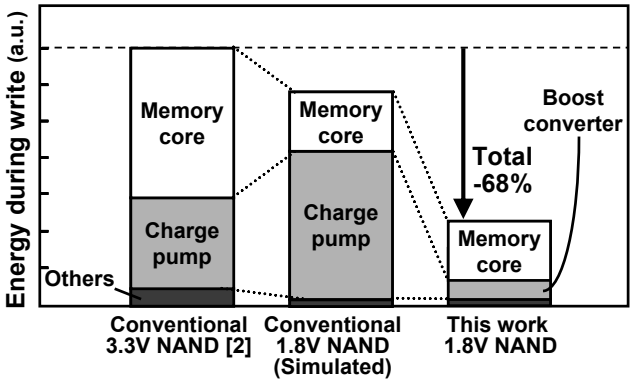

Figure 15. Comparison of the energy during write between conventional 3D-SSD with charge pump and proposed 3D-SSD with the boost converter.

0.35mm by 0.50mm. The measured parasitic resistance of the inductor is 1.05Ω. Table 2 summarizes measured key features of the boost converter and the conventional charge pump for typical NAND flash memory. Measured energy consumption to 15V is 30nJ which is 12% of the charge pump, and the rising time is 0.92ns which is 27% of the charge pump. The area of the high voltage MOSFET's is 0.175mm^2 which is 15% of the charge pump. Figure 15 shows the comparison of the energy during write between the conventional 3D-SSD with the charge pump and the proposed 3D-SSD with the boost converter. By decreasing V_{DD} of the NAND from 3.3V to 1.8V, the total energy during write of a NAND flash memory decreases by 68% compared with the conventional 3.3V NAND because the energy of the high voltage generator decreases by 88% compared to the charge pump. In the charge pump, the number of stage will increase when the V_{DD} is lowered to 1.8V, and therefore energy loss by MOS diodes increases. In contrast, since the boost converter achieves 20-V program voltage with single-stage circuit, the energy loss does not increase. In this way, the proposed spiral inductor design of the boost converter contributes to the low power and the fast write-operation of the 3D SSD.

4. Conclusion

The design methodology of the inductor of the boost converter for the 3D SSD is proposed. The on-board inductor from 250nH to 320nH is the best design point which meets all requirements including the high output voltage above 20V, the fast rising time, the low energy consumption, and the area below 25mm^2. By using the boost converter with the proposed inductor, the energy during write-operation of the proposed 1.8-V 3D-SSD is decreased by 68% compared with the conventional 3.3-V 3D-SSD with the charge pump.

5. Acknowledgment

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