A 25-mV-Sensitivity 2-Gb/s Optimum-Logic-Threshold Capacitive-Coupling Receiver for Wireless Wafer Probing Systems

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***Abstract*—A high-sensitivity capacitive-coupling receiver is presented for wireless wafer probing systems. The receiver with the optimum logic threshold (OLT) achieves the highest sensitivity of 25 mV at the data rate of 2 Gb/s in 0.18-μm CMOS. The OLT receiver increases the communication distance by more than four times while providing tolerance against distance–voltage–area variations.**

***Index Terms*—Capacitive coupling, high speed, inductive coupling, optimum logic threshold (OLT), sensitivity, tolerance, wireless wafer probing system.**

I. Introduction

THE WIRELESS wafer probing system, as an alternative to a mechanical one, provides attractive solutions. Reliability can significantly be improved, since both the physical damage and force on I/O pads are eliminated, whereas the mechanical probing system requires the careful control of probing needles to minimize the deformation of I/O pads. In addition, the wireless wafer probing can efficiently increase the number of probes, which allows for highly parallel probing for multidie and reduces the cost of testing [1], [2].

For a wireless wafer probing system, a wireless interface that is merged into the device under test (DUT) must be small so as not to degrade the established integration level of the DUT [1]. It also requires a high I/O bandwidth and should be tolerant to the variations in communication distance and transmitting voltage (or current), as well as the misalignment between two interfaces, where the maximum communication distance is a measure of the tolerance for a given receiver sensitivity. Moreover, the interferences coming from adjacent channels must be kept low to maintain the signal integrity, which is essential for multichannel applications [2].

Inductive and capacitive couplings [1]–[15] can be employed to realize a wireless wafer probing system. Table I summarizes the characteristics of inductive and capacitive couplings. Since inductive coupling [2]–[6] is current driven, the transmission gain can easily be increased, which allows for long-distance communications that can guarantee a good tolerance [3]. In contrast, capacitive coupling [1], [7]–[15] is voltage driven, and its maximum transmission gain can be limited by the voltage swing of a transmitter driver and the coupling capacitance between two electrodes; thus, its applications are restricted to short-distance communications [12].

TABLE I
Characteristic Comparison of Capacitive and Inductive Couplings

Coupling	Capacitive	Inductive
Communication distance	<10 μm [12]	<15 μm [3]
Crosstalk ($V_{xtalk,C,L}$)[a]	$RC\,dV/dt$	$\sum M\,dI/dt$
Area[b]	1x PAD I/O PAD I/O	PAD I/O >1x PAD I/O
Bandwidth	$1/(C_C+C_R)R_R$	$1/C_R R_R$

[a] R and C are a resistance and a coupling capacitance between adjacent channels, respectively. M is a mutual inductance.

[b] Two illustrations show top view of two channels within DUT, respectively.

The superior transmission capability of inductive coupling, however, leads to a large area and high power consumption because the capability is obtained by increasing the current or the number of turns of an inductor. In addition, inductive coupling requires a large pitch to minimize the crosstalk (V_{xtalk}) that is hardly shielded because it propagates in all directions in a transmitter and is superimposed in a receiver. In addition, the inductive interconnection basically requires separate interfaces (i.e., inductors), which also give rise to area overhead [2].

In contrast, the capacitive crosstalk not only is less than the inductive one but also can easily be blocked by shielding elements [16]. Consequently, one can realize a wireless interface with fine pitch. Moreover, since capacitive coupling can use the existing I/O pads instead of additional interfaces, the interface can be implemented with the high area efficiency.

The bandwidth of inductive coupling is limited by the input capacitance of a receiver, i.e., C_R, and the input resistance, i.e.,

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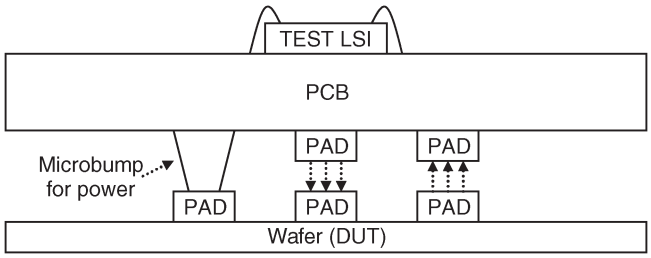

Fig. 1. Wireless wafer probing system based on a capacitive-coupling interface.

R_R, whereas that of capacitive coupling is determined by the coupling capacitance, i.e., C_C, between two electrodes, C_R, and R_R. Since C_R is more than 20 times larger than C_C, owing to the large input capacitances of electrostatic discharge (ESD) circuits, particularly for wireless wafer probing systems, both interfaces represent similar bandwidth limitations.

In this brief, a high-sensitivity high-speed capacitive-coupling receiver is proposed to provide tolerance against distance–voltage–area variations and the high I/O bandwidth for wireless wafer probing systems.

This brief is organized as follows. Section II describes the channel characteristic of a wireless wafer probing system. The proposed capacitive-coupling receiver is discussed in Section III. Section IV presents the test environment and the experimental results. Section V gives the conclusions.

II. Wireless Wafer Probing System

Fig. 1 illustrates the wireless wafer probing system based on a capacitive-coupling interface. The upper pads are implemented on the bottom side of a printed circuit board (PCB) that can reduce cost and can easily be customized, whereas the lower pads are realized on the tested wafer. Power is supplied through a physical connection such as microbumps [10].

Fig. 2(a) illustrates a simplified channel model for the wireless wafer probing system. In contrast to chip-to-chip interfaces (e.g., 3-D integrated circuits [3]–[8], [10]–[15]), our system has large input capacitances $C_{\mathrm{RX}}(\simeq C_{\mathrm{ESD}} + C_{\mathrm{PAD}} + C_{\mathrm{WIRE}})$ caused by ESD protection circuits, which results in both significant signal attenuation and bandwidth limitation in a receiver, where C_{ESD} is the capacitance of ESD, C_{PAD} is the capacitance of the pad, and C_{WIRE} is the capacitance of the bonding wire. The simulation results indicate that the signal attenuation is greater than 35 dB for the DUT to TEST LSI. This value corresponds to the received voltage (V_{RX}) of about 30 mV with a transmitted voltage of 1.8 V. The estimated minimum V_{RX} against the different input capacitances of a receiver is shown in Fig. 2(b). A coupling capacitor with a distance of 4 μm and an area of 80 μm $\times$ 80 μm is used for the estimation. Consequently, the signal attenuation due to the large input capacitance of a receiver limits the minimum area of the pads, the misalignment between two pads, the maximum allowable distance, and the minimum voltage swing of the transmitter driver. The high sensitivity of the receiver can mitigate all these limitations and, in turn, increases the tolerance against distance–voltage–area variations.

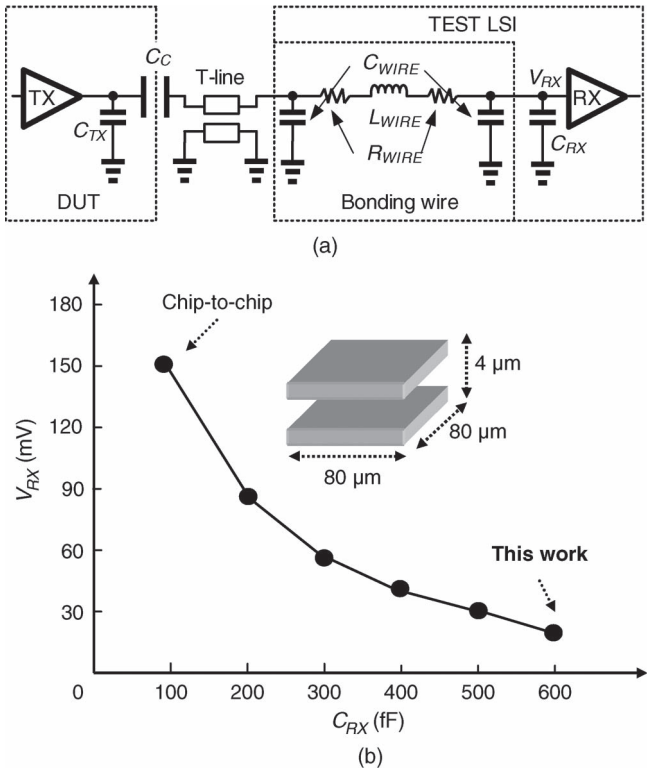

Fig. 2. (a) Simplified channel model. (b) Estimated minimum received voltages against different input capacitances of a receiver for the wireless wafer probing system.

In this brief, a capacitive-coupling receiver with the highest sensitivity of 25 mV at the data rate of 2 Gb/s in a 0.18-μm CMOS process is presented.

III. High-Sensitivity OLT Receiver

A. Interface Characteristic

In contrast to previous works [1]–[6], [9], [10], [12], [13], the proposed receiver has a large RC time constant (τ) for high-sensitivity high-speed operation, where τ has its usual meaning. The receiver with small τ restores asymmetric and triangular pulses with filtered low-frequency components [9]. The signals with attenuated pulse swing, which is caused by the channel characteristic, represent a narrow pulsewidth, which reduces the timing margin for data recovery and limits the maximum data rate [10]. Thus, the small-τ receiver with a limited timing margin requires complex timing control circuits to recover transmitted signals for a given data rate [2], [3], [9], [10]. In contrast, a large-τ receiver maintains the original forms of transmitted signals; thus, one can achieve the maximum timing margin, even when the pulse swing becomes smaller, owing to the channel characteristic [17]. As a result, the large-τ receiver exhibits higher sensitivity and a higher data rate than the small-τ receiver.

The large-τ receiver, however, suffers from the dc offset (i.e., various logic thresholds) as a result of distance–area–supply-voltage variations and the zero wander effect, wherein the received signals go down below '0' V [17]. The direct application of a fixed reference results in both low sensitivity

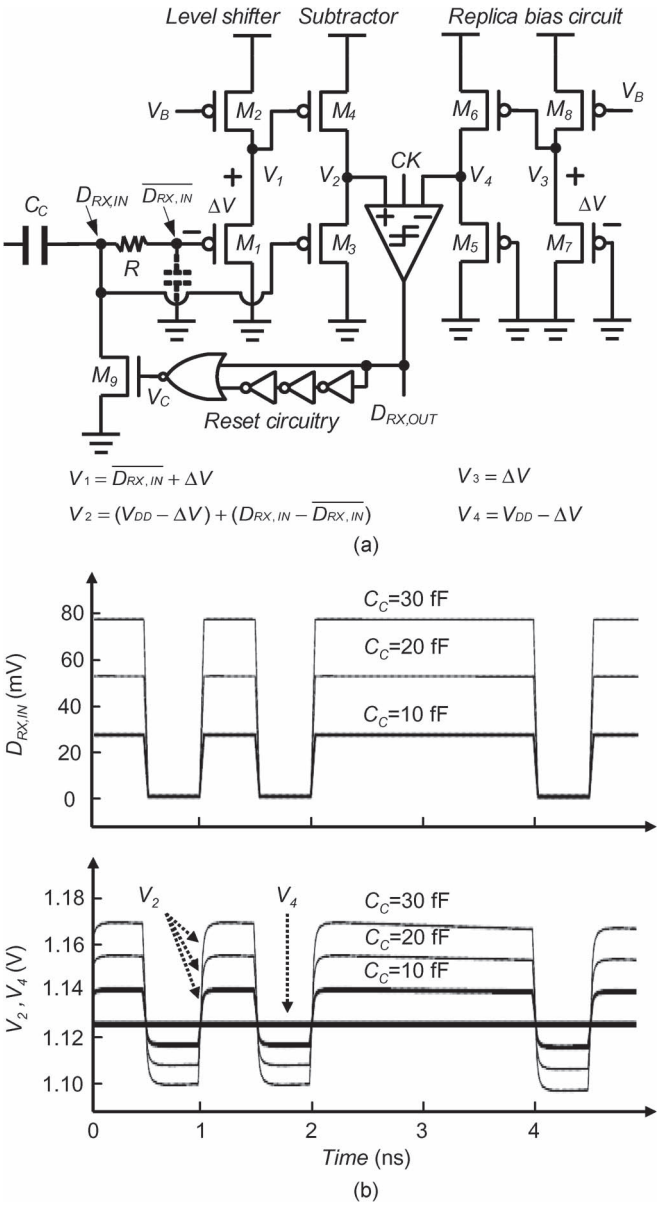

Fig. 3. (a) Schematic of the proposed OLT receiver. (b) Simulated waveforms at 2 Gb/s.

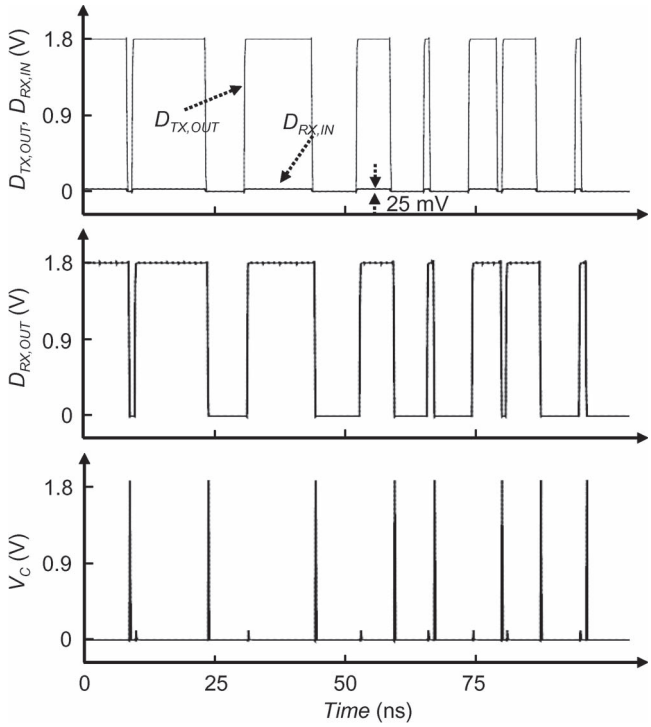

Fig. 4. Simulated waveforms of TX and RX at 2 Gb/s.

and pulsewidth distortion, which, in turn, increase the bit error rate (BER). To remove the dc offset, one can insert a coupling capacitor in front of the receiver. However, the required capacitance is normally large [17]. A feedback topology can remove the dc offset and the zero wander effect, but it limits the maximum data rate and is not suitable for high-speed applications [17], [18]. The proposed receiver employs a feedforward topology without the coupling capacitor and converts the received signals into other signals with the optimum logic threshold (OLT) to eliminate the dc offset and the zero wander effect.

B. OLT Receiver

Fig. 3(a) shows the schematic of the proposed OLT receiver. The receiver is composed of a level shifter, a subtractor, a replica bias circuit, a comparator, and a reset circuitry. The subtractor and the replica bias circuit provide output signals V_2 and V_4 to the following comparator (sense amplifier-type flip-flop), respectively. The RC network consisting of resistor R and input capacitor of M1 produces an averaged signal $\overline{D_{\mathrm{RX,IN}}}$ with the same logic threshold voltage V_{TH} as those of the received signal $D_{\mathrm{RX,IN}}$ under a balanced data pattern (e.g., 8B/10B encoding). After an appropriate level shift by ΔV, the circuit consisting of M3 and M4 subtracts the shifted signal (V_1) from $D_{\mathrm{RX,IN}}$ and generates the output signal V_2 with a constant V_{TH}, as shown in Fig. 3(b). Since the subtractor removes $\overline{D_{\mathrm{RX,IN}}}$ from $D_{\mathrm{RX,IN}}$ and produces signals with the OLT, the OLT receiver can recover both small and large $D_{\mathrm{RX,IN}}$ with different V_{TH} with high sensitivity.

A replica bias circuit, consisting of M5–M8, provides a fixed reference voltage (V_4), which is equal to the V_{TH} of V_2, which can easily be achieved by applying the same potentials to the gates of M5 and M7.

A reset circuitry provides reset signal V_C to M9 to maintain the bottom level of $D_{\mathrm{RX,IN}}$. The zero wander effect can easily be eliminated by the reset signal because the continuous fall of the bottom level of $D_{\mathrm{RX,IN}}$ is prevented by the reset to '0' V after the transitions of output signals $D_{\mathrm{RX,OUT}}$.

Fig. 4 shows simulated waveforms of the transmitter and the receiver. The transmitted signal $D_{\mathrm{TX,OUT}}$ with 1.8 V is attenuated to $D_{\mathrm{RX,IN}}$ with about 25 mV, particularly when the input capacitance of the receiver of 600 fF and the coupling capacitance of 10 fF, which corresponds to the distance of about 4 μm in air and a pad size of 80 μm $\times$ 80 μm, are applied to the capacitive-coupling interface. The 25-mV signals are successfully recovered by the proposed OLT receiver.

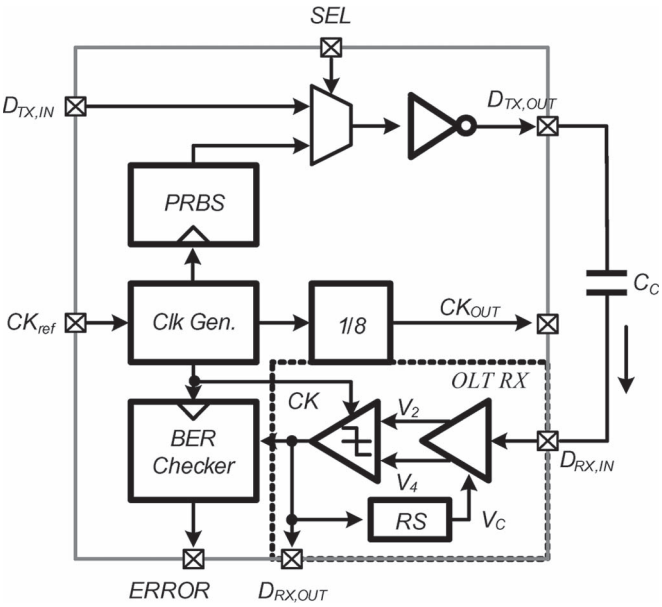

Fig. 5. Block diagram of the test chip.

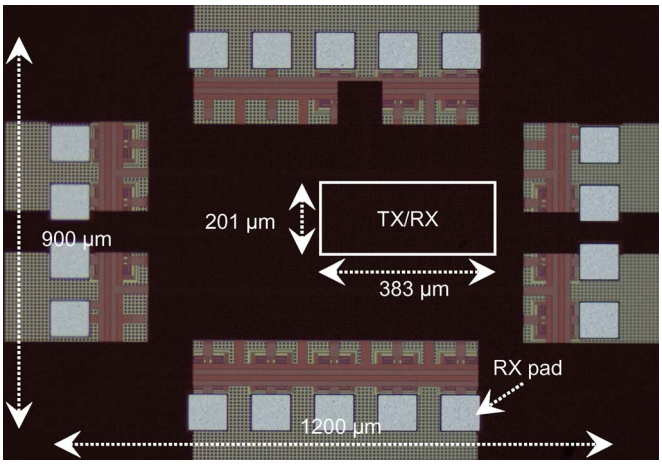

Fig. 6. Micrograph of the test chip.

C. Test Chip

Fig. 5 shows the block diagram of the transmitter and the proposed OLT receiver for chip test. The transmitter is a buffer that drives the transmitter pad, and the OLT receiver converts $D_{\mathrm{RX,IN}}$ to $D_{\mathrm{RX,OUT}}$. A pseudorandom bit sequence (PRBS) generator and a BER checker with pattern lengths of $2^{33}-1$ are used for the built-in self-test. A clock generator provides clock signals of 2 GHz for the transmitter and the receiver. Skews between the data and the clock are compensated by simple delay elements because the proposed interface has a sufficient timing margin.

IV. Experimental Results

The micrograph of the test chip fabricated by the 1.8-V 0.18-μm CMOS process is shown in Fig. 6.

Fig. 7(a) shows the test environment for the proposed OLT receiver. For chip-to-board communication, a TX pad of

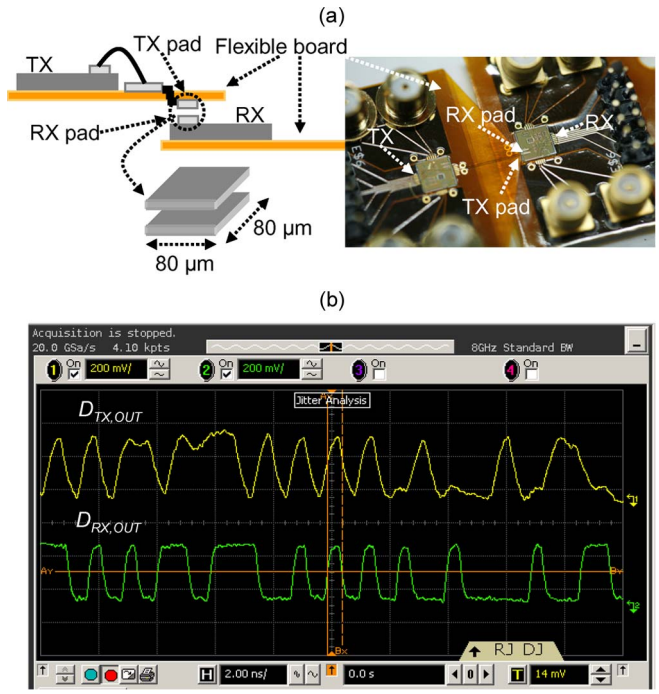

Fig. 7. (a) Test environment. (b) Measured waveforms at the maximum data rate of 2 Gb/s.

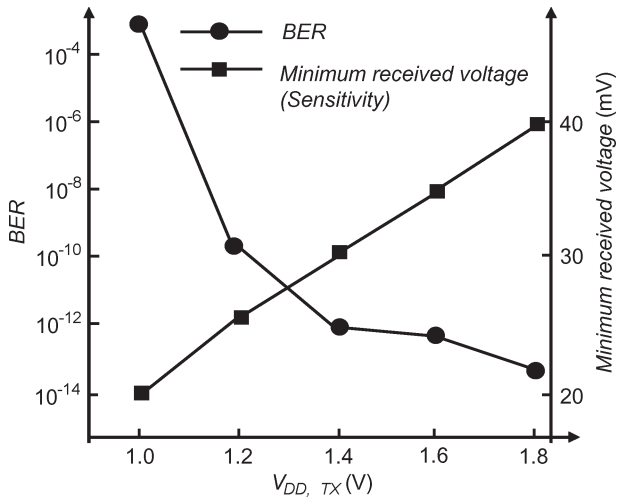

Fig. 8. Measured BER and simulated minimum received voltage.

80 μm $\times$ 80 μm is patterned on the thin transparent flexible board, and one of the peripheral I/O pads is used as the RX pad of the same size. The measured waveforms at the maximum data rate of 2 Gb/s, which was determined from the comparator performance, are shown in Fig. 7(b).

The BER was measured as a function of the supply voltage of TX and the simulated received voltage of RX (Fig. 8) using the internal PRBS and BER checker with pattern lengths of $2^{33}-1$. For a received voltage of 25 mV and a communication distance of 4 μm, the BER is $< 10^{-10}$ with the maximum data rate of 2 Gb/s. The measured performance is summarized in Table II.

Fig. 9(a) represents a performance comparison with the reported sensitivity of previous capacitive-coupling interfaces

TABLE II
PERFORMANCE SUMMARY

Technology		0.18 μm CMOS
Supply voltage		1.8 V
Max. data rate		2 Gb/s
Sensitivity		25 mV
Input cap. (RX)		>600 fF
BER		$<10^{-10}$
Core power @2 Gb/s	TX	4.87 μW
	RX	1.63 mW
Core area	TX	60 μm^2
	RX	2900 μm^2

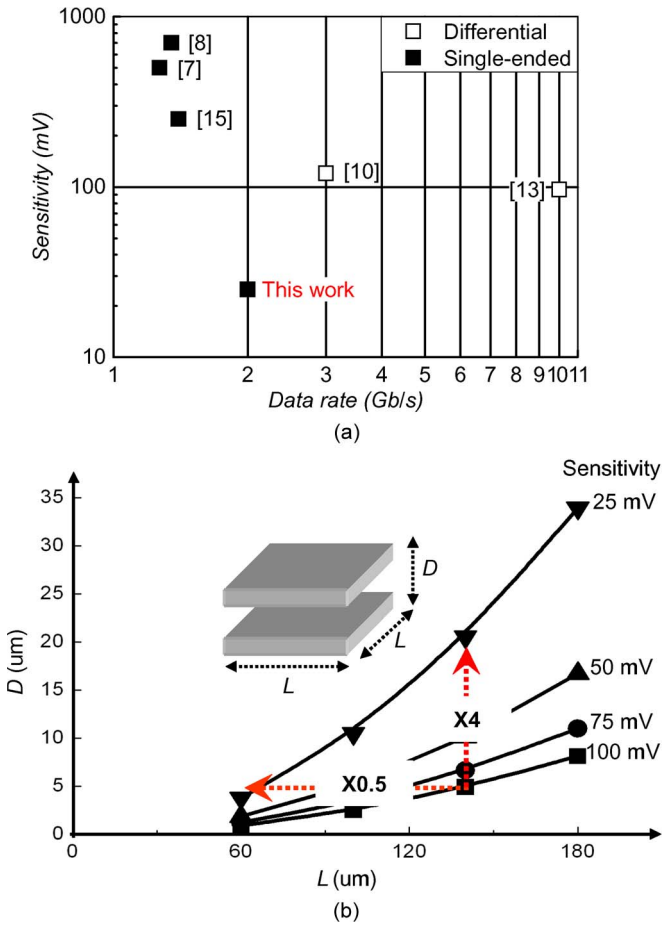

Fig. 9. Performance comparisons. (a) Sensitivity versus data rate. (b) Sensitivity versus distance versus pad area.

[7], [8], [10], [13], [15]. The performance of the proposed interface is at least four times superior to those of previous works. The OLT receiver with a sensitivity of 25 mV can increase the communication distance and reduce the pad size by more than four times, respectively, as shown in Fig. 9(b). Note that the increased maximum communication distance improves the tolerance against distance–supply-voltage–area variations.

V. CONCLUSION

A capacitive-coupling receiver fabricated by the 1.8-V 0.18-μm CMOS process has been proposed for wireless wafer probing systems. The proposed OLT receiver with high sensitivity not only extends the communication distance between two electrodes but also increases the tolerance to distance–voltage–area variations.

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