Effect of Resistance of TSV's on Performance of Boost Converter for Low Power 3D SSD with NAND Flash Memories

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***Abstract*- This paper investigates the effect of the TSV resistance (R_{TSV}) on the performance of boost converters for Solid State Drive (SSD) using circuit simulation. When R_{TSV} is 0Ω, both the rising time (t_{rise}) from 0V to 15V and the energy during boosting (E_{loss}) of the output voltage (V_{OUT}) are 10.6% and 6.6% of the conventional charge pump respectively. In contrast, when R_{TSV} is 200Ω, for example, t_{rise} is 30.1% and E_{loss} is 22.8% of the conventional charge pump. Besides, V_{OUT} cannot be boosted above 20V when R_{TSV} is larger than 210Ω. Therefore, in order to maintain the advantages of the boost converter over the charge pump in terms of t_{rise} and E_{loss}, the reduction of R_{TSV} is very important.**

1. Introduction

One of the serious design issues of SSD is the increasing power consumption. Fig. 1 shows a device architecture of a conventional SSD. A typical SSD consists of more than 16 NAND flash memories, DRAM's and a NAND controller. In SSD, each NAND flash chip has a charge pump circuit to generate the program voltage of 20V. Fig. 2 shows a schematic and issues of the charge pump to generate the program voltage (V_{OUT}). The charge pump prevents the area reduction, the V_{DD} scaling, and the fast write-operation of the NAND flash memory [1]. For example, 5 to 10% area of each NAND flash chip is occupied by the charge pump due to its large capacitance, which raises the cost of SSD. Therefore, new alternative high voltage generation circuit is strongly required to reduce the area, the power, and the write-time of the NAND flash memory.

Fig. 3 shows a 3D-integrated SSD proposed in [1]. The NAND flash memories, DRAM's, the NAND controller, and a boost converter are integrated in SiP. Through silicon vias (TSV's) are assumed as the connection of the boost converter and each NAND chip. Fig. 4 shows a schematic diagram of the boost converter which consists of two high-voltage nMOS transistors and an inductor. In the proposed 3D SSD, both the low power and the fast write-operation are achieved, because both the voltage conversion efficiency and the output current drivability of the boost converter are higher than those of the charge pump. The die area of the NAND flash memory is also reduced, because the charge pumps on each flash memory are merged into the boost converter on an interposer.

In [1], the advantage of the boost converter over the charge pump was shown by measurements. The feasibility of the 3D SSD with TSV connections, however, is not clear, because the measurement does not take into account the parasitic RLC's accompanying TSV's. In reality, when 3D-SSD's are implemented using TSV's, the parasitic RLC's may degrade the performance of the boost converter. The parasitic L and C of the TSV's, however, can be neglected, because the parasitic L and C are under 0.03% and 1% of the inductance of the inductor and the output load capacitance, respectively, of the boost converter [2]. In contrast, the parasitic resistance of TSV's (R_{TSV}) cannot be disregarded.

Therefore, in this paper, the impact of R_{TSV} on the performance of the boost converter (output voltage (V_{OUT}), rising time (t_{rise}), and energy during boosting (E_{loss})) is simulated using SPICE. The performance is also compared with that of the conventional charge pump.

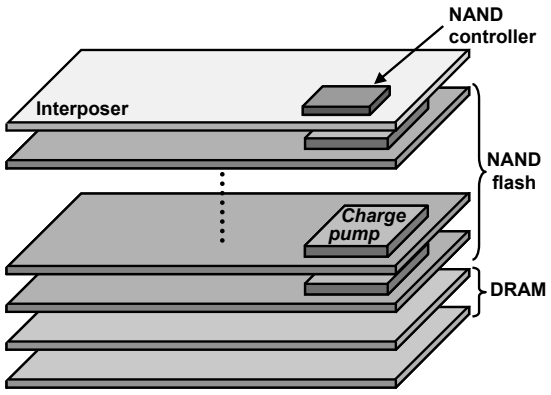

Fig. 1. Conventional 3D-SSD with charge pump.

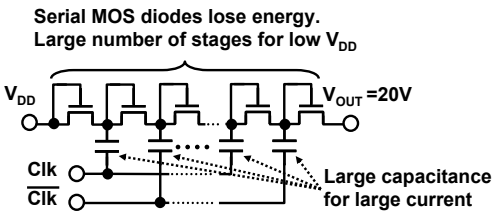

Fig. 2. Schematic and issues of the charge pump.

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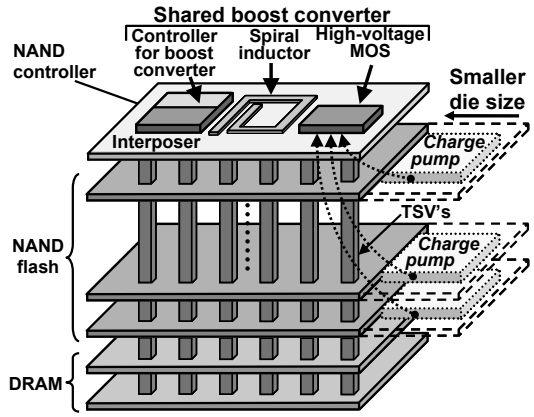

Fig. 3. Proposed 3D-SSD with boost converter.

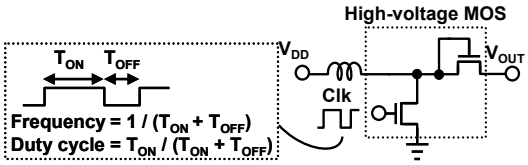

Fig. 4. Circuit diagram of boost converter.

2. Effect of TSV's on performance of boost converter

R_{TSV} is determined by TSV materials, the thickness of NAND chips and the number of stacked NAND chips. For example, the resistance of Cu TSV's with a diameter of 2~5μm and a height of 5μm is 80~200mΩ/via [3], while the resistance of doped poly-Si TSV with a diameter of 28~46μm and a height of 50μm is 1.3~5.0Ω/via [4]. Considering the thickness of a NAND chip which is assumed as 35μm, the resistance of Cu TSV's per NAND chip is 0.56~1.4Ω, and the resistance of poly-Si TSV is 0.91~3.5Ω. In a 64 chip stacked SSD where a boost converter is connected to all the chips using only one TSV, the maximum total R_{TSV} becomes 224Ω (poly-silicon TSV) and 89.6Ω (copper TSV). Therefore, R_{TSV} up to 250Ω is considered in this section.

Fig. 5 shows the equivalent circuit of the simulated boost converter. Input voltage (V_{DD}) is 1.8V, and the target output voltage (V_{OUT}) is 20V. A NAND flash chip as the output load of the boost converter is emulated by the load resistance (R_L=1MΩ) and capacitance (C_L=160pF). The resistance and capacitance of the word line of the NAND flash chip is also considered using distributed RC lines in order to compare RC delay due to word lines and RC delay due to R_{TSV}. The total resistance of word lines ($R_{WLtotal}$) is 500kΩ, thereby R_{WL} is 166.7kΩ. The total capacitance of word lines ($C_{WLtotal}$) is 2pF, thereby C_{WL1} is 0.333pF and C_{WL2} is 0.666pF. The voltage of the node after distributed RC line of word lines is defined as V_{WL}. V_{WL} also need to be boosted up to 20V. Parasitic resistance of the interconnects (R_1-R_5) and the inductor (R_{Ind}) are also included. Switching frequency (or period) and duty cycle are 18.2MHz (55ns) and 80% respectively, and the amplitude of the clock is 3.6V. R_{TSV} is serially connected directly after R_5. The current which flows into R_{TSV} is defined as I_{RTSV}. A 270nH-inductor is used based on the result of [5]. R_{Ind} is 0.51Ω.

Fig. 6 shows the simulated R_{TSV} dependence of V_{OUT} and V_{WL} of the boost converter. V_{OUT} and V_{WL} are exactly same line. The dashed line denotes the target voltage of 20V. Both V_{OUT} and V_{WL} decrease, as R_{TSV} increases. In order to achieve V_{OUT} and V_{WL} above 20V, R_{TSV} less than 210Ω is required. However, it can be said that the impact of R_{TSV} on V_{OUT} and V_{WL} is small compared with Figs. 8 and 10.

Fig. 7 shows the simulated waveforms of V_{OUT}, V_{WL}, I_{in}, and clock of the boost converter. Fig. 8 shows the simulated R_{TSV} dependence of t_{rise} of the boost converter. t_{rise} is defined as the time to boost V_{OUT} and V_{WL} from 0V to 15V as shown in Fig. 7. The right axis of Fig. 8 is t_{rise} of V_{OUT} compared to the conventional charge pump [1]. Simulation of the charge pump is conducted under same output load condition of C_L and R_L and t_{rise} of the charge pump is 3.45μs [1]. The graph of V_{OUT} in Fig. 8 is not smooth, because V_{OUT} of 15V are achieved by several pulses as shown in Fig. 7. If t_{rise} of V_{WL} is determined by $R_{WLtotal}$ x $C_{WLtotal}$ time constant, t_{rise} of V_{WL} does not depend on R_{TSV}, because $R_{WLtotal}$ x $C_{WLtotal}$ is 1μs while maximum R_{TSV} x C_L is 40ns. In reality, however, t_{rise} of V_{WL} is largely affected by R_{TSV}. This means that t_{rise} is not determined by the RC time constant. In order to investigate

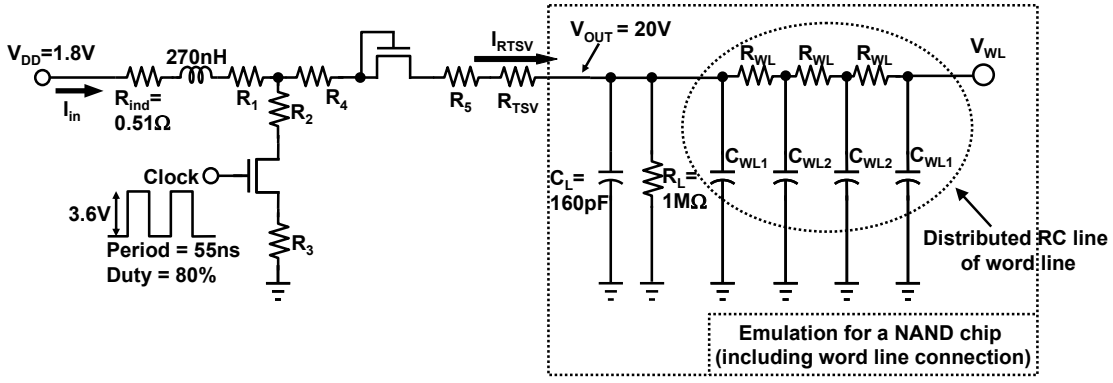

Fig. 5. Equivalent circuit of simulated boost converter.

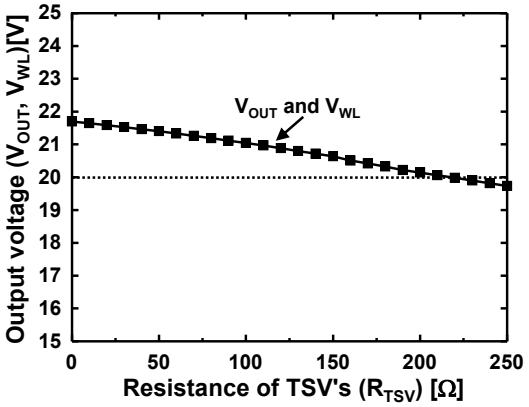

Fig. 6. Simulated dependence of output voltage of boost converter on resistance of TSV's.

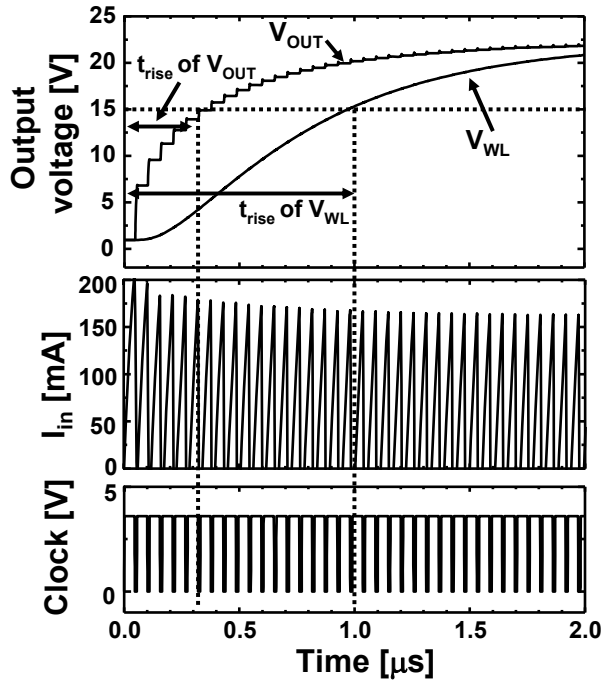

Fig. 7. Simulated waveforms of boost converter

the reason, Fig. 9 shows simulated dependence of peak current of I_{RTSV} during the first switching on R_{TSV}. This shows that the peak current of I_{RTSV} decreases when R_{TSV} increases. As a result, t_{rise} increases in Fig. 8. In this way, t_{rise} is not determined by $R_{WLtotal}$ x $C_{WLtotal}$ time constant but by I_{RTSV}.

Fig. 10 shows the simulated R_{TSV} dependence of E_{loss} of V_{OUT}. E_{loss} is calculated from equation (1) using V_{DD}, the input current (I_{in}), and t_{rise}. The right axis of Fig. 10 is E_{loss} compared to the conventional charge pump [1]. E_{loss} of the charge pump is 253nJ [1].

$$E_{loss} = \int_0^{t_{rise}} V_{DD} \cdot I_{in} dt \qquad (1)$$

E_{loss} is proportional to t_{rise}, because I_{in} is almost not affected by R_{TSV}.

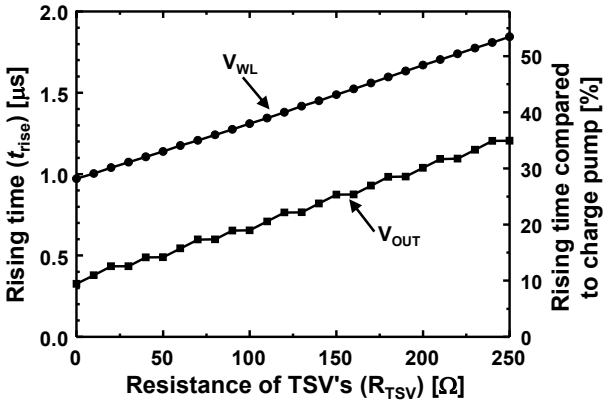

Fig. 8. Simulated dependence of rising time on resistance of TSV's.

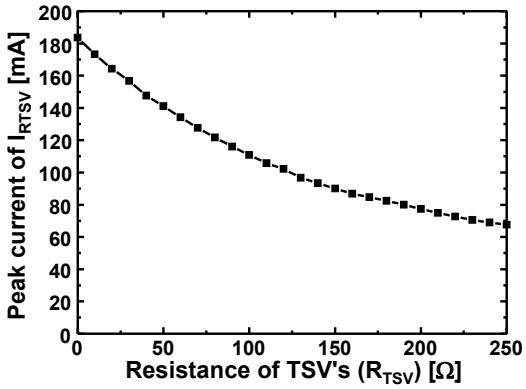

Fig. 9. Simulated dependence of peak current of I_{RTSV} on resistance of TSV's.

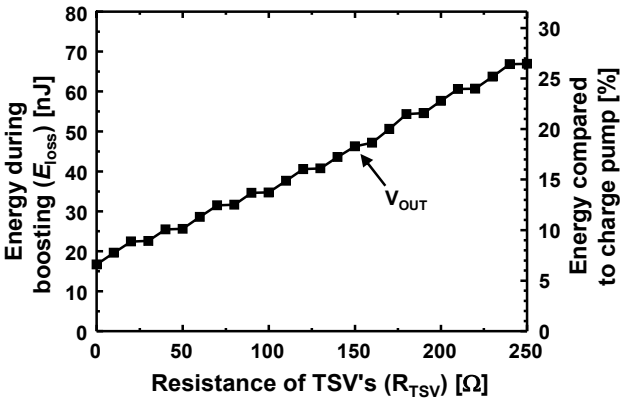

Fig. 10. Simulated dependence of energy consumption during boosting on resistance of TSV's

When R_{TSV} is 200Ω, for example, t_{rise} of V_{OUT} is 30.1% and E_{loss} of V_{OUT} is 22.8% of the conventional charge pump. Besides, V_{OUT} cannot be boosted above 20V when R_{TSV} is larger than 210Ω as shown in Fig. 6. Therefore, in order to maintain the large advantages of the boost converter over the charge pump in terms of t_{rise} and E_{loss}, reduction of R_{TSV} is very important.

Cu TSV's would be are more suitable than poly-silicon TSV's for the proposed application, because NAND flash chips are made with expensive processes and Cu TSV's have

an advantage over poly-silicon TSV's in area due to the lower resistivity.

3. Conclusions

The effect of R_{TSV} on the boost converter was investigated. When R_{TSV} is 0Ω, t_{rise} and E_{loss} of V_{OUT} are 10.6% and 6.6% of the conventional charge pump respectively. In contrast, when R_{TSV} is 200Ω, for example, t_{rise} of V_{OUT} is 30.1% and E_{loss} of V_{OUT} is 22.8% of the conventional charge pump. Besides, V_{OUT} cannot be boosted above 20V when R_{TSV} is larger than 210Ω. Therefore, in order to maintain the large advantages of the boost converter over the charge pump in terms of t_{rise} and E_{loss}, reduction of R_{TSV} is very important.

Acknowledgments

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