A Capacitive Coupling Interface with High Sensitivity for Wireless Wafer Testing

Gil-Su Kim, Makoto Takamiya, and Takayasu Sakurai
The Institute of Industrial Science
The University of Tokyo
Tokyo, Japan
gskim@iis.u-tokyo.ac.jp; mtaka@iis.u-tokyo.ac.jp; tsakurai@iis.u-tokyo.ac.jp

***Abstract*—A high-sensitivity capacitive-coupling interface is presented for wireless wafer testing systems. The transmitter is a buffer that drives the transmitter pad, and the receiver converts the data with various logic thresholds to that with optimum logic threshold. The receiver with the optimum logic threshold achieves the highest sensitivity of 25 mV at the data rate of 2 Gb/s in 0. 18 µm CMOS. The proposed receiver increases the communication distance over 4 times while providing tolerance against the distance-voltage-area variations.**

I. INTRODUCTION

The wireless wafer level testing, as a counterpart to a mechanical one, provides promising solutions to pick out known good die, such as improved reliability, increased production yield, and even reduced cost [1]. Reliability can be increased as a result of elimination of physical damage on I/O pads. In contrast, the mechanical wafer testing requires the careful control of probing needles to minimize the deformation of I/O pads. The wireless wafer level testing also increases the number of probes, which allows for highly parallel testing for multidie and reduces the cost of testing. Besides, the wireless approach can provide internal testing points as well as peripheral points, by adding wireless interfaces within the device under test (DUT); thus it allows for the flexible layout of tested pads.

For a wafer level testing, a wireless interface that is combined into the DUT must be implemented with small area so as not to degrade the established integration level of the DUT [1]. It also requires a high I/O bandwidth and should be tolerant to the variations in communication distance and transmitting voltage (or current) as well as misalignment between two interfaces, where the maximum communication distance is a measure of the tolerance for a given receiver sensitivity. Moreover, the interferences coming from adjacent channels must be kept low to maintain the signal integrity, which is essential for multichannel applications [1].

Inductive and capacitive couplings [1]−[8] can be adopted to implement a wireless wafer testing system. Since inductive coupling [1]–[4] is current driven, the transmission gain can be increased easily, which allows for long distance communications that can guarantee a good tolerance [2]. In contrast, capacitive coupling [5]–[8] is voltage driven, and its maximum transmission gain can be limited by the voltage swing of a transmitter driver and the coupling capacitance between two electrodes; thus its applications are usually restricted to short-distance communications [7].

The superior transmission capability of inductive coupling, however, leads to large area as well as high power consumption because the capability is obtained by increasing the current or the number of turns of an inductor. In addition, inductive coupling requires large pitch to minimize the crosstalk that is hardly shielded because it propagates in all directions in a transmitter and is superimposed in a receiver. Although modulation can be used to avoid the crosstalk, it limits the maximum data rate and requires huge inductors. Moreover, the inductive interconnection basically requires separate interfaces (i.e., inductors) which also give rise to area overhead [1].

In contrast, the capacitive crosstalk is not only less than the inductive one, but also can be blocked easily by shielding elements [9]. Consequently, one can realize a wireless interface with fine pitch. Moreover, since capacitive coupling can use the existing I/O pads instead of additional interfaces, the interface can be implemented with high area efficiency.

The bandwidth of inductive coupling is limited by the input capacitance of a receiver and the input resistance, whereas that of capacitive coupling is determined by the coupling capacitance between two electrodes, the input capacitance of a receiver, and the input resistance. Since the input capacitance of the receiver is normally larger than the coupling capacitance owing to large input capacitances of ESD circuits, particularly for wireless wafer level testing, both interfaces represent similar bandwidth limitations.

In this paper, a capacitive-coupling interface with the high sensitivity is presented to increase the communication distance

978-1-4244-4512-7/09/$25.00 ©2009 IEEE

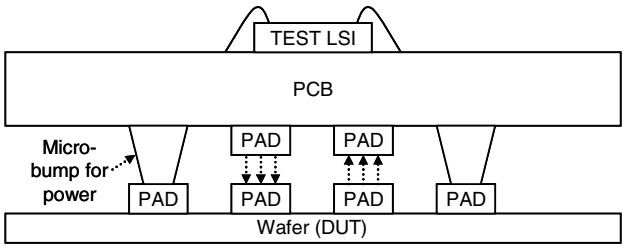

Fig.1. The wireless wafer testing system based on a capacitive-copling interface.

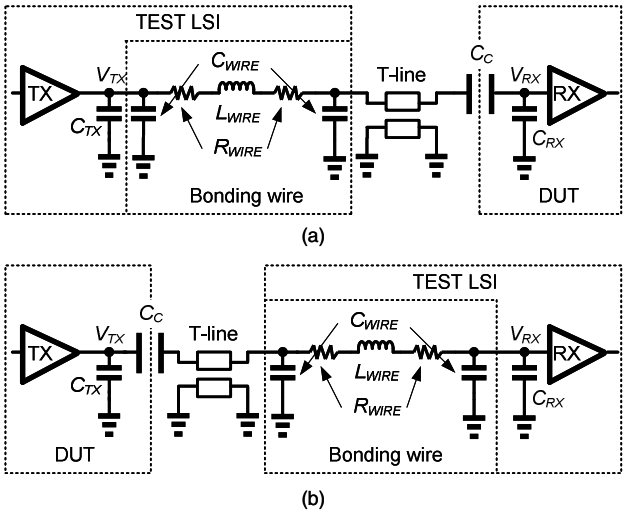

Fig. 2. Simplified channel models for (a) The TEST LSI-to-DUT. (b) The DUT-to-TEST LSI.

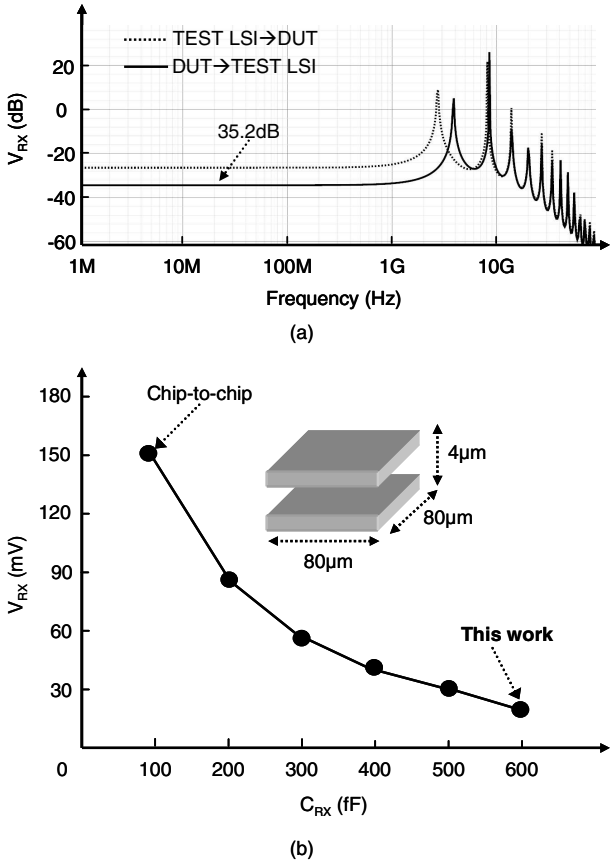

Fig. 3. (a) Simulated frequency characteristic of the channel. (b) Estimated minimum received voltages against different capacitances of a receiver for the wireless wafer probing system.

while providing tolerance against distance-voltage-area variations for wireless wafer testing.

II. Wireless Wafer Tesing System

Fig. 1 illustrates the wireless wafer testing system based on a capacitive-coupling interface. The upper pads are implemented on the bottom side of a printed circuit board (PCB) that can reduce cost and can easily be customized, whereas the lower pads are realized on the tested wafer. The power is supplied through a physical connection such as microbumps [6]. Fig. 2 illustrates simplified channel models for the wireless wafer testing system. In contrast to chip-to-chip interfaces (e.g., 3-D ICs [2]–[4], [6]–[8]), the wireless wafer testing system has large input capacitances, C_{RX} ($\simeq C_{ESD} + C_{PAD} + C_{WIRE}$) caused by ESD protection circuits, which results in both significant signal attenuation and bandwidth limitation in a receiver, where C_{ESD} is the capacitance of ESD, C_{PAD} is the capacitance of the pad, and C_{WIRE} is the capacitance of the bonding wire. The simulation results (Fig. 3(a)) indicate that the signal attenuation is greater than 35 dB for the DUT-to-TEST LSI. This value corresponds to the received voltage (V_{RX}) of about 30 mV with a transmitted voltage of 1.8 V. The estimated minimum V_{RX} against different input capacitances of a receiver is shown in Fig. 3(b). A coupling capacitor with the distance of 4 μm and the area of 80 μm × 80 μm is used for the estimation. Consequently, the signal attenuation due to the large input capacitance of a receiver limits the minimum area of pads, the misalignment between two pads, the maximum allowable distance, and the minimum voltage swing of the transmitter driver. The high sensitivity of the receiver can mitigate all these limitations, and, in turn, increases the tolerance against the distance-voltage-area variations.

In this paper, a capacitive-coupling interface with the highest sensitivity of 25 mV at the data rate of 2 Gb/s in 0.18 μm CMOS process is presented.

III. High-Sensitivity Optimum Logic Threshold Receiver

A. Interface Characteristic

In contrast to previous works [1]–[7], the proposed interface has a large *RC* time constant (τ) for high-sensitivity, high-speed operation, where τ has its usual meaning and is determined by the resistance and the capacitance of a receiver. The receiver with small τ restores asymmetric and triangular pulses with filtered low-frequency components [5], as shown

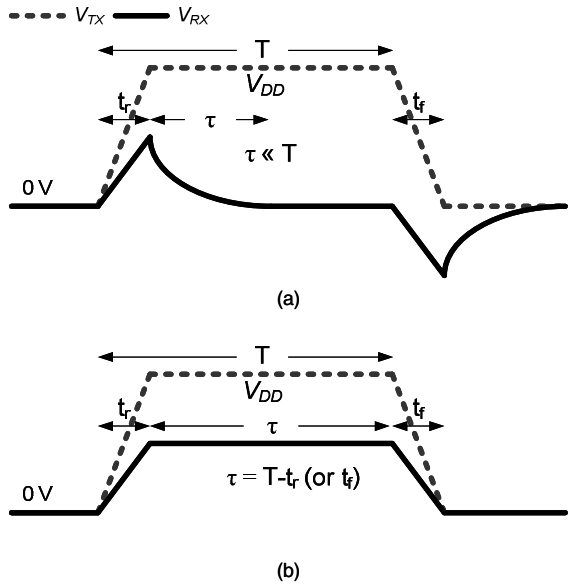

Fig. 4. Transient responses for (a) The small-τ interface. (b) The large-τ interface.

in Fig. 4(a). The signals with attenuated pulse swing, which is caused by the channel characteristic, represent narrow pulse width, which reduces the timing margin for data recovery and limits the maximum data rate [6]. Thus, the small-τ receiver with a limited timing margin requires complex timing control circuits to recover transmitted signals for a given data rate [1], [2], [5], [6]. In contrast, a large-τ receiver maintains the original forms of transmitted signals (Fig. 4(b)); thus one can achieve the maximum timing margin, even when the pulse swing becomes smaller owing to the channel characteristic [10]. As a result, the large-τ receiver exhibits higher sensitivity and a higher data rate than the small-τ receiver.

The large-τ receiver, however, suffers from the DC-offset (i.e., various logic thresholds) as a result of distance-area-supply voltage variations and the zero wander effect wherein the received signals go down below '0' V [10]. The direct application of a fixed reference results in both low sensitivity and pulse width distortion, which in turn increase BER. In order to remove the DC-offset, one can insert a coupling capacitor in front of the receiver. However, the required capacitance is normally large [10]. Feedback topology can remove the DC-offset and the zero wander effect, but it limits the maximum data rate and is not suitable for high-speed applications [10]. The proposed receiver employs feedforward topology without the coupling capacitor and converts the received signals into other signals with the optimum logic threshold (OLT) in order to eliminate the DC-offset and the zero wander effect.

B. Optimum Logic Threshold Receiver

Fig. 5(a) shows the schematic diagram of the proposed OLT receiver. The receiver is composed of a level shifter, a subtractor, a replica bias circuit, a comparator, and a reset circuitry. The subtractor and replica bias circuit provide output signals, V_2 and V_4, to the following comparator (sense amplifier-type flip-flop), respectively. The *RC* network consisting of resistor *R* and input capacitor of M1 produces an averaged signal, $\overline{D_{RX,IN}}$, with the same logic threshold voltage, V_{TH}, as those of the received signal, $D_{RX,IN}$, under a balanced data pattern (e.g., 8B/10B encoding). After an appropriate level shift by ΔV, the circuit consisting of M3 and M4 subtracts the shifted signal (V_1) from $D_{RX,IN}$ and generates the output signal, V_2, with a constant V_{TH}, as shown in Fig. 5(b), where the output voltage of the subtractor can be defined as

$$V_2 = (V_{DD} - \Delta V) + (D_{RX,IN} - \overline{D_{RX,IN}}). \quad (1)$$

Equation (1) indicates that the OLT receiver can recover both small and large $D_{RX,IN}$ with different V_{TH}, with high sensitivity,

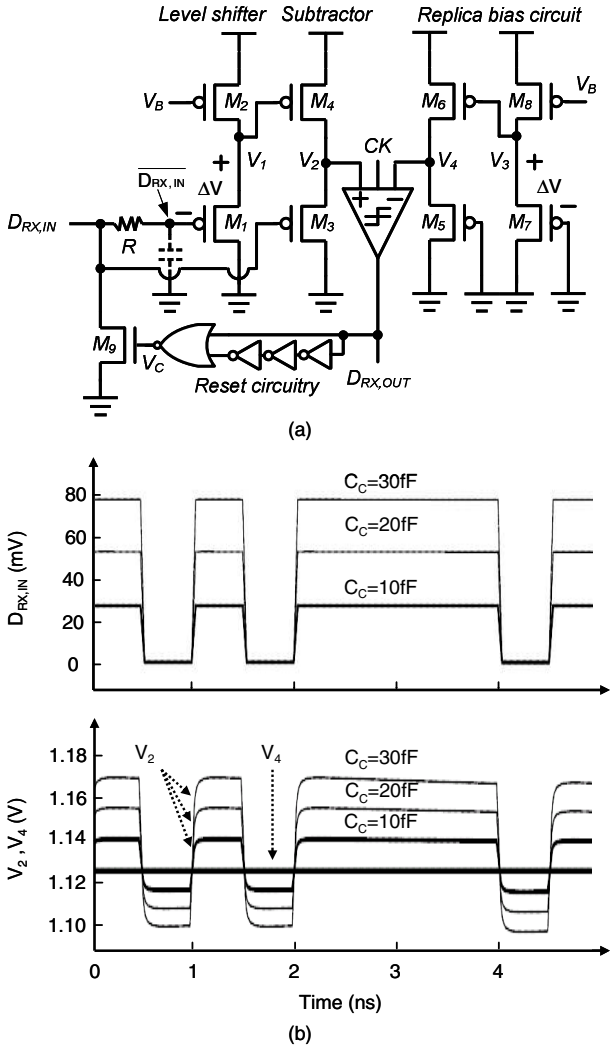

Fig. 5. (a) Schematic diagram of proposed OLT receiver. (b) Simulated waveforms at the data rate of 2 Gb/s.

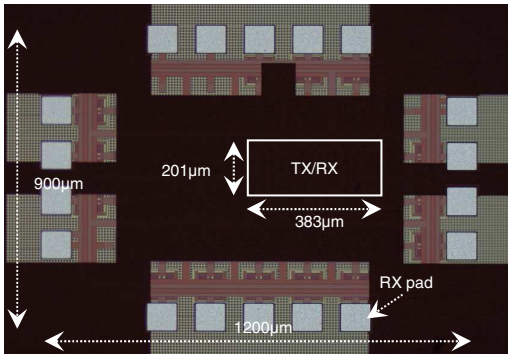

Fig. 6. Micrograph of test chip.

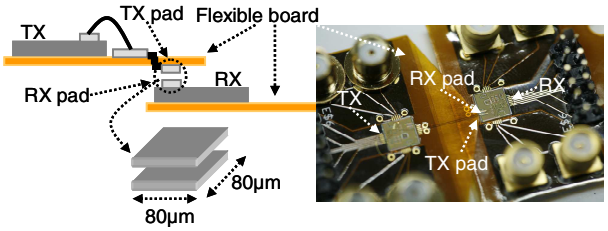

Fig. 7. Test environment of test chip.

because the subtractor removes $\overline{D_{RX,IN}}$ from $D_{RX,IN}$ and produces signals with the optimum logic threshold.

A replica bias circuit, M5-M8, provides a fixed reference voltage, V_4, which is equal to V_{TH} of V_2, which can be easily achieved by applying the same potentials to the gates of M5 and M7.

A reset circuitry provides reset signal, V_C, to M9, in order to maintain the bottom level of $D_{RX,IN}$. The zero wander effect can be easily eliminated by the reset signal because the continuous fall of the bottom level of $D_{RX,IN}$ is prevented by the reset to '0' V after the transitions of output signals, $D_{RX,OUT}$.

IV. Experimental Results

The micrograph of the test chip fabricated by the 1.8 V, 0.18 μm CMOS process is shown in Fig. 6.

Fig. 7 shows the test environment for the proposed OLT receiver. For chip-to-board communication, a TX pad of 80 μm × 80 μm is patterned on the thin transparent flexible board, and one of the peripheral I/O pads is used as the RX pad of the same size.

The BER was measured as a function of the supply voltage of TX and the simulated received voltage of RX (Fig. 8) using the internal PRBS and BER checker with pattern lengths of 2^{33}-1. For a received voltage of 25 mV and a communication distance of 4 μm, the BER is $<10^{-10}$ with the maximum data of 2 Gb/s. The measured performance is summarized in Table I. The performance of the proposed interface is at least 4 times superior to those of previous works. The OLT receiver with the sensitivity of 25 mV can increase the communication distance and reduce the pad size over 4 times, respectively. Note that the increased maximum communication distance

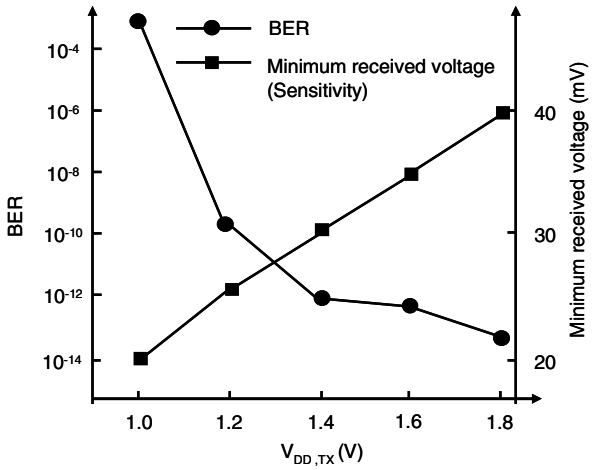

Fig. 8. Measured BER and simulated minimum received voltage.

Table I. Performance summary.

Technology		0.18 μm CMOS
Supply voltage		1.8 V
Max. data rate		2 Gb/s
Sensitivity		25 mV
Input cap. (RX)		>600 fF
BER		$<10^{-10}$
Core power @2 Gb/s	TX	4.87 μW
	RX	1.63 mW
Core area	TX	60 μm²
	RX	2900 μm²

improves the tolerances against the distance-supply voltage-area variations.

V. Conclusion

A capacitive-coupling interface fabricated by the 1.8 V, 0.18 μm CMOS process has been proposed for wireless wafer testing systems. The proposed optimum logic threshold receiver with high sensitivity not only extends the communication distance between two electrodes, but also increases the tolerance to the distance-voltage-area variations.

Acknowledgement

This work is part of ASET 3D-Integration Technology project of FY 2008 under a NEDO entrustment. Useful discussions with members of 3D-Integration Technology project are acknowledged.

References

[1] C. V. Sellathamby, M. M. Reja, L. Fu, B. Bai, E.Reid, S. H. Slupsky, I. M. Filanovsky, and K. Iniewski, "Non-contact wafer probe using wireless probe cards," in *Proc. IEEE Int. Test Conf.*, 2005, pp. 1-6.

[2] N. Miura, D. Mizoguchi, M. Inoue, K. Niitsu, Y. Nakagawa, M. Tago, M. Fukasishi, T. Sakurai, and T. Kuroda, "A 1 Tb/s 3 W inductive-

coupling transceiver for 3D-stacked inter-chip clock and data link," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 111-122, Jan. 2007.

[3] N. Miura, H. Ishikuro, K. Niitsu, T. Sakurai, and T. Kuroda, "A 0.14 pJ/b inductive-coupling transceiver with digitally-controlled precise pulse shaping," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 285-291, Jan. 2008.

[4] N. Miura, Y. Kohama, Y. Sugimori, H. Ishikuro, T. Sakurai, and T. Kuroda, "A high-speed inductive-coupling link with burst transmission," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 947-955, Mar. 2009.

[5] J. Kim, I. Verbauwhede, and M.-C. F. Chang, "A 5.6-mW 1-Gb/s/pair pulsed signaling transceiver for a fully ac coupled bus," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1331-1340, Jun. 2005.

[6] L. Luo, J. M. Wilson, S. E. Mick, J. Xu, L. Zhang, and P. D. Franzon, "3 Gb/s ac coupled chip-to-chip communication using a low swing pulse receiver," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 287-296, Jan. 2006.

[7] D. Hopkins, A. Chow, R. Bosnyak, B. Coates, J. Ebergen, S. Fairbanks, J. Gainsley, R. Ho, J. Lexau, F. Liu, T. Ono, J. Schauer. I. Sutherland, and R. Drost, "Circuit techniques to enable 430Gb/s/mm^2 proximity communication," in *IEEE ISSCC Dig. Tech. Papers*, 2007, pp. 368-369.

[8] A. Fazzi, R. Canegallo, L. Ciccarelli, L. Magagni, F. Natali, E. Jung, P. Rolandi, and R. Guerrieri, "3-D capacitive interconnections with mono- and bi-directional capabilities," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 275-284, Jan. 2008.

[9] W. J. Dally and J. W. Poulton, *Digital Systems Engineering*, New York: Cambridge University, 1998, Ch. 6, pp. 267-280.

[10] T. J. Gabara and W. C. Fischer, "Capacitive coupling quantized feedback applied to conventional CMOS technology," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 419-427, Mar. 1997.