13.2 A 1.8V 30nJ Adaptive Program-Voltage (20V) Generator for 3D-Integrated NAND Flash SSD

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Decreasing power consumption is the key design issue of SSDs. A typical SSD consists of more than 16 NAND Flash memories, DRAMs and a NAND controller. Since the NAND write performance is 10MB/s [1,2], to raise the write speed of SSD to the level of HDD, 100MB/s, 8 or more NAND chips in SSD are simultaneously programmed. As the feature size decreases, the total bitline capacitance in a chip increases beyond 200nF. If 8 or more NAND chips operate in parallel, a large current of 800mA flows to charge the bitline capacitance in a sub-30nm SSD [3]. A good strategy to decrease the power is lowering the supply voltage, V_{DD}, from 3.3 to 1.8V. Yet, at 1.8V, the power consumption of conventional charge pumps, used to generate the 20V program voltage, V_{PGM}, drastically increases and the total power consumption of the NAND does not decrease, as shown in Fig. 13.2.1(a). The charge-pump area more than doubles, which increases the NAND chip area by 5 to 10%. To overcome this problem, we implement a low-power program-voltage generator (PVG) using a boost converter with an adaptive-frequency and duty-cycle (AFD) controller.

Figure 13.2.1(b) shows our 3D-integrated SSD. NAND chips, DRAM, a NAND controller and the PVG are integrated with SiP. The PVG consists of an inductor in an interposer, the high-voltage MOS (HVMOS) and the AFD controller. An inductor is available with no area penalty by using wiring in the interposer connecting dice. The die size of the NAND decreases by 5 to 10% because no charge pump is needed. The HVMOS is fabricated with a mature NAND process and its area is just 15% of the conventional charge pump. Since the die size of the AFD controller is 0.188mm^2 with a 0.18μm CMOS process, it can be integrated in a NAND controller with a negligible area increase.

A PVG using a boost converter was reported for a NOR flash memory [4]. A comparison between the PVG for a NOR flash memory and for a NAND flash memory is summarized in Fig. 13.2.2(a). In a NOR flash memory, the load of the PVG is resistive. The PVG continuously supplies a load current of 20mA at an output voltage of 5V. With a resistive load and a low output voltage, a conventional PWM is employed [4]. In a NAND flash memory, the load is capacitive and the output voltage, V_{PGM}, is 20V. During program, V_{PGM} is applied to the wordline and a DC load current of 20μA flows. Also, a PVG for a NAND Flash memory should support on and off modes to save power. In this condition both switching frequency and duty cycle must be dynamically optimized and the conventional PWM of changing only the duty cycle cannot be used.

To identify the most power-efficient frequency and duty cycle, an input supply current, I_{DD}, is measured with our PVG. As shown in Fig. 13.2.2(b), each V_{PGM} has a different optimal frequency and duty cycle that minimizes I_{DD}. In other words, the power efficiency is a function of V_{PGM}, the switching frequency and a duty cycle, since the PVG operates in a discontinuous mode with a capacitive load. With a bit-by-bit program-verify scheme, in each program cycle, V_{PGM} is incremented by 0.5V from 15 to 25V [5]. For each V_{PGM}, the our AFD controller adaptively manages the switching frequency and the duty cycle simultaneously so that the energy loss is minimized.

Figure 13.2.3 shows the PVG with the AFD controller. V_{PGM} is monitored with three comparators and the control logic selects the proper switching frequency and duty cycle from the registers, $Reg._L$, $Reg._M$, and $Reg._H$. These registers store a table of the frequency and duty cycle that minimize both the power and the output-voltage fluctuation. A digitally controlled oscillator (DCO) is depicted in Fig. 13.2.4. The DCO consists of current-reference circuits and a couple of capacitor arrays. The DCO enables the clock shape to be determined only by the resistor and the capacitor, since the reference current I_{REF} is copied to the node V_{CAPA} and V_{CAPB} with a current mirror [6]. The frequency and the duty cycle are robust against V_{DD} fluctuation, global transistor V_T variation and temperature variation. The switching times of the DCO, $T_{ON} = R{\cdot}C_{A1\text{-}An}$, and $T_{OFF} = R{\cdot}C_{B1\text{-}Bn}$. Since $C_{A1\text{-}An}$ and $C_{B1\text{-}Bn}$ are independently selected according to the data in the registers, T_{ON} and T_{OFF} are independently controlled.

To suppress the V_{PGM} fluctuation, the AFD controller dynamically changes the frequency and the duty cycle in three steps, as shown in Fig. 13.2.5. In the first step, a power-efficient lower frequency is chosen. The AFD controller outputs pulses with the switching frequency and duty cycle, f_L and D_L, determined by $Reg._L$. V_{PGM} rises coarsely and rapidly until V_{PGM} reaches V_{REFL}. With f_L and D_L, the voltage increment for each pulse is 5V. The frequency becomes higher in the second and the third steps. In the second step, the AFD controller changes the switching pulse from frequency and duty cycle f_L and D_L to f_M and D_M as determined by $Reg._M$. Finally, the AFD controller finely raises V_{PGM} with f_H and D_H toward the target voltage. When V_{PGM} reaches the target voltage, the AFD controller stops switching pulses to save power. As a result, the PVG raises V_{PGM} more than 3× faster than the conventional charge pump with minimum power. V_{PGM} is precisely controlled with less than 0.3V fluctuation, which enables a tight memory-cell V_T distribution.

Key features of this work and experimental results are summarized in Fig. 13.2.6. Figure 13.2.7 shows the micrograph of the breadboard model of the SSD consisting of the HVMOS chip (0.35 × 0.50mm^2), the AFD controller chip (0.67 × 0.28mm^2), a 270nH 0.5Ω inductor in an interposer (5 × 5mm^2), and a 56nm 16Gb NAND Flash memory chip. The measured waveforms during the program of a 56nm 16Gb NAND flash memory with the PVG are shown in Fig.13.2.6. When a write command inputs to the NAND, the ready/busy signal turns to low and the NAND goes into the busy state. The program voltage is supplied from the PVG and the program pulse is applied to the memory cells. Then, the verify-read detects that all memory cells are successfully programmed and the ready/busy-signal returns to high.

The measured power consumption of the PVG is 30nJ, which is 12% of the conventional charge pump. Measured rising time of the PVG is 0.92μs (at V_{DD} of 1.8V and V_{PGM} of 15V), while that of the charge pump is 3.45μs. As the rising time of the V_{PGM} decreases by 2.53μs, the program pulse width is shortened by 2.53μs. As a result, the total program time of a NAND flash memory, a sum of the program pulse width and the verify-read time, is 7.8% shorter than the conventional 1.8V NAND Flash memory. The area of the HVMOS chip is 15% of the charge pump without a control circuit or an oscillator. By decreasing V_{DD} from 3.3V to 1.8V, the total power consumption of a NAND flash memory decreases by 68%, as shown in Fig. 13.2.1(a).

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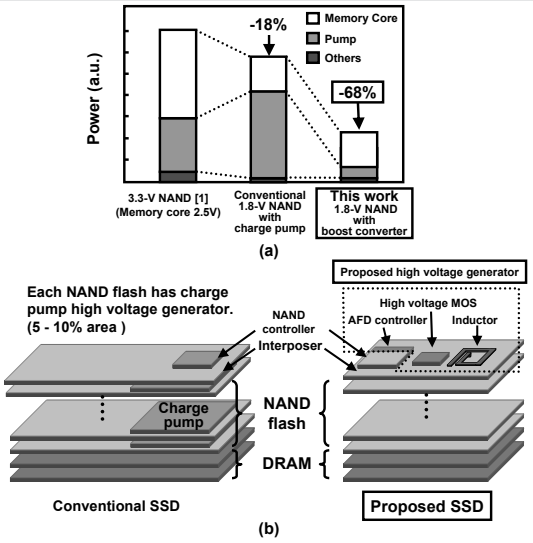


Figure 13.2.1: (a) Comparison of the power consumption of NAND flash memories and (b) structure of the proposed 3D-integrated SSD.

	PWM [4]	This work
Load	Resistive	Capacitive
V_{PGM}	5V	20V
I_{LOAD}	20mA	20µA
Operation	Continuously on	On-and-off
Control	Duty cycle only	Frequency and duty cycle

(a)

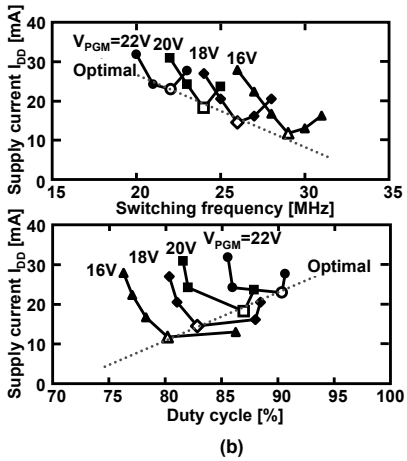


Figure 13.2.2: (a) Comparison of the conventional boost converter [4] and this work and (b) measured optimal switching frequencies and duty cycles for various V_{PGM}.

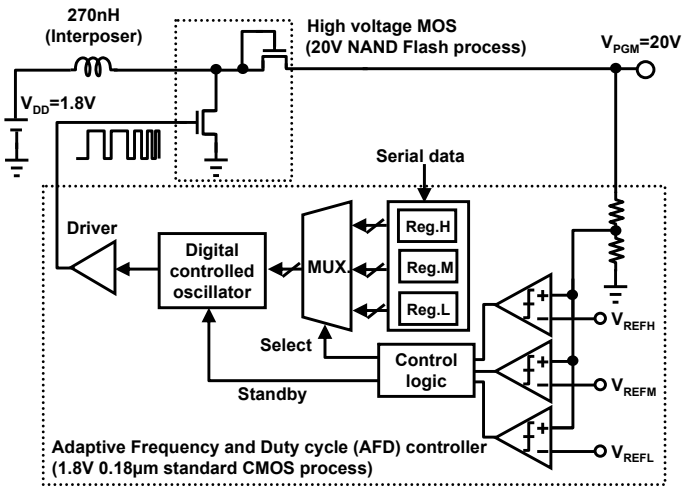


Figure 13.2.3: Circuit diagram of the adaptive high-voltage generator.

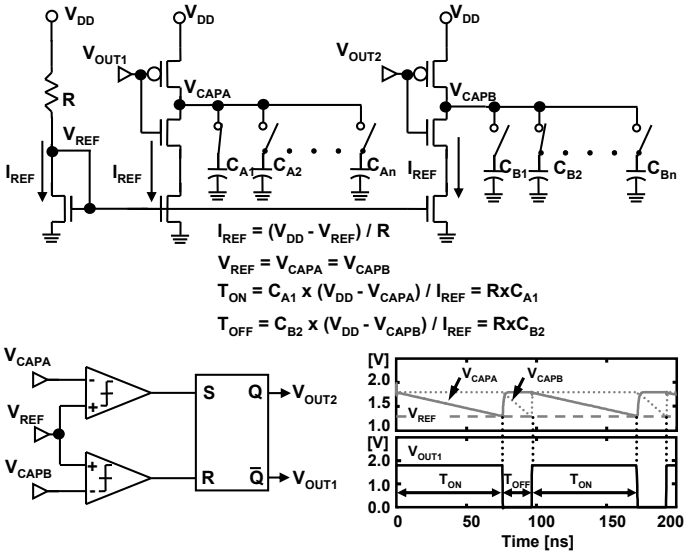


Figure 13.2.4: Digitally controlled oscillator (DCO).

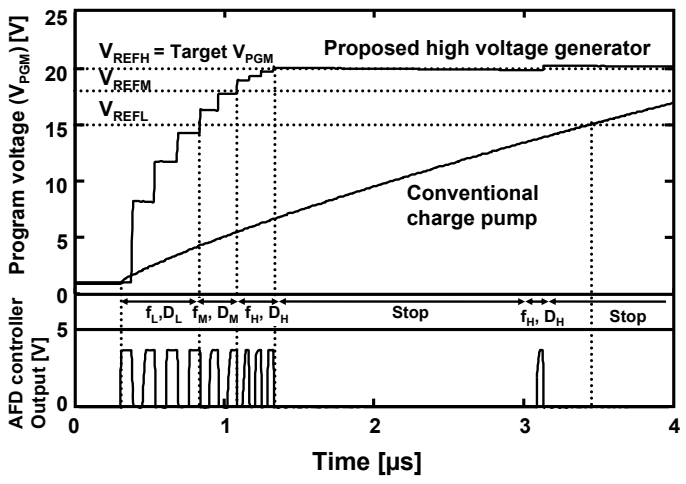
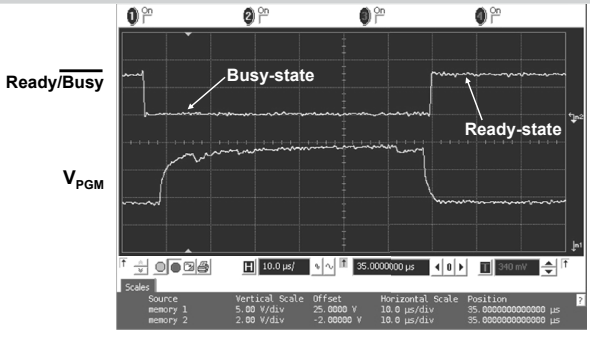


Figure 13.2.5: Simulation result.



	This work (Measured)	Conventional Charge Pump (Simulated)
Power consumption	30nJ (12%)	253nJ (100%)
Chip Area (high voltage MOS)	0.175mm² (15%)	1.19mm² (100%)
Chip Area (AFD controller)	0.188mm²	-----
Rising time	0.92µs (27%)	3.45µs (100%)
Technology (high voltage MOS)	20V NAND flash process	--------
Technology (AFD controller)	1.8V 0.18µm standard CMOS	--------
Supply voltage	1.8V	1.8V

Figure 13.2.6: Experimental results and key features.

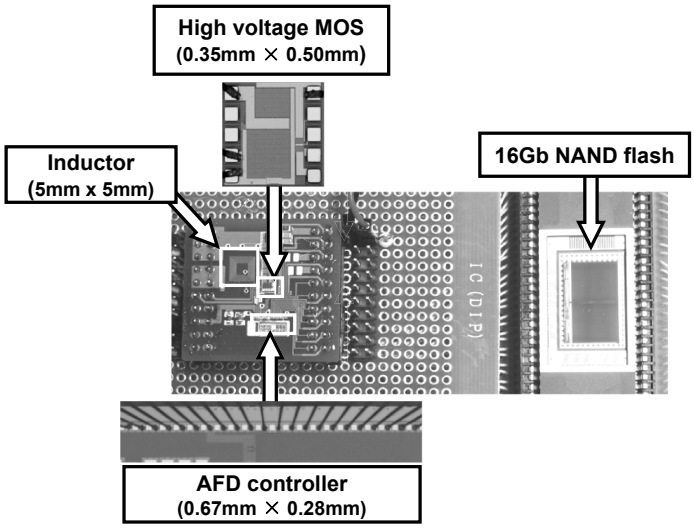


Figure 13.2.7: Die micrograph.

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