A 107-pJ/bit 100-kb/s 0.18-μm Capacitive-Coupling Transceiver With Data Edge Signaling and DC Power-Free Pulse Detector for Printable Communication Sheet

Lechang Liu, Makoto Takamiya, *Member, IEEE*, Tsuyoshi Sekitani, Yoshiaki Noguchi, Shintaro Nakano, Koichiro Zaitsu, Tadahiro Kuroda, *Fellow, IEEE*, Takao Someya, *Member, IEEE*, and Takayasu Sakurai, *Fellow, IEEE*

***Abstract*—A novel communication system which simultaneously achieves the mobility of wireless communication and the low-power performance of wireline communication is developed with a printable sheet. By combining meter-scale wireline communication and micrometer-scale wireless capacitive-coupling communication, the proposed communication system enables multiple electronic objects scattered over tables, walls, and ceilings to communicate contactlessly with each other by establishing communication paths without cumbersome physical connections. The transceiver developed for the 20 cm × 20 cm communication sheet features a data-edge-signaling transmitter and a dc power-free pulse detector, thereby achieving the lowest energy of 107 pJ/bit at 100 kb/s in wireless communications at a distance of 60 cm in 0.18-μm CMOS.**

***Index Terms*—Capacitive coupling, inductive coupling, low power, proximity communication, transceiver.**

I. Introduction

UBIQUITOUS electronics refers to electronic environments that are sensitive and responsive to the presence of people. In a ubiquitous electronics world, devices work in concert to support people to carry out their activities and tasks in an easy natural way using information and intelligence that is hidden in the network connecting these devices. The vision on the future of consumer electronics and telecommunications is shown in Fig. 1(a). To protect safety and security, promote healthcare and welfare, and provide entertainment and convenience, 1000–10 000 electronic devices are distributed around the user's environment.

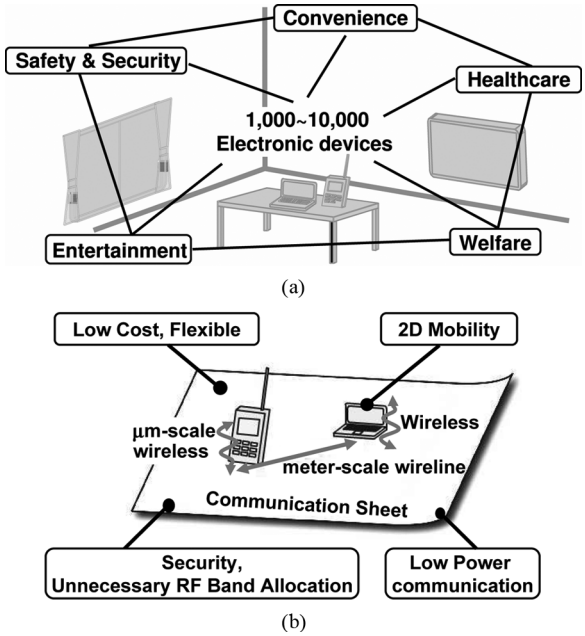


Fig. 1. (a) Ubiquitous electronics. (b) Proposed commutation system.

The future ubiquitous electronics requires a huge number of chips, and thus, each of the chips should be implemented at a minimal power level. To capture the user's environment, the basic idea is to integrate sensor networks into wireless communication systems. However, singular wireless communication systems attain improved flexibility and mobility at the expense of increased circuit complexity and power consumption over their wireline counterparts. In this paper, a novel communication method which simultaneously achieves the mobility of wireless communication and the low-power performance of wireline communication is implemented with a low-cost printable sheet [1], [2]. The proposed commutation system is shown in Fig. 1(b). By combining meter-scale wireline communication and micrometer-scale wireless capacitive-coupling communication, the sheet enables multiple electronic objects scattered over tables, walls, and ceilings to communicate contactlessly with

Manuscript received October 15, 2008; revised December 10, 2008. First published February 18, 2009; current version published November 04, 2009. This work is supported in part by CREST, by the Japan Science and Technology Agency, and by the the Ministry of Education, Culture, Sports, Science and Technology. This paper was recommended by Associate Editor Y. Massoud.

M. Takamiya is with the VLSI Design and Education Center, The University of Tokyo, Tokyo 153-8505, Japan.

T. Sekitani, Y. Noguchi, and K. Zaitsu are with the Quantum-Phase Electronics Center, School of Engineering, The University of Tokyo, Tokyo 113-8656, Japan.

S. Nakano was with The University of Tokyo, Tokyo 113-8656, Japan. He is now with Toshiba Corporation, Tokyo, 141-8664, Japan.

T. Kuroda is with the Department of Electronics and Electrical Engineering, Keio University, Yokohama 223-8522, Japan.

T. Someya is with the Department of Applied Physics and the Quantum-Phase Electronics Center, School of Engineering, The University of Tokyo, Tokyo 113-8656, Japan.

L. Liu and T. Sakurai are with the Institute of Industrial Science, The University of Tokyo, Tokyo 153-8505, Japan (e-mail: llch@iis.u-tokyo.ac.jp).

Digital Object Identifier 10.1109/TCSI.2009.2015596

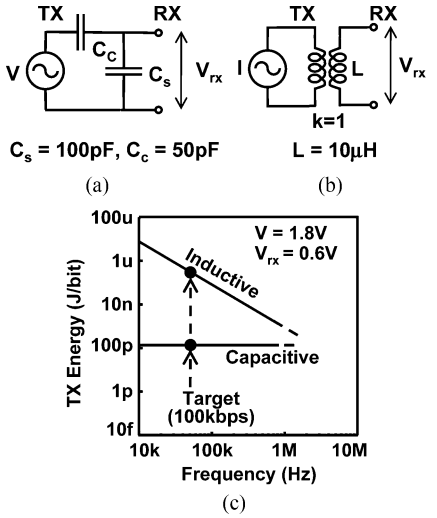


Fig. 2. Comparison of capacitive and inductive coupling. (a) Capacitive coupling. (b) Inductive coupling. (c) Energy–frequency characteristic.

each other by establishing communication paths without cumbersome physical connections. Together with the wireless power transmission sheet [3], [4], the presented communication sheet can build an infrastructure for ubiquitous electronics, wireless sensor networks, and ambient intelligence.

The overview of the whole communication system is described in Section II. Sections III and VI present the proposed data-edge-signaling transmitter (TX) and the dc power-free receiver (RX), respectively. Experimental results are presented in Section V, and Section VI concludes this paper.

II. Printable Communication Sheet

A. Capacitive versus Inductive Coupling

The communication between the transceiver and the sheet is similar to the conventional proximity communication [5]–[11]. Proximity communication is based on the observation that faster lower cost communication is possible over shorter distances. For the communication sheet, this is achieved by placing two sheets face-to-back in a manner that aligns the pads of the TX/RX sheet with the pads of the routing sheet. Proximity communication can be implemented by capacitive and inductive coupling. The option between capacitive and inductive coupling is complicated by various factors. If the received signal is large enough so that the power consumption of the receiver can be ignored, the power consumption of the whole system is only determined by the transmitter.

For the capacitive-coupling system, the transmitter requirement is straightforward. A simple chain of inverters with adequate drive strength is usually sufficient. Fig. 2(a) shows the simplified schematic of capacitive-coupling system. The capacitances C_c and C_s represent the coupling and parasitic capacitances of the sheet, respectively. C_c and C_s form a capacitance divider and reduce the received signal swing on the receiver pad. The energy consumption of the capacitive-coupling system can be approximated by

$$E = CV^2, \qquad C = C_c||C_s. \tag{1}$$

Compared with the capacitive-coupling system, an inductive-coupling system can transfer both power and signal information across an interface. A large size of inductors is required to send both dc and ac signals, which negates the ability to have high-density integration. However, if the inductive coupling is only used to transfer ac information, the size of inductors can be reduced, and a simple current-mode driver is sufficient. Fig. 2(b) shows the simplified schematic of the inductive-coupling system. For the given receiver voltage $V_{\rm rx}$, the energy consumption of the transmitter can be approximated by

$$E = LI^2, \qquad I = \frac{V_{\rm rx}}{j\omega L}. \tag{2}$$

In the communication sheet, the available maximum effective inductance is 10 μH, and the worst case parasitic capacitance is 100 pF. If the given receiver voltage $V_{\rm rx}$ is 0.6 V, the required coupling capacitance should be 50 pF. Fig. 2(c) shows the calculated frequency dependence of TX energy consumption. The target data rate is limited to 100 kb/s by the bandwidth of the plastic microelectromechanical system (MEMS) switches. At the target data rate, the energy of capacitive coupling is two orders of magnitude lower than that of inductive coupling. Therefore, the capacitive coupling is used in such a low-data-rate and low-parasitic-capacitance system.

B. System Overview

The overview of the whole system is shown in Fig. 3(a). The point-to-point communication is achieved by combining the meter-scale wireline communication on the sheet and the micrometer-scale proximity communication between the sheet and the transceiver. This work implements proximity communication by capacitively coupling the transmitter to the receiver. The transmitter drives a plate of metal on the TX sheet that couples to a corresponding plate of routing line on the communication sheet, and the plate on the other end of the routing line, in turn, drives the receiver on the RX sheet. The typical pad distance for the capacitive coupling is 75 μm, which corresponds to 50-pF capacitance. In this application, differential signaling is required because there is no common ground among the TX, communication, and RX sheets. The 90 ° rotation of the TX/RX sheet can be countered by the other two additional pads.

The communication route is dynamically formed using the plastic MEMS switches, and the routing information is stored in the organic nonvolatile memories [2]. The "1"–"0" current ratio of organic nonvolatile memory exceeds 10^5, and the retention time is more than 15 days in air. In practical application, the routing on the communication sheet is similar to the routing of a 2-D field-programmable gate array. With the increased size of the communication sheet and the increased number of electronic objects scattered over the sheet, specially designed programmable switch blocks are required, and the interference between different TX/RX pairs due to crosstalk and misalignment is inevitable [12]. To simplify the analysis of the whole communication system, a routing model for nonoverlapped point-to-point communication is proposed in Fig. 3(b). The sheet is composed of 8×8 units, and every unit consists of four pads. The communication between each two units is achieved by turning on the adjacent two MEMS switches and

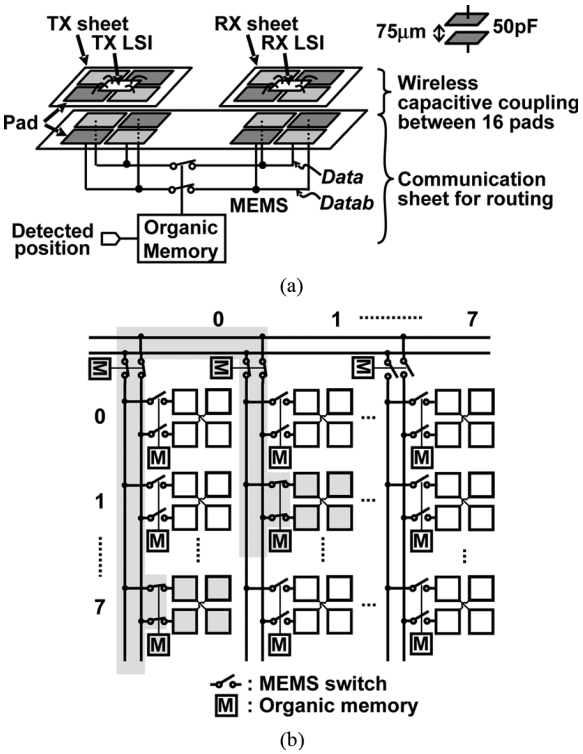


Fig. 3. (a) Overview of the communication system. (b) Model of the communication sheet.

the top two routing switches. Thus, only four switches are required for the point-to-point communication. Since the information transmitted over the sheet is confined in a small space close to *ad hoc* routed paths, the system is free from the issues related with radio-frequency band allocation which has already been tight.

C. Device Structure

The device structure of the communication sheet is shown in Fig. 4(a). It consists of five low-cost printed sheets: a 16×16 pad array for capacitive coupling, two 9×8 MEMS switching matrices for differential signal routing, a 9×8 organic nonvolatile memory array for routing information storage, and an 8×8 position-detection coil array. The 16×16 capacitive-coupling pad arrays are fabricated on a polyimide film. The side length of the square pad is 9.7 mm, and the distance between each pad is 3.0 mm. Silver gate electrodes and polyimide gate dielectric layers are patterned by using inkjet printing.

The MEMS switching matrix is formed by using inkjet printing and screen printing. The electrodes for electrostatic attraction are patterned on a 25-μm-thick polyimide membrane. Compared with an organic FET switch, a MEMS switch provides lower ON-resistance and lower parasitic capacitance, which contributes to low energy/bit communication. When 9 V is applied to the control electrodes of the MEMS switch, the resistance changes from 1 MΩ to 20 Ω. The maximum frequency response of the MEMS switch is 1 kHz.

The position-sensing coil array is manufactured by screen printing. The inner diameter of the copper coils is 10 mm. Both the width and spacing of the copper lines are 100 μm. The inductance and resistance are 20 μH and 17 Ω, respectively. The

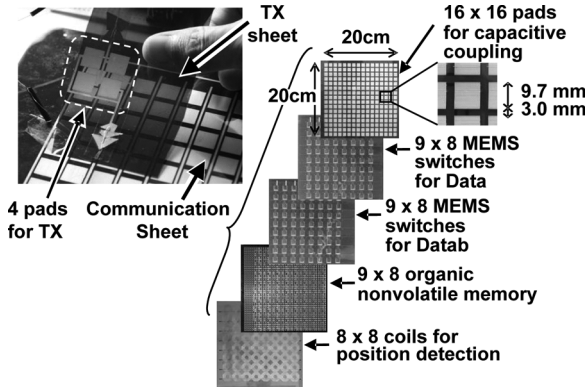


Fig. 4. Device structure of communication sheet.

measured result shows that the deterioration of position-detection sensitivity due to the four sheets above the coil array is only 7% and that this value can be ignored. The principle of the position-sensing sheet is similar to the power transmission sheet of the literature [4]. A voltage of $\pm$ 10 V at a resonance frequency (2.95 MHz) is applied to the position-sensing cells. When the distance between the position-sensing coil and the receiver coil reduces, the output voltage will be increased by 91%.

III. Data-Edge-Signaling Transmitter

A. DC Wander Effect

For the capacitive coupling, a key constraint to consider is that, when a long string of "1s" and "0s" is passed through the transmitter, the signal experiences the dc wander effect. For the capacitive-coupling system in Fig. 3(a), the series coupling capacitance yields a high-pass characteristic. In the time domain, the high-pass filtering passes the time rate change of the voltage signal $(\mathrm{d}v/\mathrm{d}t)$. The receiver will receive positive pulses for rising edges and negative pulses for falling edges. This makes the detection of the signal more difficult since the dc drift of the signal causes a loss of noise margin.

B. Data Edge Signaling

Conventionally, quantized feedback is introduced to generate a complementary signal to compensate the decaying signal [13]. In this paper, the input non-return-to-zero (NRZ) signal is converted into a return-to-$V_{\mathrm{DD}}/2$ signal pulse to avoid this constraint. As shown in Fig. 5(a), compared with the previous synchronous circuits [14], the proposed asynchronous circuits have no global clocks, and the operation is triggered by signal transitions, potentially having the advantages of low power dissipation.

Fig. 5(b) shows the schematics of the proposed transmitter. The modulated data are achieved by switching the input data and the output of the half V_{DD} generator [15]. The edge detector is used to generate the switching signal for the selector by detecting both the rising and falling edges of the input data. Fig. 5(c) shows the simulated dependence of the power consumption on the data-transition probability at 100 kb/s. The power consumption of the transceiver is proportional to the data-transition probability. In the conventional synchronous topology, the transmitted signal changes at every clock cycle, and the consumed power is constant for different data rates. In

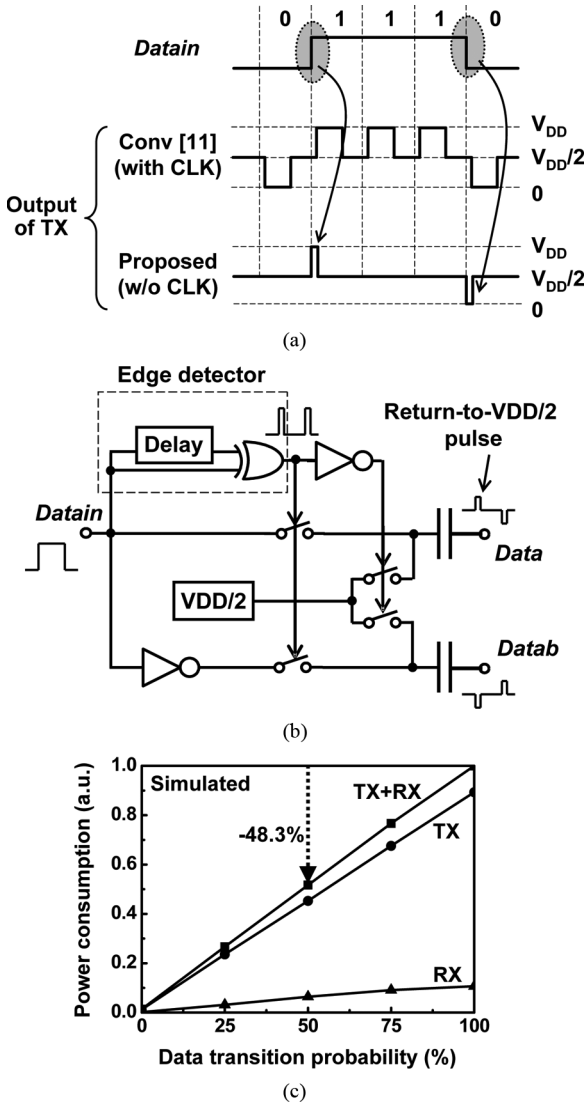


Fig. 5. Data-edge-signaling transmitter. (a) DC wander effect. (b) Circuit schematic. (c) Power dependence on data transition.

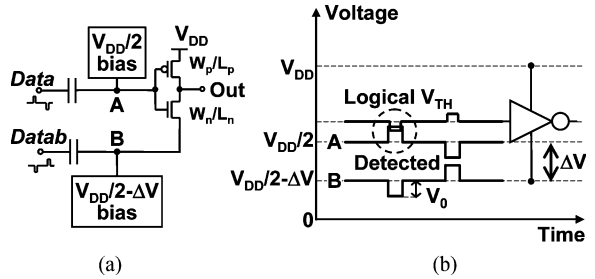


Fig. 6. DC power-free pulse detector. (a) Circuit schematic. (b) Operation principle.

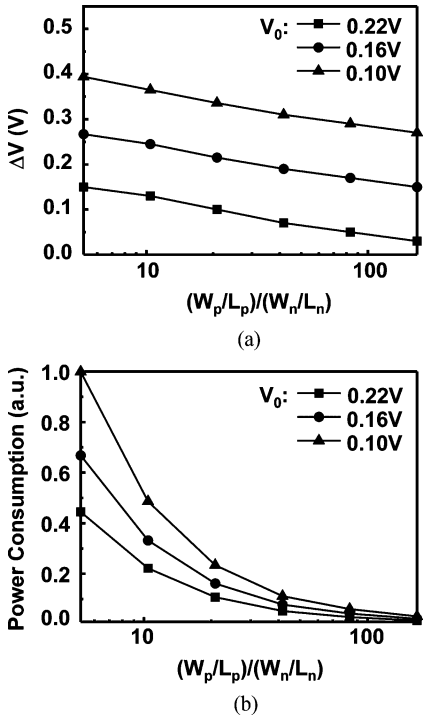


Fig. 7. Simulated ratio dependence. (a) Voltage bias ΔV. (b) Power consumption.

the proposed asynchronous topology, the power consumption of the transceiver can be reduced by 48.3% at 50% data-transition probability.

IV. DC Power-Free Pulse Detector

A. DC Power Dissipation of Conventional Receiver

The receiver requirements depend upon the details of the interconnecting medium and the expected signal degradation from driver to receiver. Capacitive coupling is implemented by forming one of the electrodes on the pad of the TX/RX sheet and the other electrode on the pad of the communication sheet. When the chip is brought into extremely close proximity, a capacitor is formed. In this implementation, no mechanism exists to allow dc input voltage to pass through the same interface as the ac coupled signals. In the conventional capacitive-coupling transceiver, the dc level of the received signal is first biased to a reference voltage, and then, an amplifier and a comparator is used in the first stage of the receiver to amplify the signal for the following demodulation [14], [16]. The major disadvantage of this topology is the large dc power dissipation that occurs even for no ac input. In the transmitted signal of the communication sheet, the circuit spends long periods of time with no ac signal. Power dissipated in these periods is wasted.

B. DC Power-Free Pulse Detector

The design aims to minimize the dc power consumption by implementing a dynamic threshold receiver and a pulse detection approach that maximize power efficiency. The proposed dc power-free pulse detector is basically based on the CMOS inverter. As shown in Fig. 6(a), the gate of the inverter is biased to $V_{\rm DD}/2$ and capacitively coupled to the received data while the source of the inverter is biased to $V_{\rm DD}/2-\Delta V$ and capacitively coupled to the inverted received data. Fig. 6(b) shows the voltages on nodes A and B and the logical threshold of the inverter. When the received voltage on node A and the logical threshold $V_{\rm th}$ of the inverter are overlapped, the pulse is detected, and the power is only consumed on this period. Unbalanced inverters with lower threshold voltages can be used to further reduce the power consumption. As shown in Fig. 7, for the given received voltage, the required bias ΔV and the power consumption can

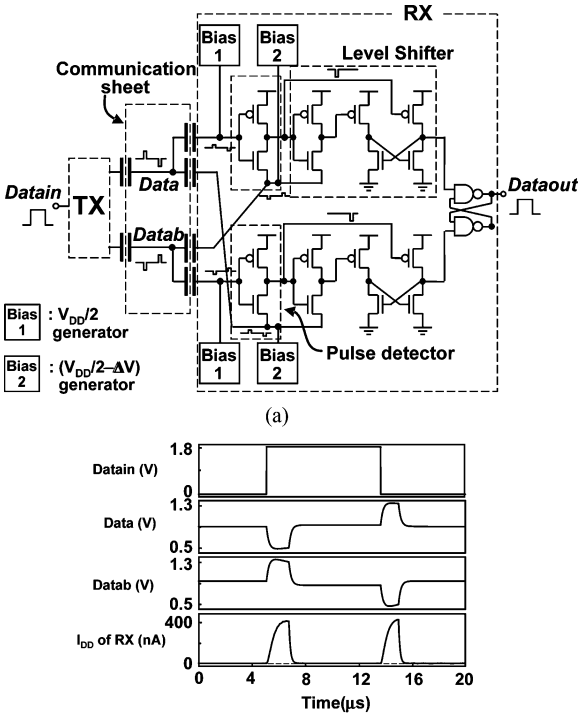


Fig. 8. DC power-free receiver. (a) Circuit schematic. (b) Simulated waveforms.

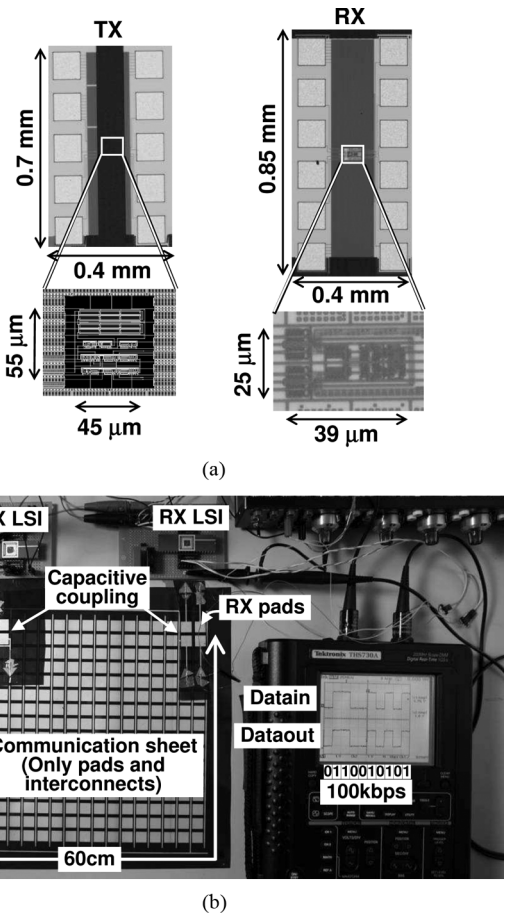


Fig. 9. (a) Chip micrographs. (b) Measurement setup.

be decreased with the increase of the ratio between PMOS and NMOS.

Fig. 8(a) shows the circuit schematic of the proposed pulse detector. Two unbalanced inverters are used to detect the rising and falling edges, respectively, and the detection results are level shifted to $V_{\rm DD}$. The simulated waveforms of the received signal and power supply current of the two inverters are shown in Fig. 8(b). The proposed pulse detector consumes essentially zero power dissipation for no ac input.

V. Measurement Results

A. Performance Summary

A test chip was designed and fabricated in 0.18-μm 1P6M CMOS process, and the microphotograph is shown in Fig. 9(a). The core area for the TX and RX are 2475 and 975 μm^2, respectively. Fig. 9(b) shows the measurement setup. The TX/RX chips are bonded to the TX/RX pads on the TX/RX sheet, and the pads are capacitively coupled to the communication sheet. To simplify the measurement, the MEMS switching matrices, the organic nonvolatile memory array, and the position-detection coil array are removed, and the communication route is laid out to 60 cm directly.

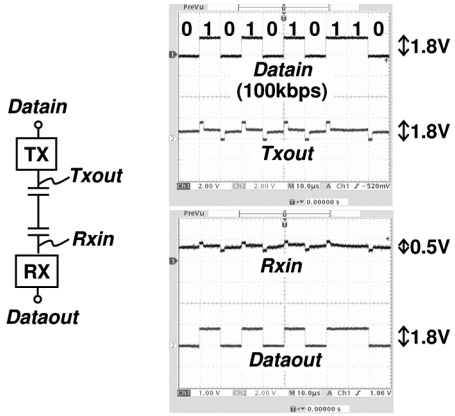
The measured performance is summarized in Table I. The developed data edge signaling and the dc power-free pulse detector enable 107-pJ/bit energy consumption at 100 kb/s. Fig. 10(a) shows the measured waveforms at 100 kb/s. The transmitted data are converted to return-to-$V_{\rm DD}/2$ signal Txout, and the amplitude of Txout is 1.8 V. The amplitude of the received signal Rxin is 0.5 V, and Dataout is the demodulation output. The eye diagram at the maximum data rate of 8 Mb/s is shown in Fig. 10(b). The maximum data rate is determined by the drive current of the transceiver and the parasitic capacitance of the communication sheet. For the given parameters of the communication sheet, a higher data rate can be achieved by increasing the drive current of the transmitter and the receiver.

TABLE I
Performance Summary

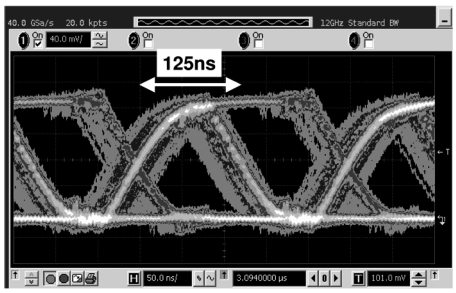
Technology		0.18μm CMOS
Supply Voltage		1.8V
Data Rate	Typ	100kbps
	Max	8Mbps
Communi-cation Distance	Capacitive Coupling	150μm
	Wireline	60cm
Alignment Tolerance		7.5mm
Power @100kbps	TX	9.73μW
	RX	0.97μW
	Total	10.7μW
Energy per bit		107pJ/bit
Core Area	TX	2475μm^2
	RX	975μm^2

B. Misalignment Tolerance

For the capacitive-coupling system, a critical challenge in high-performance communication is correctly aligning the pads on the sheets. In an aligned proximity communication system, each TX/RX pad lines up perfectly with a routing pad, and the



(a)



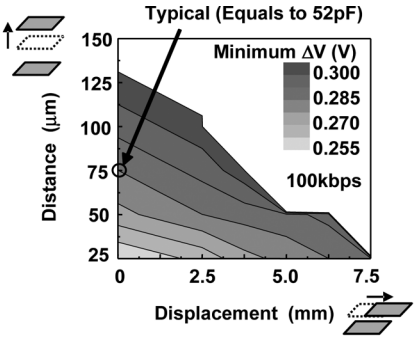
(b)

Fig. 10. Measurement results. (a) Measured waveforms at 100 kb/s. (b) Eye diagram at 8 Mbits/s.

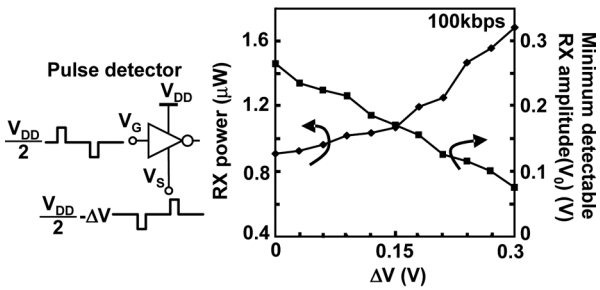
pads are pushed together such that their dielectric and passivation surfaces touch or nearly touch, thus maximizing the signal coupled between the pads, reducing the parasitic capacitance, and saving the power. With misaligned pads, one transmitter will be coupled to several other receivers, simultaneously reducing the intended signal and increasing crosstalk to the other receiver.

Fig. 11(a) shows the measured sensitivity requirement for the horizontal misalignment and the vertical pad distance. The contour represents the required minimum ΔV to achieve the capacitive-coupling communication. For the normal 75-μm pad distance, which is equal to the sheet thickness, the sheet can operate up to 3.75-mm displacement. The maximum tolerable displacement is 7.5 mm, which corresponds to the 77% of the pad size.

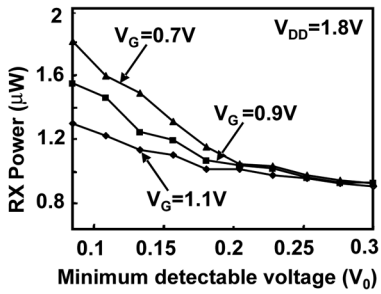
The sensitivity of the receiver is tuned by the source bias voltage of the inverter. The amplitude of the received voltage can be approximated by $V_{\rm rx} = V_{\rm tx} \times C_c/(C_c + C_s)$. With the increased size of the communication sheet, the parasitic capacitance of the sheet will be increased, and therefore, the received voltage will be reduced. The tradeoff between the RX sensitivity and the power consumption is shown in Fig. 11(b). By reducing the bias voltage $V_{\rm DD}/2 - \Delta V$, the sensitivity of the receiver can be increased and communication distance can be extended but the power consumption will be increased. The power consumption of the receiver can be further reduced by lowering the supply voltage. Fig. 11(c) shows the measured supply voltage dependence of power consumption. The voltages V_G and $V_S(= V_G - \Delta V)$ represent the gate and source biases,



(a)



(b)



(c)

Fig. 11. (a) ΔV dependence of displacement. (b) Tradeoff between power and sensitivity. (c) Supply voltage dependence of power consumption.

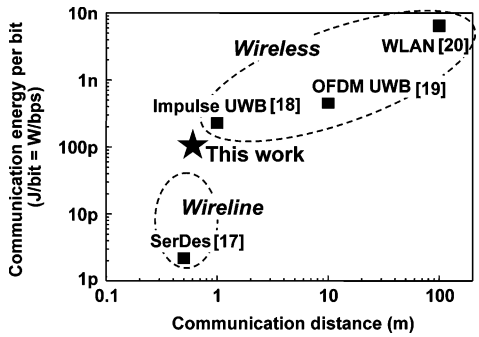


Fig. 12. Comparison with the state-of-the-art wireless and wireline communications.

respectively. Lower power consumption is achieved with lower supply voltage $(V_{\rm DD} - V_S)$.

Fig. 12 shows the comparison with the state-of-the-art communication systems [17]–[20]. Wireline communication refers to the transmission of data over a wire-based communication technology. Examples include telephone networks, cable television, and fiber-optic communication. Alternatively, wireless communication is used to describe telecommunications in which electromagnetic waves carry the signal over

the communication path. Examples of short-distance wireless technology include wireless LAN and ultrawideband. Compared to wireless communication, the communication sheet fills the space around it with a nonradiative electric field instead of irradiating the whole environment with electromagnetic waves. As shown in Fig. 12, the proposed communication method achieves lower energy consumption than conventional wireless communication, thus realizing a low-energy feature of wireline communication with an easy-to-use feature of wireless communication.

VI. Conclusion

A transceiver for the printable 20 cm $\times$ 20 cm communication sheet combining the capacitive coupling and the point-to-point connection from TX to RX on the sheet has been developed. The transceiver with a data-edge-signaling transmitter and dc power-free pulse detector achieves the lowest energy of 107 pJ/bit at 100 kb/s in the wireless communications at a distance of 60 cm in 0.18-μm CMOS. The proposed data-edge-signaling transmitter avoid the dc wander effect by converting the input NRZ signal to return-to-$V_{\mathrm{DD}}/2$ signal. For the 50% data-transition probability, the power consumption of the transceiver can be reduced by 48.3%. The proposed dc power-free detector has essentially zero power dissipation for no ac input, and the four-pad differential signaling scheme can tolerate 7.5-mm misalignment, which corresponds to 77% of the pad size.

Acknowledgment

The electronic-design-automation (EDA) tools are supported by the VLSI Design and Education Center, The University of Tokyo, Tokyo, Japan, in collaboration with Cadence Design Systems, Inc., Synopsys, Inc., and Mentor Graphics, Inc.

References

[1] L. Liu, M. Takamiya, T. Sekitani, Y. Noguchi, S. Nakano, K. Zaitsu, T. Kuroda, T. Someya, and T. Sakurai, "A 107 pJ/b 100 kb/s 0.18 μm capacitive-coupling transceiver for printable communication sheet," in *Proc. IEEE ISSCC Tech. Dig. Papers*, 2008, pp. 292–293.

[2] T. Sekitani, Y. Noguchi, S. Nakano, K. Zaitsu, Y. Kato, M. Takamiya, T. Sakurai, and T. Someya, "Communication sheets using printed organic nonvolatile memories," in *IEDM Tech. Dig.*, 2007, pp. 221–224.

[3] T. Sekitani, M. Takamiya, Y. Noguchi, S. Nakano, Y. Kato, K. Hizu, H. Kawaguchi, T. Sakurai, and T. Someya, "A large-area flexible wireless power transmission sheet using printed plastic MEMS switches and organic field-effect transistors," in *IEDM Tech. Dig.*, 2006, pp. 287–290.

[4] M. Takamiya, T. Sekitani, Y. Miyamoto, Y. Noguchi, H. Kawaguchi, T. Someya, and T. Sakurai, "Design solutions for multi-object wireless power transmission sheet based on plastic switches," in *Proc. IEEE ISSCC Tech. Dig. Papers*, 2007, pp. 362–363.

[5] R. J. Drost, R. D. Hopkins, R. Ho, and I. E. Sutherland, "Proximity communication," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1529–1535, Sep. 2004.

[6] A. Fazzi, R. Canegallo, L. Ciccarelli, L. Magagni, F. Natali, E. Jung, P. L. Rolandi, and R. Guerrieri, "3D capacitive interconnections with mono- and bi-directional capabilities," in *Proc. IEEE ISSCC Tech. Dig. Papers*, 2007, pp. 356–357.

[7] A. Fazzi, L. Magagni, M. Mirandola, B. Charlet, L. Di Cioccio, E. Jung, R. Canegallo, and R. Guerrieri, "3-D capacitive interconnections for wafer-level and die-level assembly," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2270–2282, Oct. 2007.

[8] N. Miura, H. Ishikuro, T. Sakurai, and T. Kuroda, "A 0.14 pJ/b inductive-coupling inter-chip data transceiver with digitally-controlled precise pulse shaping," in *Proc. IEEE ISSCC Tech. Dig. Papers*, 2007, pp. 358–359.

[9] N. Miura, Y. Kohama, Y. Sugimori, H. Ishikuro, T. Sakurai, and T. Kuroda, "An 11 Gb/s inductive-coupling link with burst transmission," in *Proc. IEEE ISSCC Tech. Dig. Papers*, 2008, pp. 298–299.

[10] M. Ghovanloo and S. Atluri, "An integrated full-wave CMOS rectifier with built-in back telemetry for RFID and implantable biomedical applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 10, pp. 3328–3334, Nov. 2008.

[11] C. Sauer, M. Stanacevic, G. Cauwenberghs, and N. Thakor, "Power harvesting and telemetry in CMOS for implanted devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2605–2613, Dec. 2005.

[12] C. Dong, D. Chen, S. Haruehanroengra, and W. Wang, "3-D nFPGA: A reconfigurable architecture for 3-D CMOS/nanomaterial hybrid digital circuits," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 11, pp. 2489–2501, Nov. 2007.

[13] T. J. Gabara and W. C. Fischer, "Capacitive coupling and quantized feedback applied to conventional CMOS technology," *IEEE J. Solid-State Circuits*, vol. 32, no. 3, pp. 419–427, Mar. 1997.

[14] K. Kanda, D. D. Antono, K. Ishida, and T. Sakurai, "1.27 Gb/s/pin 3 mW/pin wireless super-connect (WSC) interface scheme," in *Proc. IEEE ISSCC Tech. Dig. Papers*, 2003, pp. 288–289.

[15] S. Fujii, S. Saito, Y. Okada, M. Sato, S. Sawada, S. Shinozaki, K. Natori, and O. Ozawa, "A 50 pA standby 1 MW $\times$1 b/256 KW $\times$ 4 b CMOS DRAM," in *Proc. IEEE ISSCC Tech. Dig. Papers*, 1986, pp. 266–269.

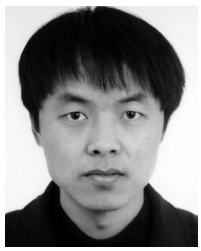
[16] A. Tamtrakarn, H. Ishikuro, K. Ishida, M. Takamiya, and T. Sakurai, "A 2.3 mW baseband impulse-UWB transceiver front-end in CMOS a 1-V 299 μW flashing UWB transceiver based on double thresholding scheme," in *Proc. IEEE Symp. VLSI Circuits Tech. Dig. Papers*, 2006, pp. 250–251.

[17] R. Palmer, J. Poulton, W. J. Dally, J. Eyles, A. M. Fuller, T. Greer, M. Horowitz, M. Kellam, F. Quan, and F. Zarkeshvari, "A 14 mW 6.25 Gb/s transceiver in 90 nm CMOS for serial chip-to-chip communications," in *Proc. IEEE ISSCC Tech. Dig. Papers*, 2007, pp. 440–441.

[18] I. D. O'Donnell and R. Brodersen, "A 2.3 mW baseband impulse-UWB transceiver front-end in CMOS," in *Proc. IEEE Symp. VLSI Circuits Tech. Dig. Papers*, 2006, pp. 200–201.

[19] J. R. Bergervoet, K. S. Harish, S. Lee, D. Leenaerts, R. van de Beek, G. van der Weide, and R. Rooverss, "A WiMedia-compliant UWB transceiver in 65 nm CMOS," *Proc. IEEE ISSCC Tech. Dig. Papers*, pp. 112–113, 2007.

[20] M. Simon, P. Laaser, V. Filimon, H. Geltinger, D. Friedrich, Y. Raman, and R. Weigel, "An 802.11a/b/g RF transceiver in an SoC," *Proc. IEEE ISSCC Tech. Dig. Papers*, pp. 562–563, 2007.



Lechang Liu received the B.S. degree from Shandong University, Jinan, China, in 2000, the M.S. degree from Harbin Institute of Technology, Harbin, China, in 2002, and the Ph.D. degree in electronic engineering from Shanghai Jiao Tong University, Shanghai, China, in 2006.

From 2007 to 2009, he was with VLSI Design and Education Center, The University of Tokyo, Japan, where he conducted research on low-power and high-performance impulse radio ultra-wideband (UWB) transceivers. Since 2009, he has been a project researcher with the Institute of Industrial Science, The University of Tokyo, Japan. His current research interests include signal processing and mixed-signal circuit design for low-power wireless communications.

Makoto Takamiya (S'98–M'00) received the B.S., M.S., and Ph.D. degrees in electronic engineering from The University of Tokyo, Tokyo, Japan, in 1995, 1997, and 2000, respectively.

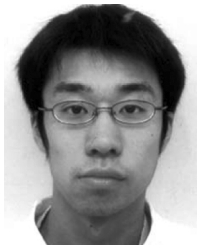
In 2000, he joined NEC Corporation, Japan, where he was engaged in the circuit design of high-speed digital large-scale integration. In 2005, he joined The University of Tokyo, where he is an Associate Professor with the VLSI Design and Education Center. His research interests include the circuit design of low-power RF circuits, ultralow-voltage digital circuits, and large-area electronics with organic transistors.

Dr. Takamiya is a member of the technical program committees for the IEEE Symposium on VLSI Circuits and the IEEE Custom Integrated Circuits Conference.

Tsuyoshi Sekitani was born in Yamaguchi, Japan, in 1977. He received the B.S. degree from Osaka University, Osaka, Japan, in 1999, and the Ph.D. degree in applied physics from The University of Tokyo, Tokyo, Japan, in 2003.

From 1999 to 2003, he was with the Institute for Solid State Physics, The University of Tokyo, where he developed measurement techniques in magnetic fields up to 600 T and studied the solid-state physics of condensed matter, particularly in high-Tc superconductors, and where he has been a Research Associate with the Quantum-Phase Electronics Center since 2003. His current object of physics research is organic semiconductors and organic-FET devices.

Dr. Sekitani is a member of the Materials Research Society, the Physical Society of Japan, and the Japanese Society of Applied Physics.



Yoshiaki Noguchi was born in Kanagawa, Japan, in 1983. He received the M.S. degree in applied physics from The University of Tokyo, Tokyo, Japan, in 2007, where he is currently working toward the Ph.D. degree in applied physics.

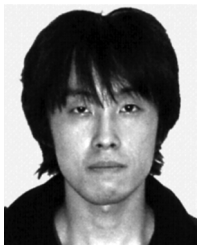
His research interests include organic transistors, large-area electronics, and printed electrical devices.

Mr. Noguchi is a student member of the Japanese Society of Applied Physics. He is also a member of the Japan Society for the Promotion of Science Research Fellowships.

Shintaro Nakano received the M.S. degree in applied physics from The University of Tokyo, Tokyo, Japan, in 2008, where he developed large-area printed microelectromechanical systems switches for organic electronics.

He is currently with Toshiba Corporation, Tokyo, Japan.

Mr. Nakano was the recipient of the Tanaka Shoji Award for applied physics from The University of Tokyo in 2008.



Koichiro Zaitsu was born in Oita, Japan, in 1984. He received the B.S. degree in applied physics from The University of Tokyo, Tokyo, Japan, in 2007, where he is currently working toward the M.S. degree in applied physics.

His research interests include ferroelectric polymers and new devices integrated with organic transistors.

Mr. Zaitsu is a member of the Japanese Society of Applied Physics.

Tadahiro Kuroda (M'88–SM'00–F'06) received the Ph.D. degree in electrical engineering from The University of Tokyo, Tokyo, Japan, in 1999.

In 1982, he joined Toshiba Corporation, Tokyo, Japan, where he designed CMOS SRAMs, gate arrays, and standard cells. From 1988 to 1990, he was a Visiting Scholar with the University of California, Berkeley, where he conducted research in the field of VLSI computer-aided design. In 1990, he returned to Toshiba Corporation where he was engaged in the research and development of BiCMOS application-specified integrated circuits, emitter-coupled-logic gate arrays,ECL high-speed CMOS large-scale integrations (LSIs) for telecommunications, and low-power CMOS LSIs for multimedia and mobile applications. He invented a variable threshold-voltage CMOS technology to control VTH through substrate bias and applied it to a DCT core processor and a gate array in 1995. He also developed a variable supply-voltage scheme using an embedded dc–dc converter and employed it to a microprocessor core and an MPEG-4 chip for the first time in the world in 1997. In 2000, he joined Keio University, Yokohama, Japan, where he has been a Professor since 2002. He has been a Visiting Professor with both Hiroshima University, Hiroshima, Japan, and University of California, Berkeley. He has published more than 200 technical publications, including 50 invited papers and 20 books/chapters, and has filed more than 100 patents. His research interests include low-power high-speed CMOS design for wireless and wireline communications, human–computer interactions, and ubiquitous electronics.

Dr. Kuroda is an elected AdCom member for the IEEE Solid-State Circuits Society (SSCS) and an IEEE SSCS Distinguished Lecturer. He was the General Chairman for the Symposium on VLSI Circuits, the Vice Chairman for the Asia and South Pacific Design Automation Conference (ASP-DAC), the subcommittee chair for the Asian Solid-State Circuits Conference, the International Conference on Computer-Aided Design, and the Structures, Structural Dynamics, and Materials Conference (SSDM), and a program committee member for the Symposium on VLSI Circuits, Custom Integrated Circuits Conference, DAC, ASP-DAC, International Symposium on Low-Power Electronics and Design, SSDM, International Symposium on Quality Electronic Design, and other international conferences. He is a recipient of the 2005 IEEE System LSI Award, the 2005 P&I Patent of the Year Award, the 2006 LSI IP Design Award, the 2006 IP/SoC Best Design Paper Award, and the 2007 ASP-DAC Best Design Award.

Takao Someya (M'03) received the Ph.D. degree in electrical engineering from The University of Tokyo, Tokyo, Japan, in 1997.

In 1997, he joined the Institute of Industrial Science, The University of Tokyo, as a Research Associate. He was appointed as a Lecturer with the Research Center for Advanced Science and Technology, The University of Tokyo, in 1998, where he was an Associate Professor in 2002. From 2001 to 2003, he was with the Nanoscale Science and Engineering Center, Columbia University, New York, NY, and with Bell Labs, Lucent Technologies, as a Visiting Scholar. Since 2003, he has been an Associate Professor with the Department of Applied Physics and the Quantum-Phase Electronics Center, The University of Tokyo. His current research interests include organic transistors, flexible electronics, plastic integrated circuits, large-area sensors, and plastic actuators.

Prof. Someya is a member of the IEEE Electron Devices Society, the Materials Research Society, and the Japanese Society of Applied Physics. He is a subcommittee member for IEEE International Electron Devices Meeting and a program cochair for the Third Organic Microelectronics Workshop.

Takayasu Sakurai (S'77–M'78–SM'01–F'03) received the Ph.D. degree in electrical engineering from The University of Tokyo, Japan, in 1981.

In 1981, he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and system-on-a-chip solutions. He has worked extensively on interconnect delay and capacitance modeling known as the Sakurai model and the alpha power-law MOS model. From 1988 to 1990, he was a Visiting Researcher with the University of California, Berkeley, where he conducted research in the field of VLSI computer-aided design. Since 1996, he has been a Professor with The University of Tokyo, Tokyo, Japan, working on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic ICs, and large-area electronics. He has published more than 350 technical publications, including 70 invited publications and several books, and filed more than 100 patents.

Dr. Sakurai is a Semiconductor Technology Academic Research Center (STARC) fellow, an elected AdCom member for the IEEE Solid-State Circuits (SSC) Society, and an IEEE Circuits and Systems Society Distinguished Lecturer. He was a Conference Chair for the Symposium on VLSI Circuits and the International Conference on IC Design and Technology (ICICDT), a Vice Chair for the Asia and South Pacific Design Automation Conference, a Technical Program Committee Chair for the first Asian Solid-State Circuits Conference and the VLSI Symposia, and a program committee member for the International Solid-State Circuits Conference (ISSCC), Custom Integrated Circuits Conference, Design Automation Conference, European Solid-State Circuits Conference, International Conference on Computer-Aided Design, FPGA Workshop, International Symposium on Low-Power Electronics and Design, TAU, and other international conferences. He is a plenary speaker for the 2003 ISSCC. He is a recipient of the 2005 IEEE ICICDT Award, 2005 IEEE ISSCC Takuo Sugano Award, and the 2005 P&I Patent of the Year Award.