28.3 A Stretchable EMI Measurement Sheet with 8×8 Coil Array, 2V Organic CMOS Decoder, and -70dBm EMI Detection Circuits in 0.18μm CMOS

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Electromagnetic interference (EMI) is a serious issue degrading the dependability of electronic devices. The issue is complicated by the following technology trends: 1) RF signals and clock pulses of digital ICs are in the same frequency range. 2) The increase of LSI power consumption causes an increase of noise emission. 3) Electronic devices have 3D-structures and packaging is dense. These trends also make the root cause analysis of EMI difficult. For example, it is difficult to find the EMI generation points in electronic devices such as cell-phones and PDAs.

Typical frequencies of concern with respect to EMI issues is from 30MHz to 1GHz as specified by CISPR, International Special Committee on Radio Interference. Although the noise power is specified by electric field strength in general, magnetic field probes with X-Y scanning equipment and spectrum analyzers are used as an easy EMI measurement method. The conventional method is, however, not applicable to 3D-structure devices since the scanning equipment can only move in a flat plane.

To solve the problem, an EMI measurement sheet is proposed, which enables the measurement of the EMI distribution on the surface of the electronic devices by wrapping the devices with a sheet like "*furoshiki*".

Figure 28.3.1 shows the photograph and block diagram of the EMI measurement sheet. The 12cm×12cm sheet has a 4×4 PCB array and 2 organic circuits (decoder and selector). The PCBs and the organic circuits are connected by stretchable interconnects [1, 2] including carbon nanotubes, and the whole system is covered with a rubber sheet, which enables the sheet to be stretched. Each PCB has a 2×2 coil array picking up EMI, an LSI, and 6 stretchable interconnects. The 4 coils share the LSI. The coils are made on a rigid PCB, since coils on a flexible film cause unstable antenna characteristics. In such large-area array structures, a low-cost and large-area decoder is required to reduce the number of interconnects and organic transistors are suitable for the decoder [3]. Figure 28.3.1(c) shows the photograph of the organic CMOS 3-to-8 decoder on polyimide film. In the conventional organic design, only PMOS was available and the power supply voltage was 40V [4]. The low gain circuits in the PMOS only design and the high voltage makes the fusion of the organic circuits and LSIs difficult. To solve the problem, 2V organic CMOS technology enabled by the 2.1nm thick gate insulator [5] and organic semiconductor [6] for NMOS were developed. As shown in Fig. 28.3.1(d), the diameter of the coil on the PCB is 9.8mm. Figure 28.3.1(e) shows the 40% stretchable interconnect.

The 2V organic CMOS technology allows direct signal transmission between organic circuits and LSIs, which eliminates the level shifters [4]. Figure 28.3.2(a) shows the circuit of the 3-to-8 organic CMOS decoder. A key part of the decoder was fabricated on a silicon substrate and Fig. 28.3.2(b) shows the photograph. Figure 28.3.2(c) shows the measurement setup for the direct signal transmission between the organic circuits and an LSI. The power supply voltage for both the organic circuits and the LSI is 2.0V. The organic circuits and the LSI are connected by 12cm-stretchable interconnect. The width is 1mm, the thickness is 500μm, the resistance is 48Ω, and the resistivity is 0.02Ω cm. Figure 28.3.2(d) shows the measured waveform of both the input and output of the organic circuits and the LSI. The organic CMOS decoder successfully drives the LSI. Both the rise time and fall time of the output of the organic decoder are 0.5s, which is very slow but acceptable in this application.

Figure 28.3.3 depicts the circuit diagram of the proposed LSI. The circuit consists of four-stage amplifiers, an NMOS rectifier, sample and hold, and a comparator. The circuit handles differential signals from the antenna coil to measure magnetic fields rather than electric fields [7]. To capture the noise waveform up to 1GHz digitally, the bandwidth of a comparator should be 10GHz or higher, which is not reasonable. The system, therefore, detects the EMI noise power as a DC voltage level with an NMOS rectifier and a sample and hold. The noise power is observed as a function of reference voltage of the comparator. The rectifier relaxes comparator design of both speed and resolution. In fact, the comparator can operate at 100kHz. EMI noise of -70dBm, equivalent to 45μV with 50Ω input resistance, is picked up by the coil and raised to proper level by amplifiers that connect to the rectifier. The four-stage amplifiers have a gain of around 80dB. The bandwidth of the final stage amplifier can be changed by simply cutting off some parallel transistors. The EMI noise frequency can be roughly estimated by this selectable bandwidth amplifier.

Figure 28.3.4 shows measurement configuration of the proposed silicon chip and measurement result of the minimum detectable EMI noise power and dynamic range. Input noise is emulated by using a signal generator and a coil, and its magnetic field strength is monitored with a magnetic field probe (NEC CP-2S) and a spectrum analyzer. EMI noise power is plotted as a function of the reference voltage of the comparator. The measurement result demonstrates that the proposed system can detect minimum noise power of -70dBm with 25dB dynamic range and a maximum detectable frequency of 1GHz.

Figure 28.3.5 demonstrates that the proposed circuit can roughly estimate EMI noise frequency by changing the bandwidth of the amplifier. 900MHz EMI noise was measured. The left image in Fig. 28.3.5 shows the density of a high pulse output from the comparator is 71% with a wide bandwidth setting, and 100MHz cutoff frequency, and the right image shows a density of 24% of a high pulse output with a narrow bandwidth setting. This result indicates the measured EMI noise frequency is high. If the measured EMI noise frequency is low (e.g., 100MHz), the difference of the high pulse density is small when changing the bandwidth of the amplifier.

Figure 28.3.6 demonstrates the correlation of EMI measurement between the magnetic field probe and the proposed scheme. EMI noise around a memory module in a notebook PC is measured. The output spectrum by the magnetic field probe includes a peak noise power of -50dBm at 267MHz and its harmonic tones. On the other hand, the output bit stream by the proposed EMI measurement system shows a high pulse density of 81% at the same place. Without any EMI noise, the output bit stream includes no high pulses as shown in Fig. 28.3.6. Thus, the proposed system successfully detects the actual noise emitted by the electronic device.

Figure 28.3.7(a) shows the die micrograph and the layout. The LSI is implemented in a 0.18μm CMOS process and the core area is 0.18mm^2. Key features of the LSI for the EMI measurement are summarized in Fig. 28.3.7(b).

Co-integration of silicon CMOS technology, 2V organic CMOS technology, and stretchable interconnect including carbon nanotubes makes a stretchable EMI measurement sheet possible, and the proposed LSI demonstrates EMI noise measurement up to 1GHz by using an NMOS rectifier and a comparator operating at only 100kHz.

References:
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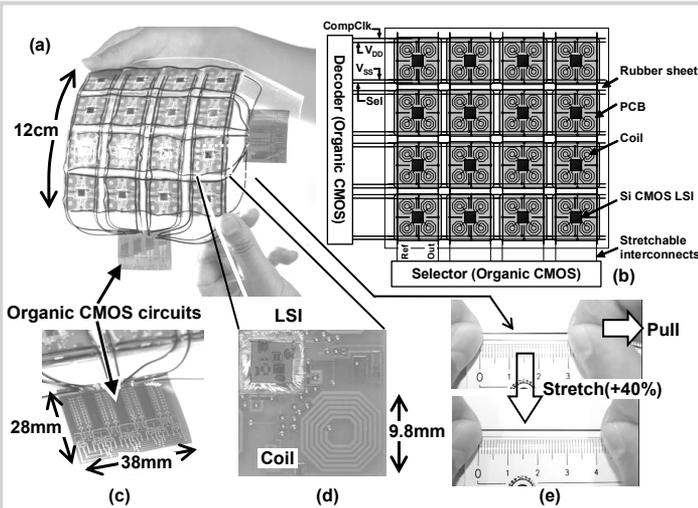
Figure 28.3.1: (a) Photograph of EMI measurement sheet. (b) Block diagram. (c) Organic CMOS decoder. (d) Coil on PCB and LSI for EMI measurement. (e) Stretchable interconnect including carbon nanotubes.
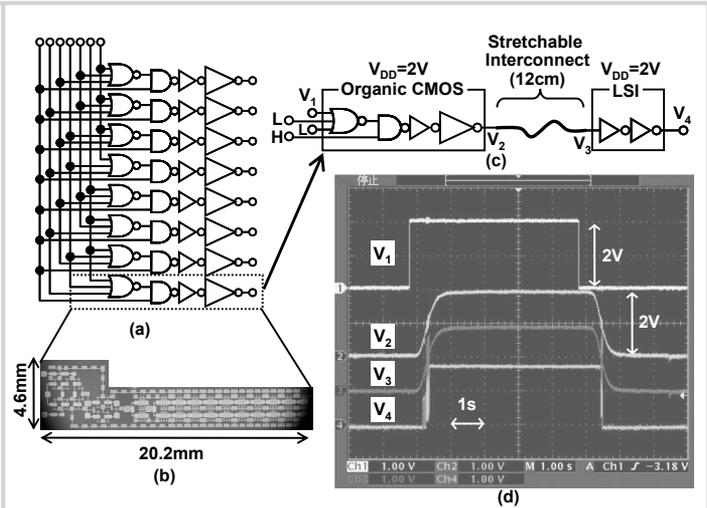

Figure 28.3.2: (a) Organic CMOS 3-to-8 decoder. (b) Photograph of the decoder on Si substrate. (c) Measurement setup for direct connection of organic CMOS and LSI. (d) Measured waveforms in (c).
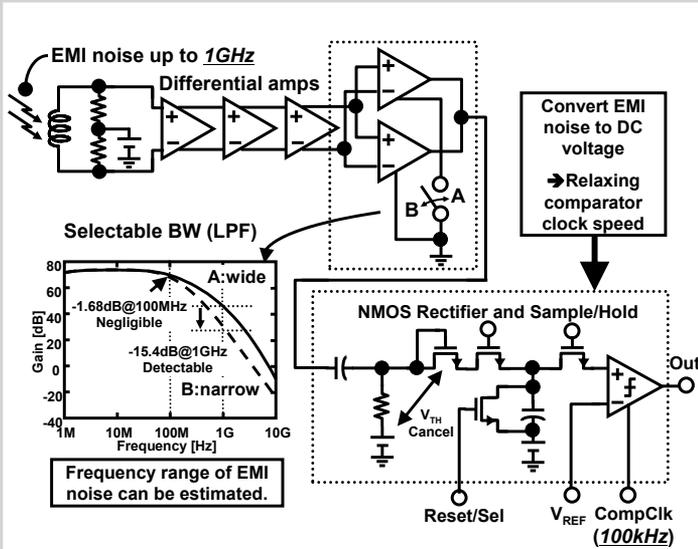

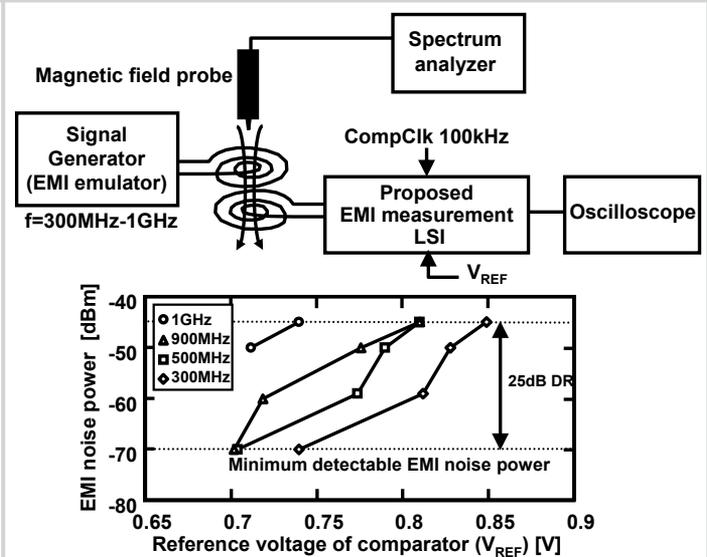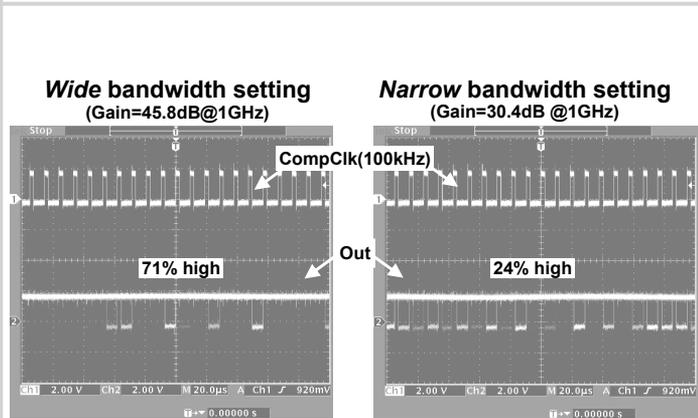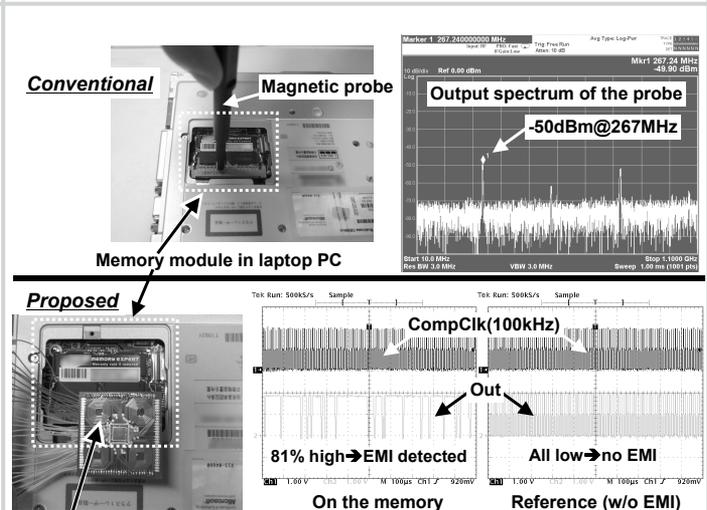Figure 28.3.3: Circuit diagram of the LSI in the proposed EMI measurement sheet.

Figure 28.3.4: Measurement configuration and measured EMI noise power.

Pulse density 71%➔ 24%
By changing BW of amplifier, EMI noise frequency can be estimated.
(The Comparator output is set to high during each pre-charge cycle)

Figure 28.3.5: Measured 900MHz EMI noise with different bandwidth of the amplifiers.

Figure 28.3.6: Correlation of EMI measurement between magnetic probe and proposed scheme.

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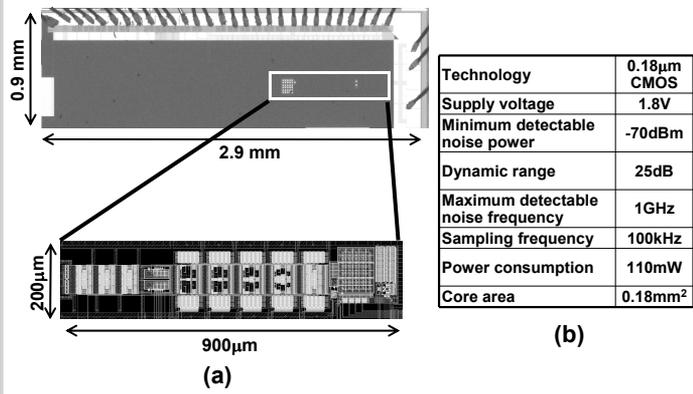| Technology	0.18μm CMOS
Supply voltage	1.8V
Minimum detectable noise power	-70dBm
Dynamic range	25dB
Maximum detectable noise frequency	1GHz
Sampling frequency	100kHz
Power consumption	110mW
Core area	0.18mm²

(b)

Figure 28.3.7: (a) Die micrograph and layout. (b) Summary of key features of LSI for EMI measurement.